Belle 2 DAQ upgrade moving to iFDAQ

Igor Konorov
TUM Physics Department E18

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Talk overview

- FPGA technology
- DAQ limitations
- DAQ upgrade steps
- DAQ upgrade step 1
- FPGA Event Builder
- Summary and concluding remarks

Why to use FPGA

FPGA capability

- Programmable architecture
- High clock frequency of 100-400 MHz
- Pipe line data processing (N steps => N operation simultaneously)
- Parallel architecture => multiple pipelines => performance = M x N
- Real real-time data processing

FPGA features

- DLL, PLL – clock synthesis, clock synchronization
- Built-in memory blocks (RAM/FIFO)
- **Multiple High speed serial links up to 28 Gbps**
  - MAC cores for 1/10/40/100 Gigabit Ethernet, PCIexpress Gen1-Gen3, Custom interfaces
- Soft core SDRAM controllers : 800 MHz bus frequency => 6.4GB/s
- Hard core SDRAM controllers : 2000 MHz bus frequency => 16 GB/s

Logic Density FPGA vs CPU/GPU

Chip	Manufacturer	Technology	Transistor count
Duo-core + GPU Iris Core i7 Broadwell-U	Intel	14 nm	1 900 000 000
22-core Xeon Broadwell-E5	Intel	14 nm	7 200 000 000
Virtex 7	Xilinx	28 nm	6 800 000 000
Virtex Ultra Scale	Xilinx	20 nm	20 000 000 000

FPGA performance parameters

Low cost FPGA (Artix7)

- Memory 1.4MB
- GBT 100 Gbps

High End FPGA (UltraScale)

- Memory 14 MB
- GBT 3000Gbps


FPGA Market Segment Growth
($M)
10,000
9,000
8,000
7,000
6,000
5,000
4,000
3,000
2,000
1,000
0
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
Forecast
Military/Civil Aerospace
Industrial
Automotive
Data Processing
Consumer
Comms

FPGA technology advantages

- Emerging technology, rapidly extends application fields
- Highly parallel architecture
- Enormous IO bandwidth
- Low cost
- Long development time => Software tools for a moment behind complexity of HW technology

FPGA is ideal technology

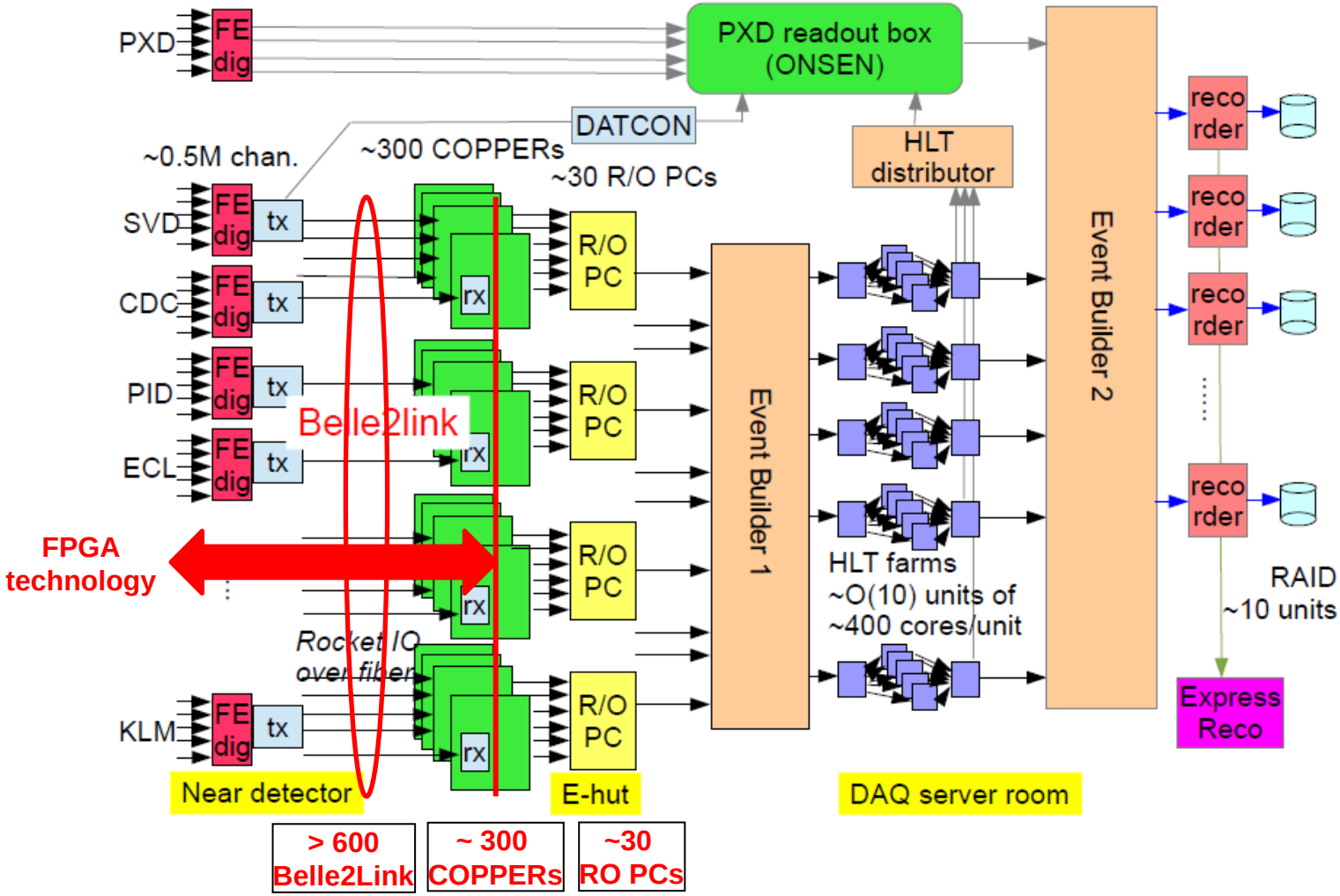
for development reliable, high performant, low cost DAQ system

iFDAQ (intelligent FPGA DAQ)

Reliability achieved by smart recovery algorithms included in FPGA

BELLE 2 DAQ

Belle 2 DAQ architecture



DAQ limitations

Although the DAQ fulfills Belle2 requirements there is a concern about long term operation of COPPER modules.

My concern is related to stability and reliability of the system due to system complexity and small performance safety margin. From my point of view it may significantly reduce UP time of the system

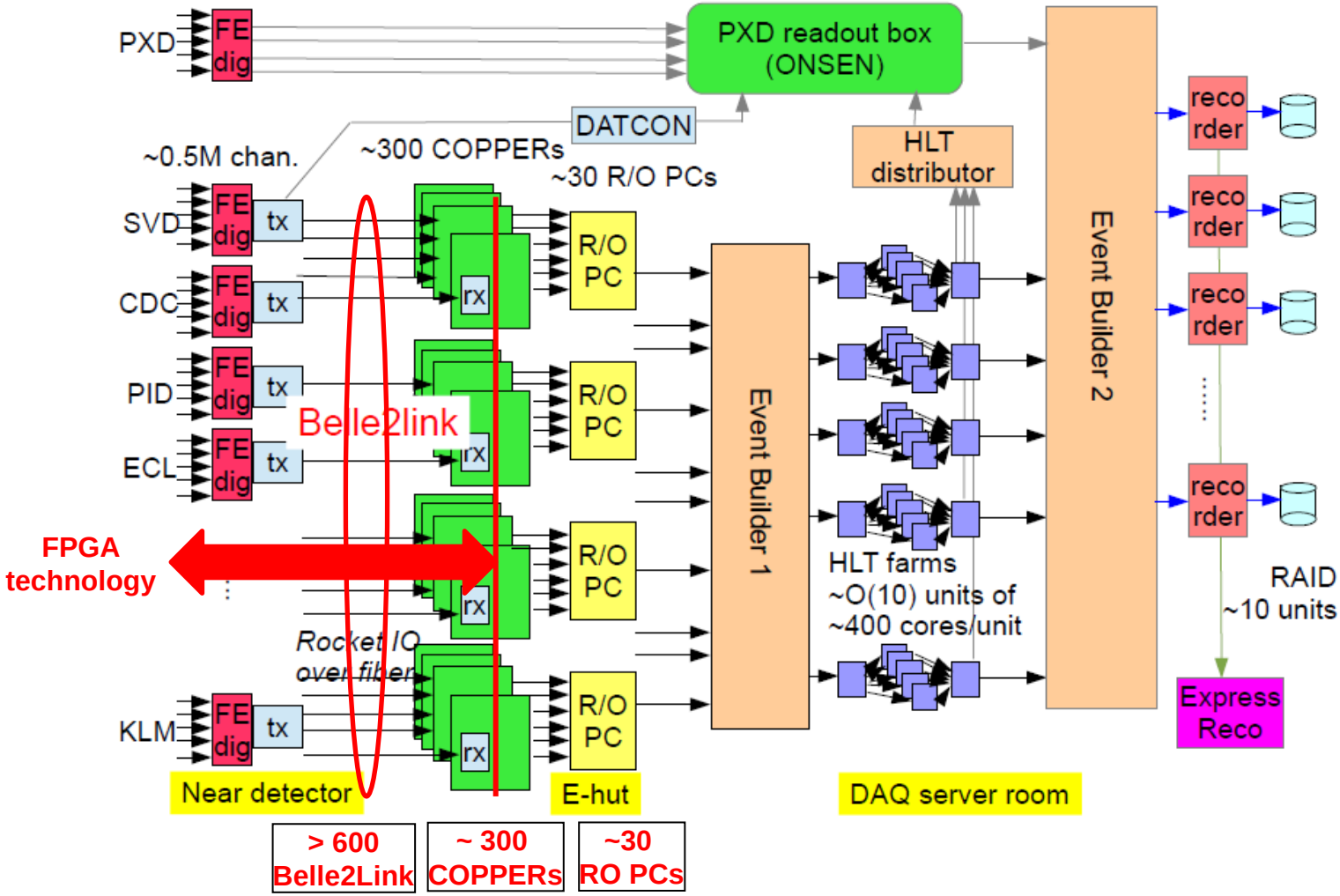
A main component which limits DAQ performance is COPPER module

- Small multiplexing factor 4:1, 2:1 and 1:1 => ~300 COPPERs employed
- Low performance and obsolete PCI technology
- Limited embedded CPU performance
  - Limited data rate
  - Limited maximum event size

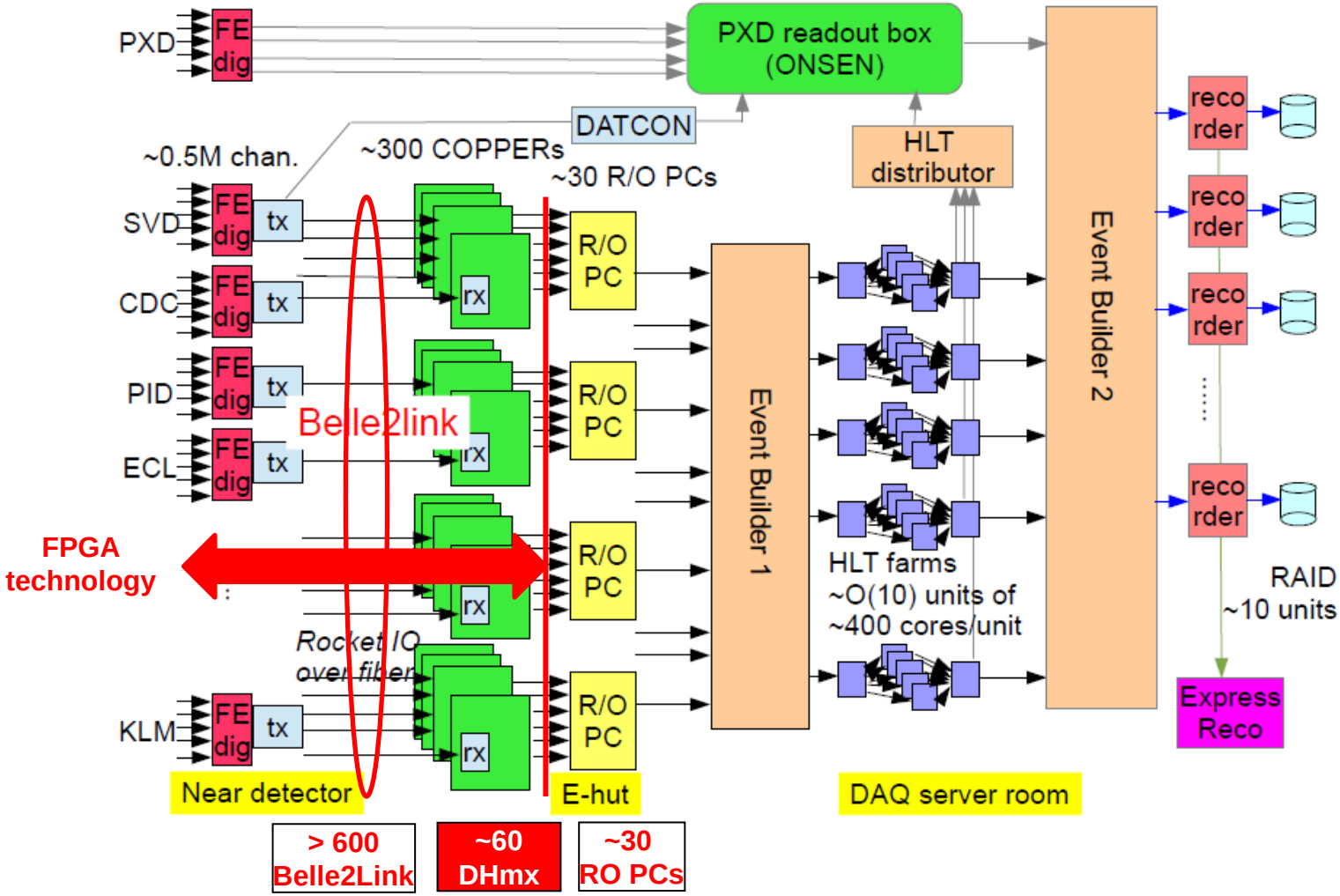
DAQ reliability will be affected by :

1. Number of DAQ HW components ~ 1000 (HSLB + COPPER)
   - Hardware failure proportional to number of components
   - Even very small instability of hardware or firmware will be amplified by number of system components
2. Big number of real time processes > 1000
   - Synchronization of so many processes for real time operation is additional complication

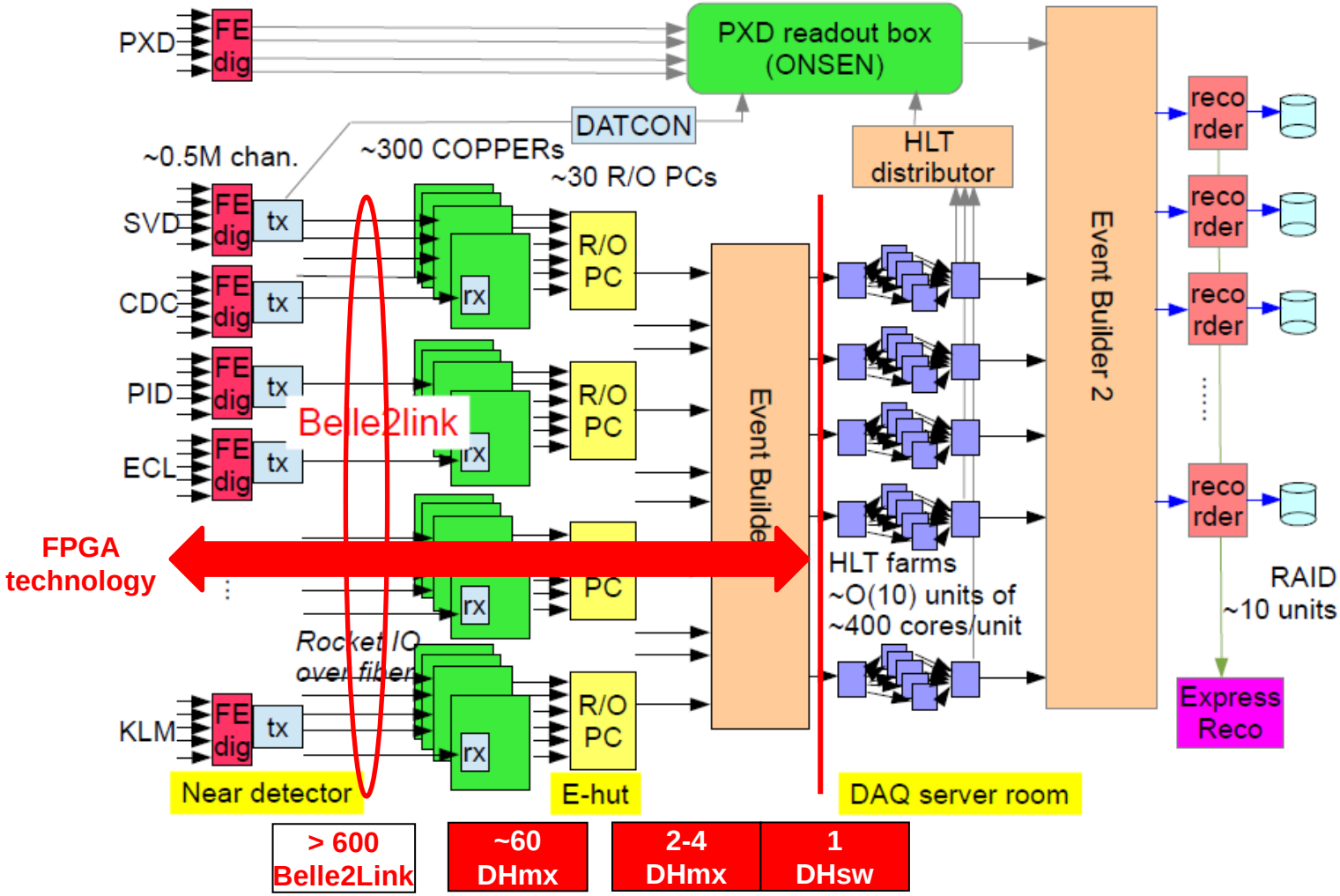
Belle 2 DAQ architecture



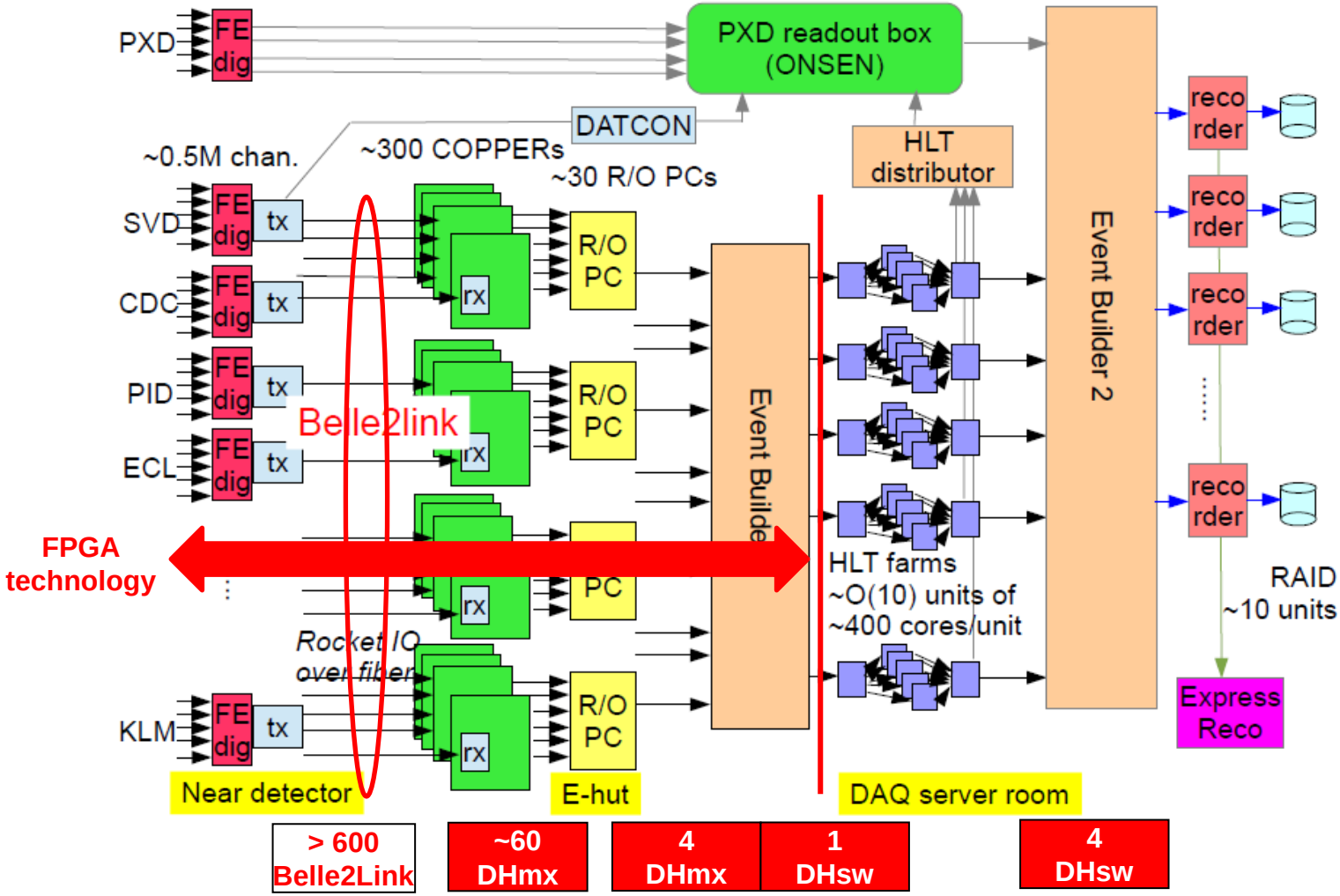
Belle 2 DAQ upgrade step 1



Belle 2 DAQ upgrade step 2



Belle 2 DAQ upgrade step 3



Proposal for DAQ upgrade

Goal :

- Offer a solution which can be evaluated now
- Proposal based on existing hardware developed for PXD detector and DAQ of COMPASS experiment
- Partial or complete upgrade before start of physics run in 2018

- Proposal was submitted in January 2016
- By now the proposal become outdated

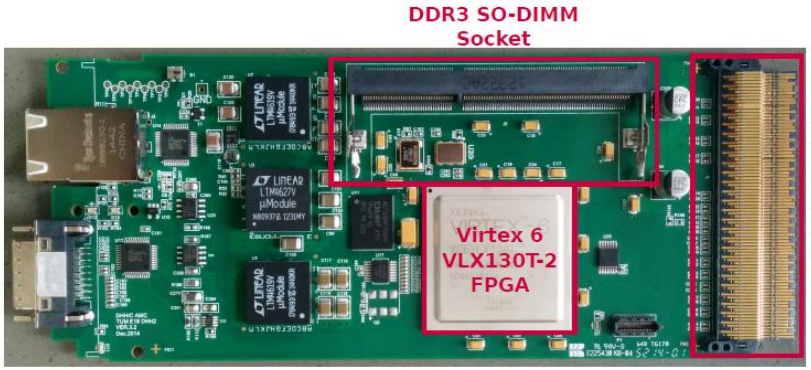
Solutions presented in this proposal are taken from our development of FPGA based DAQ for COMPASS experiment at CERN :

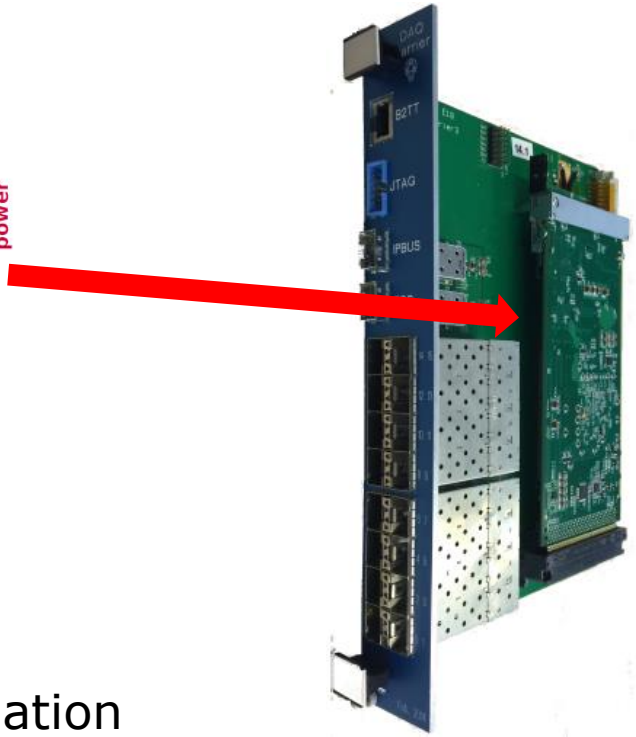
http://iopscience.iop.org/article/10.1088/1748-0221/11/02/C02025/pdf

Features of FPGA DAQ module

- Interfaces
  - Multiple high speed serial links for data transmission
  - Time distribution system B2TT
    - Real time DAQ management
      - Synchronization, Data flow control
      - Recovery/resynchronization
  - Ethernet (IPbus, very light UDP based protocol)
    - Configuration
    - Status, Errors, statistics for DAQ Run Control
- DDR memory for data buffering
  - Synchronization of data with different latency
  - avoiding congestions
  - averaging data rates
  - relaxing real time requirements for RO computers

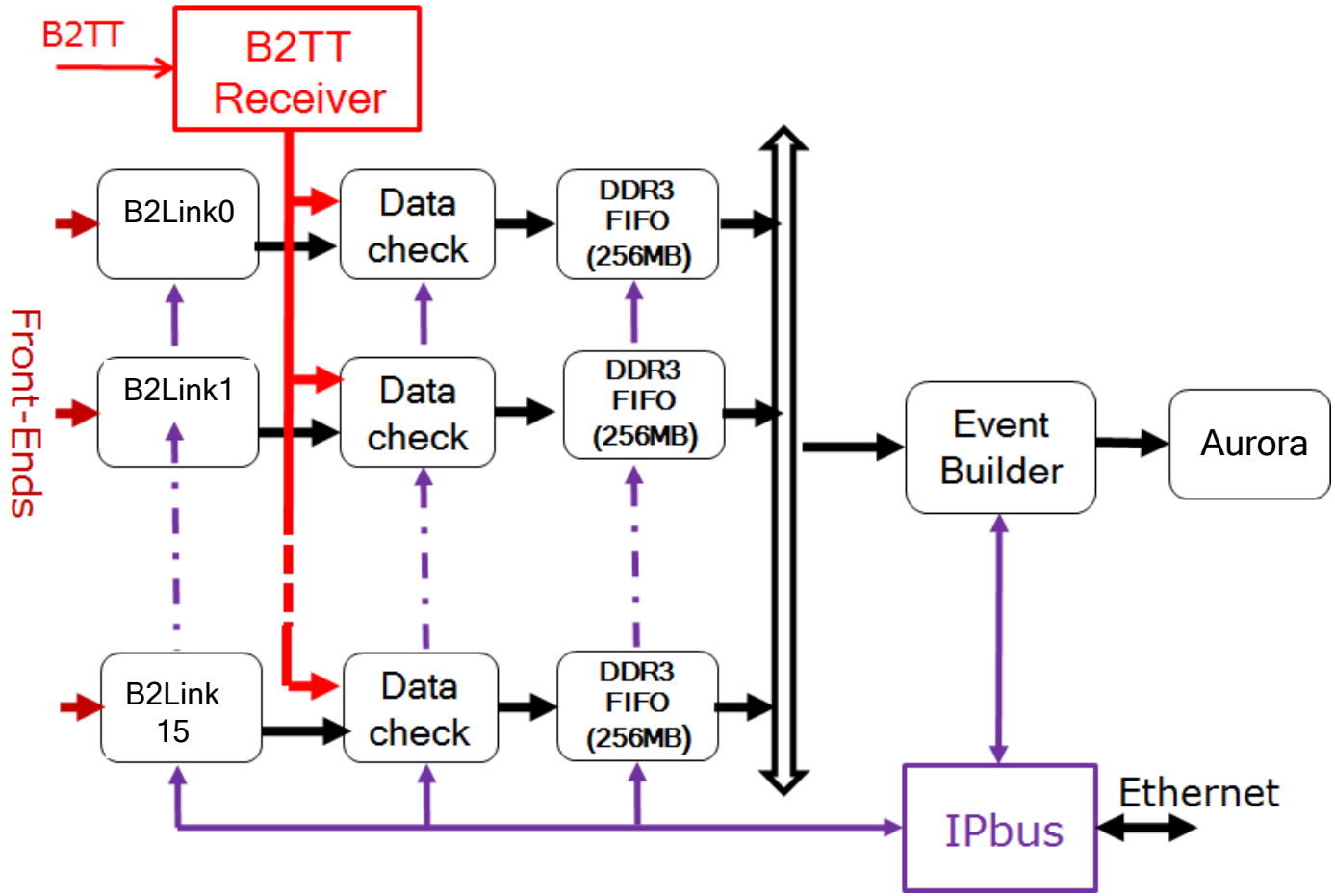
DAQ hardware modules

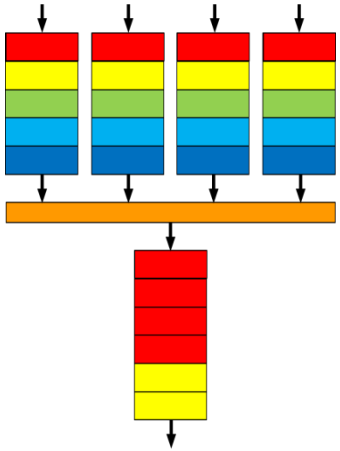




- DHmx
  - FPGA V6 VLX130T
  - 17 High speed links (17x6.5Gbps)
    - B2L, Aurora, IPBUS
  - DDR3 4GB, 3GB/s throughput
- DAQ Carrier Card for tests and evaluation
  - 16 SFP+
  - B2TT
  - JTAG
- DHpcie
  - Adapter for DHmx module
  - B2TT, Ipbus, QSFP

Multiplexer firmware functionality





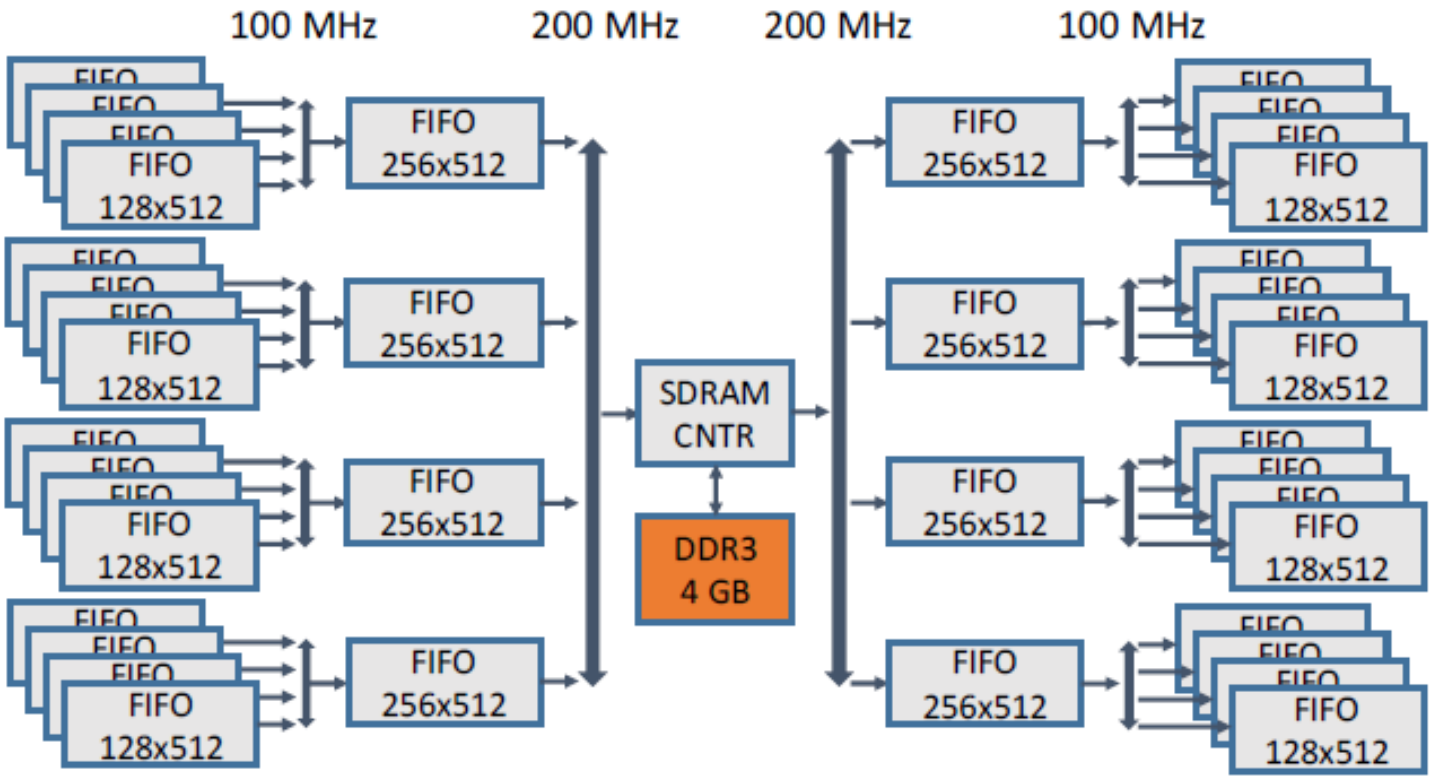
Data consistency check

- Data latency and time out
- Event format
- Event ID in data stream vs expected Event ID from B2TT
- Event size, maximum event size
- Maximum data rate
- CRC
- …

In case of error(s) event rejected and new event with error message generated instead => continuous data taking

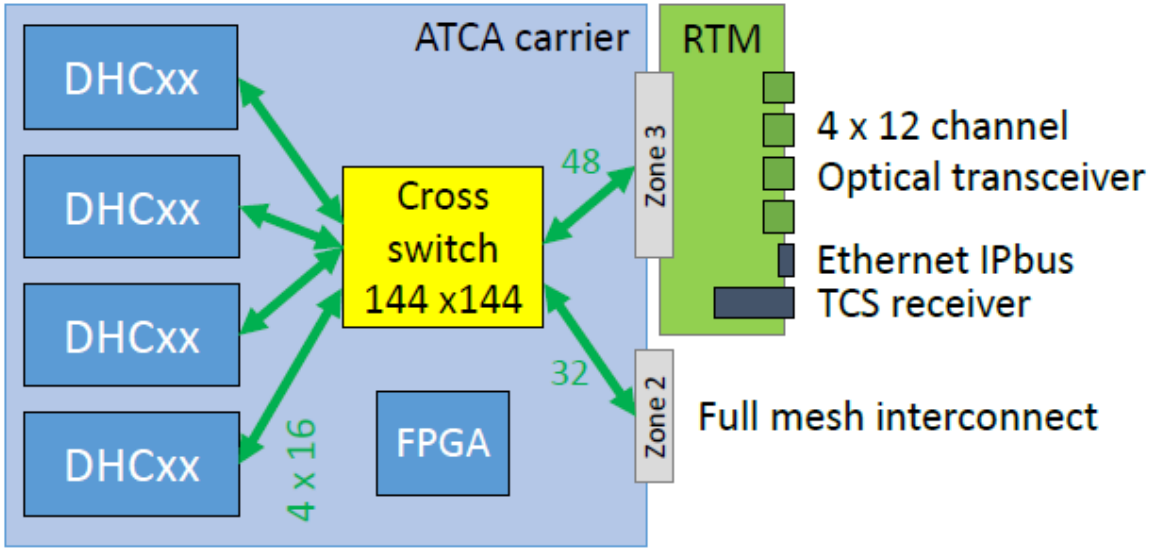
Run control reads status information and error messages via IPbus

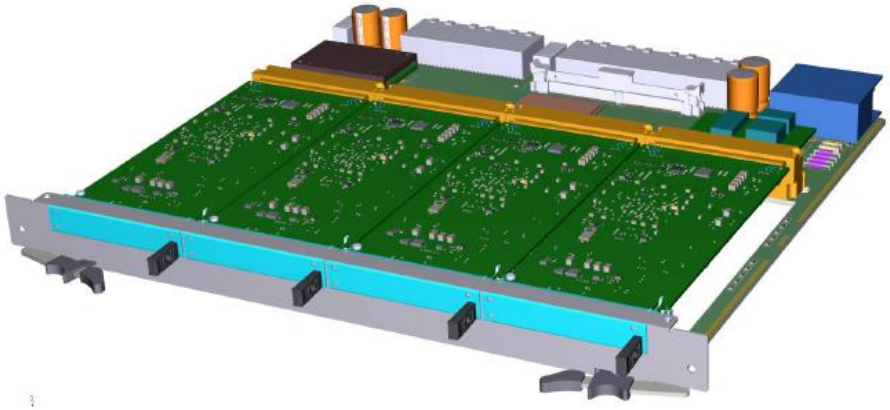
DDR3 memory controller



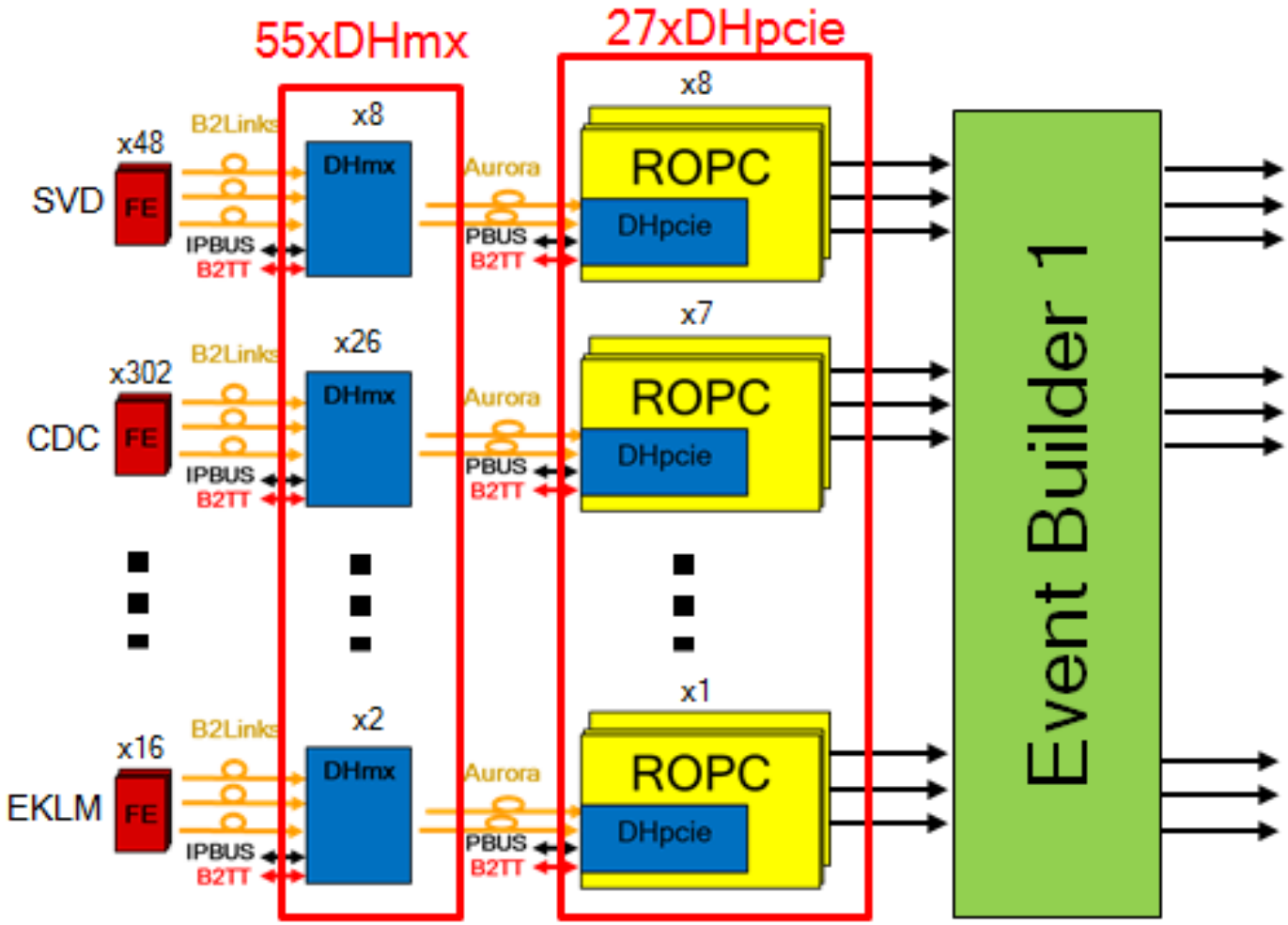
- 16 independent FIFO like memories blocks of 256 MB each
- 200 MB/s/port write performance
- 3 GB/s throughput

ATCA Carrier Card being developed for COMPASS





DAQ upgrade step 1



All DHmx modules fit in 14 ATCA cards

Cost estimate for step 1 DAQ upgrade

Number of DHxx modules

	#B2Links	#DHmx's	#DHpcie	#ROPC	MB/s/DHmx	MB/s
SVD	48	8	8	8	60	428
CDC	302	29	3	3	58	175
TOP	64	6	2	2	48	96
ARICH	90	8	2	2	45	84
ECL	52	5	5	5	72	360
BKLM	24	2	1	1	60	60
EKLM	16	2	1	1	41	42
TRG	19	2	1	1	-	-
Total	615	59	27	27	-	1245

HW Cost estimate for DAQ upgrade

	Number	Cost(kEuro)	Total(kEuro)
DHmx modules	59	1.2	70.8
DHcc modules	15	4	30
RTM	15	3	45
DHpcie	27	2	54
ATCA shelf	2	7	14
Total	-	-	213.8

DAQ features after upgrade

High reliability provided by:

- Automatic (re)synchronization of data streams
- Possibility to include and exclude any detector or subdetector during data taking
- Detecting and handling scrambled data
- Data throttling by Limiting maximum data rate on each B2Link

- Performance of single DHmx module
  - Defined by DDR3 memory throughput of 3GB/s
  - Peak data rate 15 x 200MB/s = 3GB/s
  - Maximum average rate defined by maximum outgoing link speed of 600MB/s

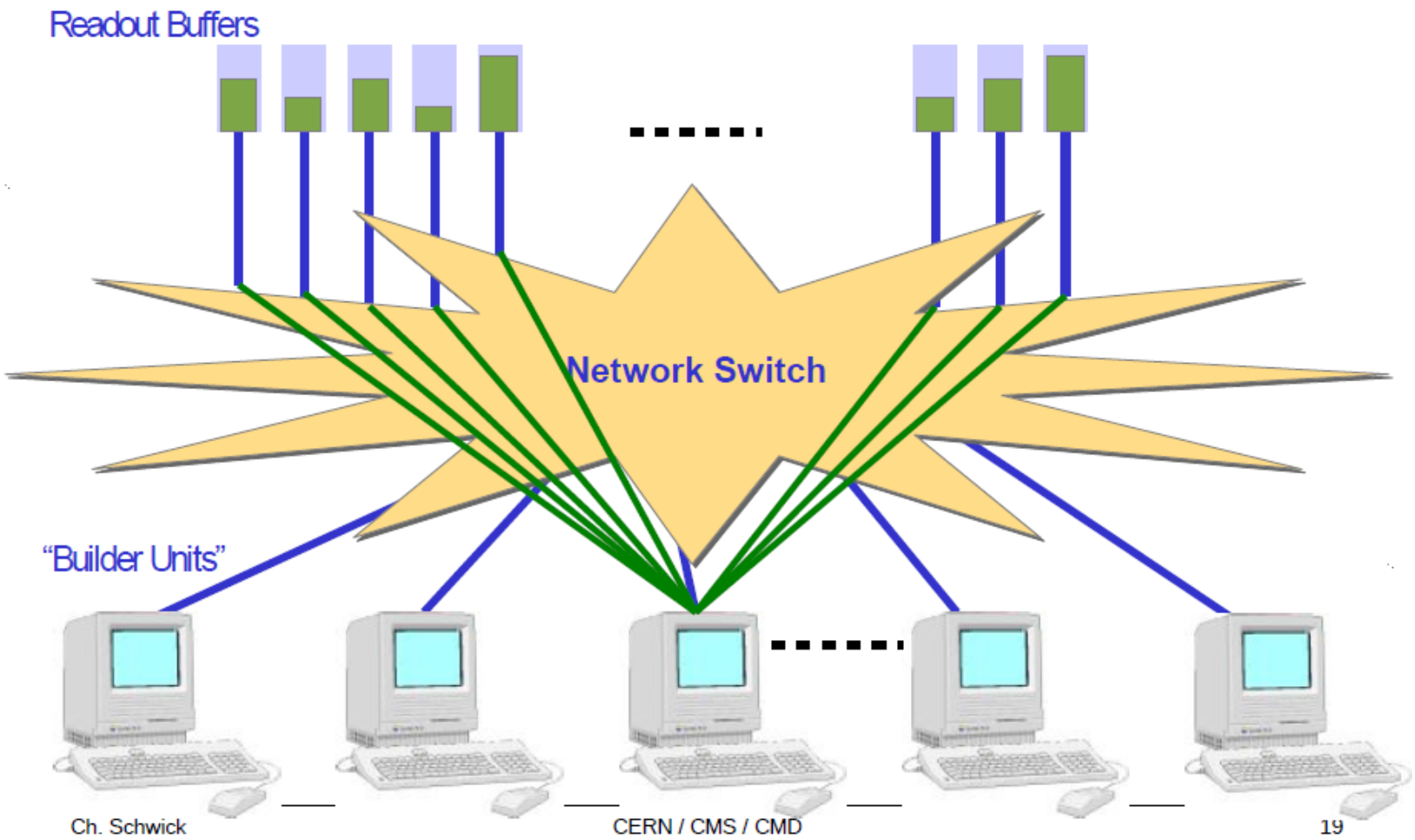
- Unification: DAQ performance allows to serve as multiple LOCAL RUN DAQs

Open issues

- How many B2Links can be implemented in single FPGA? If B2Link uses GTX without elastic buffer then number of links will be limited by BUFG and can not exceed 10
- Development of bridge between IPbus and B2Link for slow control

EVENT BUILDING in FPGA

Networking: EVB traffic

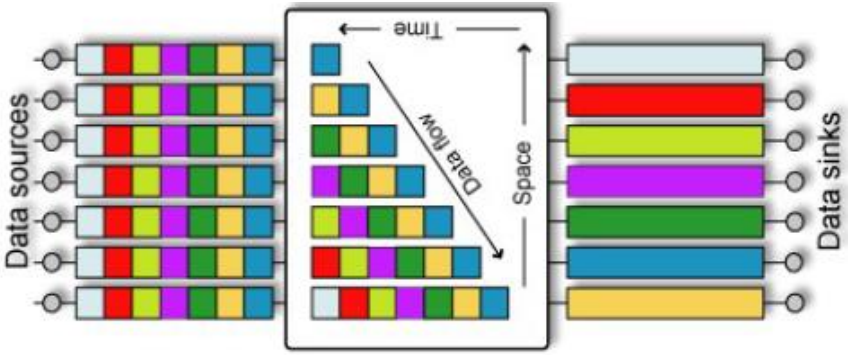


Event Building dilemma

For Event builder traffic pattern congestion is a problem...

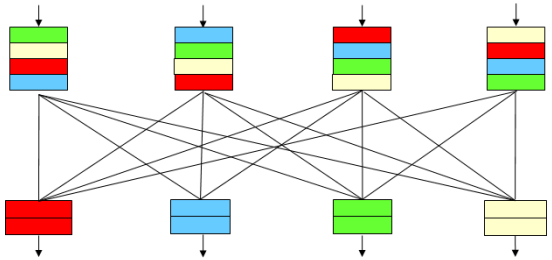
Network Switch : how to avoid congestion

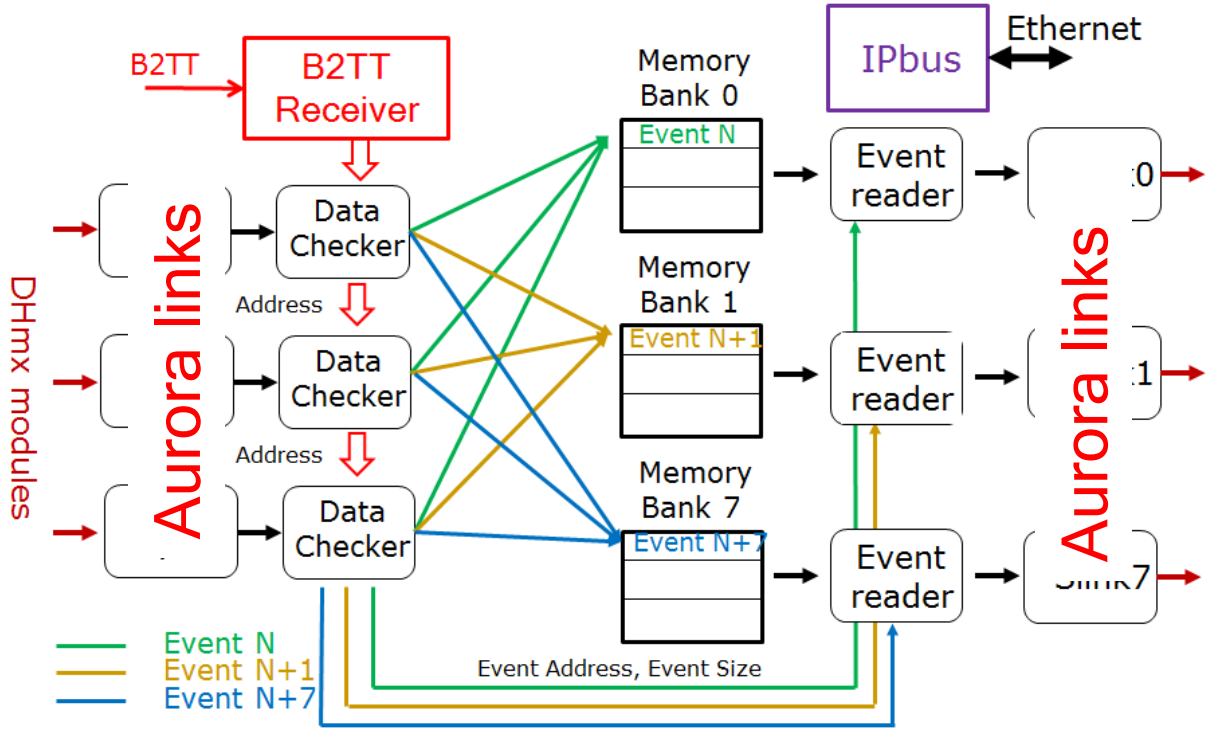
- Shape traffic



- Use expensive switch with sufficient memory
  - Automatic shaping of traffic

FPGA Switch 8x8(event builder)





- Events are processed simultaneously and buffered in DDR, no congestion
- Events distributed between outgoing links in round robin manner
- 2.5 GB/s throughput

- 4xDHmx + DHsw => Event builder 1

Summary

- FPGA technology provide low cost, reliable solutions for DAQ

Proposal for DAQ upgrade

- 60 DHmx modules + 27 DHpcie needed to substitute 300 COPPER modules
- Required investment of 220 kEuros
- New system performance would be sufficient for 10 years of Belle 2 operation
- The upgrade could provide simple , easy to handle and reliable DAQ upgrade
- Not enough time left to complete the project before start of run

Concluding remarks

- DAQ upgrade is needed it's only a question when it should be done
- From my point of view sooner is better for experiment
- DAQ architecture allows to split upgrade in few steps avoiding risk of failure
- Work on DAQ upgrade shall start as soon as possible in parallel with commissioning of current DAQ and without interference

THANK YOU