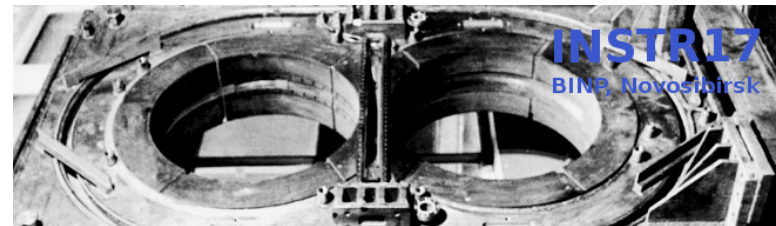


# Monitoring Complex Detectors: the uSOP approach in Belle II experiment

F. Di Capua

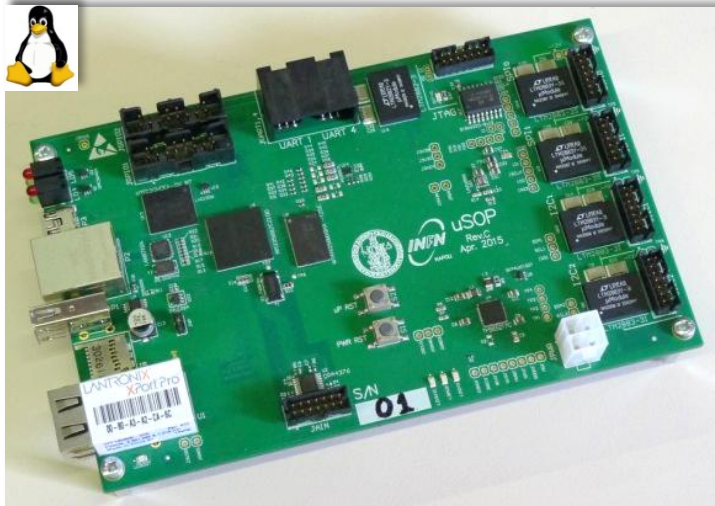
Dipartimento di Fisica, Univ. di Napoli Federico II and INFN

INSTR17, Novosibirsk 3/03/2017



# Overview

- uSOP: a Service-Oriented Platform for embedded applications
- Hardware
- Software
- uSOP at work: monitoring complex detectors
  - Belle2, Beast2 @ KEK
- Conclusions



The uSOP board

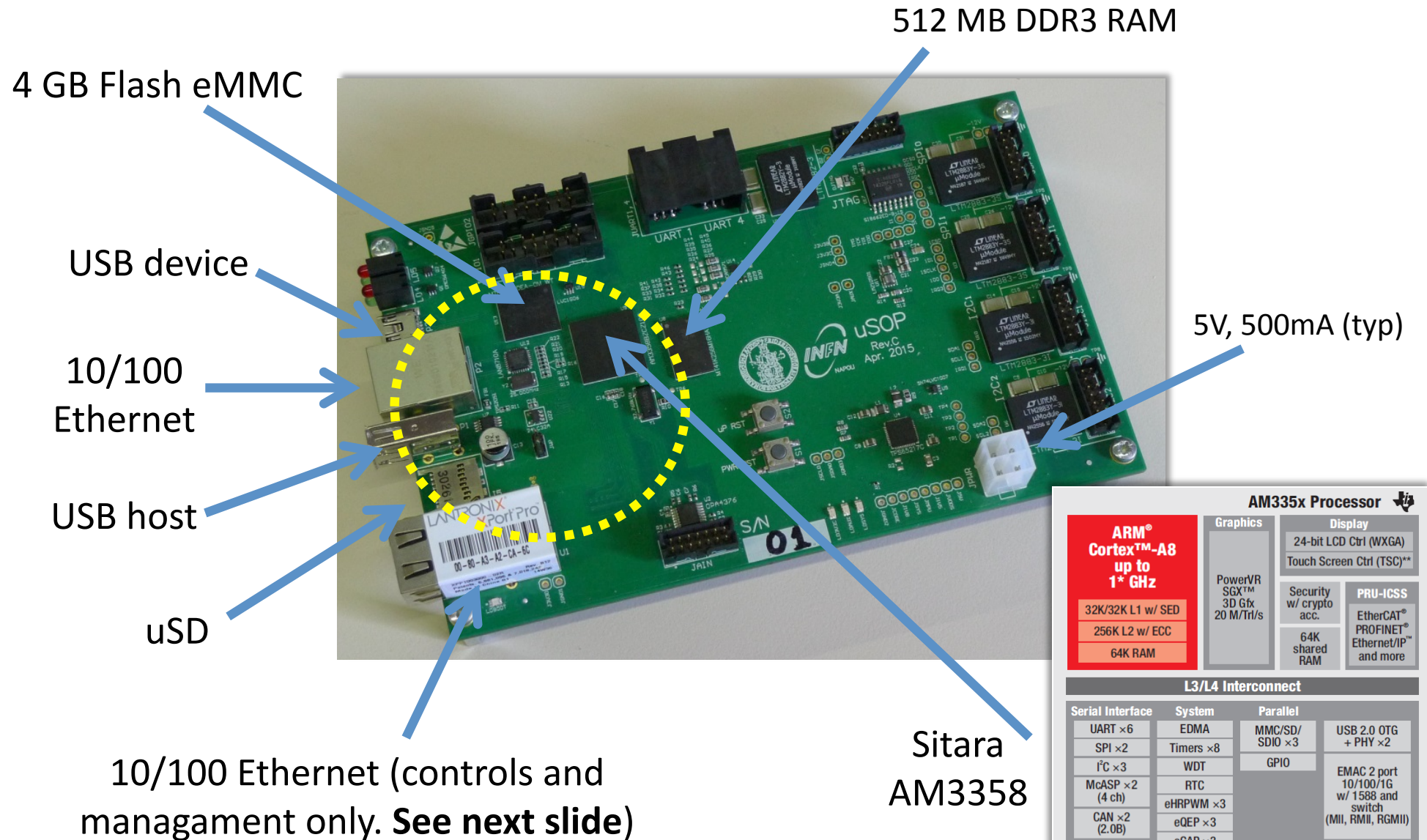
- Running Linux OS (Debian)
  - porting armv7l
- Full support for compilers and applications
- Kernels: major releases available
  - 3.x and 4.x

# uSOP

- uP- based, Service-Oriented Platform for embedded applications
- Strongly oriented to SPI, I2C, JTAG, UART, with isolated power for peripherals and sensors
- Fully managed remotely
- 3U Eurocard native form factor, expandable
- Derived-from and compatible-with BeagleBone Black open-source project

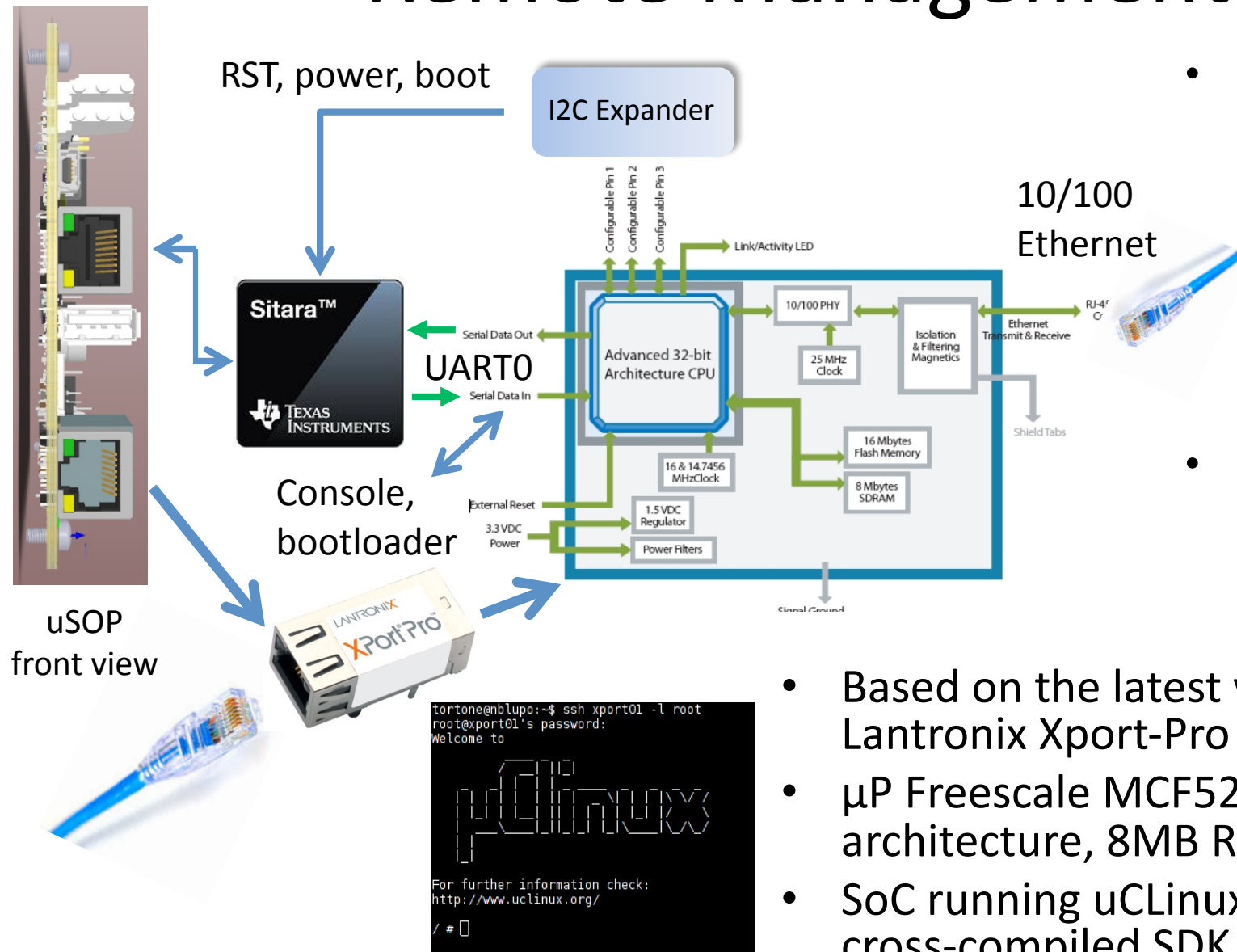


# uSOP – uP and utilities



AM335x Processor			
<b>ARM® Cortex™-A8</b> up to 1* GHz 32K/32K L1 w/ SED 256K L2 w/ ECC 64K RAM	<b>Graphics</b> PowerVR SGX™ 3D Gfx 20 M/Ti/s		<b>Display</b> 24-bit LCD Ctrl (WXGA) Touch Screen Ctrl (TSC)**
	Security w/ crypto acc. 64K shared RAM	<b>PRU-ICSS</b> EtherCAT® PROFINET® Ethernet/IP™ and more	
		<b>L3/L4 Interconnect</b>	
	<b>Serial Interface</b> UART ×6 SPI ×2 I²C ×3 McASP ×2 (4 ch) CAN ×2 (2.0B)	<b>System</b> EDMA Timers ×8 WDT RTC eHRPWM ×3 eQEP ×3 eCAP ×3 JTAG/ETB ADC (8 ch) 12-bit SAR**	<b>Parallel</b> MMC/SD/SDIO ×3 GPIO USB 2.0 OTG + PHY ×2 EMAC 2 port 10/100/1G w/ 1588 and switch (MII, RMII, RGMII) <b>Memory Interface</b> LPDDR1/DDR2/DDR3 NAND/NOR (16b ECC)

# Remote Management



- Remote control over IP for:
  - uP Reset
  - Boot mode
  - Power on/off
- UART over IP:
  - Console
  - Bootloader
- More tasks can be implemented (watchdog, controls, ...)

- Based on the latest version of Lantronix Xport-Pro
- $\mu$ P Freescale MCF5208, MMU-less architecture, 8MB RAM, 16MB Flash
- SoC running uCLinux with a full cross-compiled SDK



- Timers
- PWM
- Event Capture
- PRU

# uSOP – Peripherals/Intf

16 x GPIO

# TCK

## JTAG (\*)

**TDI**

## FPGA firmware download

2 x RS232 (\*)

2 x SPI (\*)

2 x 12C (\*)

4 x 12 bit AIN (\*\*)  
+ 2 on-board power monitoring

- = fully isolated, 5V-12V supply
- \*\* = buffered

# QuickEval compatibility

SPI and I2C busses are accessible via connectors compatible with the QuickEval specifications from Linear Technology allowing the developer to benefit from a large variety of high-performance evaluation boards

### QuickEval System

The QuickEval System is a USB-based product demonstration and data acquisition system for use with Linear Technology's ADCs, DACs, LED drivers, RF power detectors, PLL Synthesizers, IO-link transceivers, Power and Temperature Monitors, Intelligent Hot Swap Controllers, Battery Chargers and Managers, Coulomb Counters, Power over Ethernet Controllers and more. The system consists of a USB Acquisition Controller board that connects to individual daughter cards for Linear Technology products. The software also includes web links to the device data sheets and provides an automatic update feature to keep the current with the latest set of device drivers.

Use QuickEval software with the [DC590](#) or [DC2026](#) Controller boards

### Temperature Monitoring

#### LTC2983 Software

The [LTC2983](#) demo software is designed to help configure, program and LTC2983. It can configure the LTC2983, save the configuration, check for configuration errors, run the conversion results into a text file, and create Arduino-ready C code based on the configuration. The software can be used in conjunction with the DC2209 demo circuit.

#### LTC2984 Software

The [LTC2984](#) demo software is designed to help configure, program and

- [Download QuickEval](#)
- [DC590 Evaluation Kit](#)
- [DC2026 Evaluation Kit](#)
- [View All Demo Boards Using QuickEval Software](#)

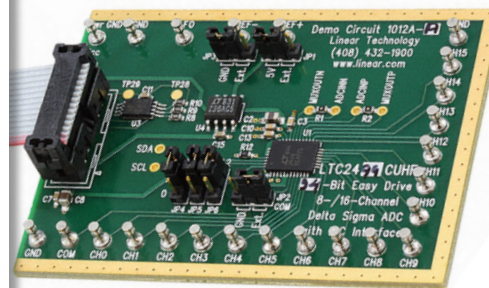
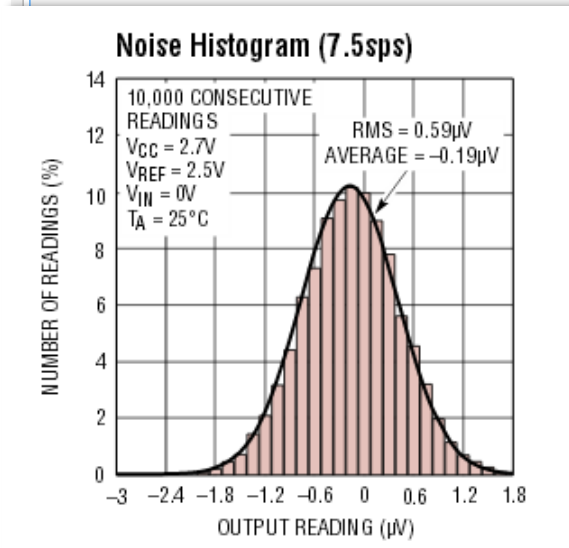
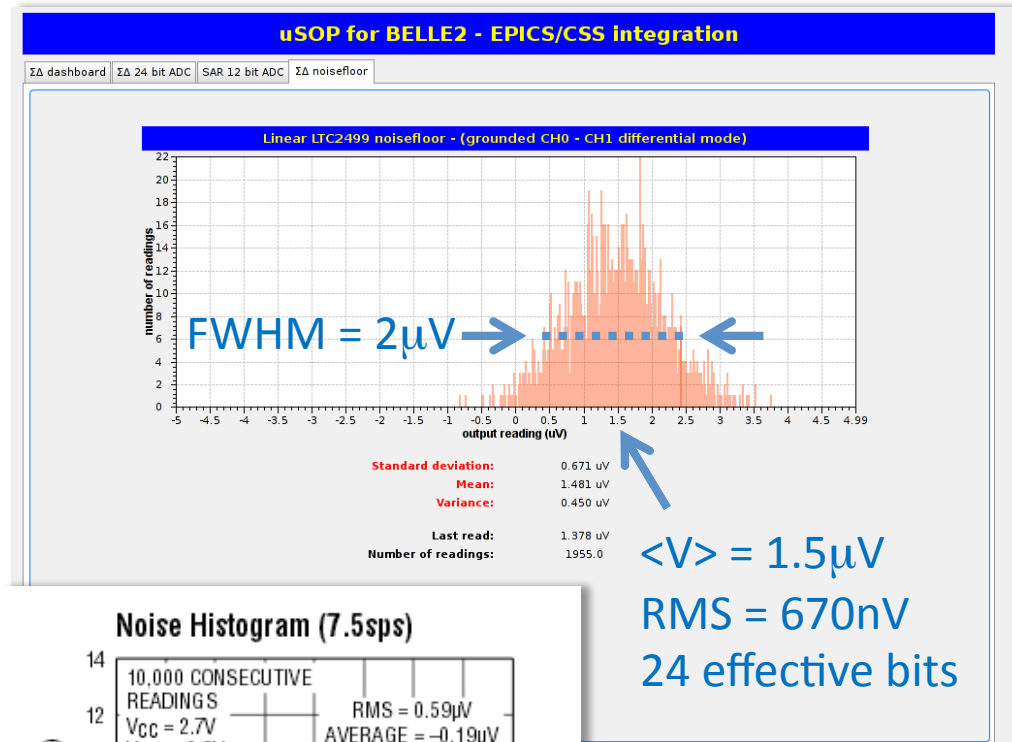
**Demo Boards matching your search.**

Demo Board #	Description	Product Page	Companion Board	Software
<a href="#">DC1009A-A</a>	LTC2492 24-bit, 2-ch ADC, req. DC590	<a href="#">LTC2492</a>	<a href="#">DC590B</a>	<a href="#">QuickEval System</a>
<a href="#">DC1009A-B</a>	LTC2488 16-bit 2-ch ADC, req DC590	<a href="#">LTC2488</a>	<a href="#">DC590B</a>	<a href="#">QuickEval System</a>
<a href="#">DC1009A-C</a>	LTC2486 16-bit 2-ch ADC with Temp Sensor, PGA, req DC590	<a href="#">LTC2486</a>	<a href="#">DC590B</a>	<a href="#">QuickEval System</a>
<a href="#">DC1010A-A</a>	LTC2493 24-Bit 4/2-ch I2C Delta Sigma ADC (Req. DC590)	<a href="#">LTC2493</a>	<a href="#">DC590B</a>	<a href="#">QuickEval System</a>
<a href="#">DC1010A-B</a>	LTC2489 16-Bit 4/2-ch I2C Easy Drive Delta Sigma ADC (req DC590B)	<a href="#">LTC2489</a>	<a href="#">DC590B</a>	<a href="#">QuickEval System</a>
<a href="#">DC1010A-C</a>	LTC2487 16-bit 4/2-ch I2C Easy Drive ADC (req DC590B)	<a href="#">LTC2487</a>	<a href="#">DC590B</a>	<a href="#">QuickEval System</a>
<a href="#">DC1011A-A</a>	LTC2498 Demo Board   24-bit, 8-ch ADC, req. DC2026	<a href="#">LTC2498</a>	<a href="#">DC2026C</a>	<a href="#">Linduino QuickEval System</a>

[MYLINEAR LOGIN](#)[CART](#)[SHARE](#)

# $\Delta\Sigma$ ADC – LTC2499 noise floor

- uSOP bench test with LTC2499:
  - $\Delta\Sigma$  ADC, 24 bit
  - I<sup>2</sup>C, powered by uSOP isolated supply
  - $V_{in} = 0V$ , Input shorted to local ground
  - ~5 Hz sampling rate
  - 50 Hz filter
  - $V_{ref}$ : 5V
  - Read-out by EPICS IOC
  - GUI by CSS/BOY



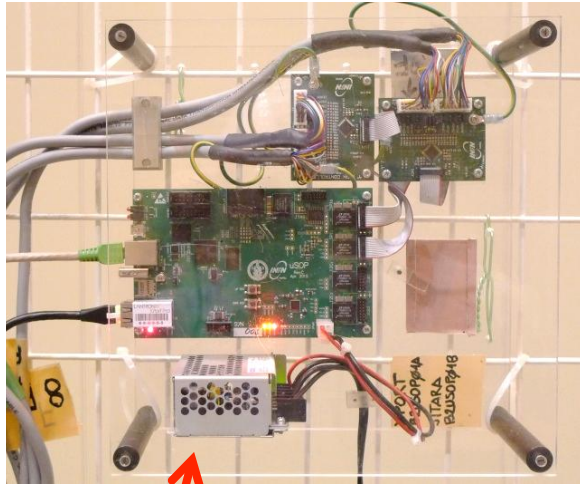
Source: linear.com



# **MONITORING COMPLEX DETECTORS**

# The Belle2 EndCap ECL\* monitoring system

uSOP box



EndCap Sectors 7F and 8F



- Minimal, stand-alone monitoring system at the EndCap ECL test station
- 4 sectors over 32 monitored to control the conditioning system (T, Rh)
- Up-time  $\approx$  2 year
- Data available via both EPICS and cloud

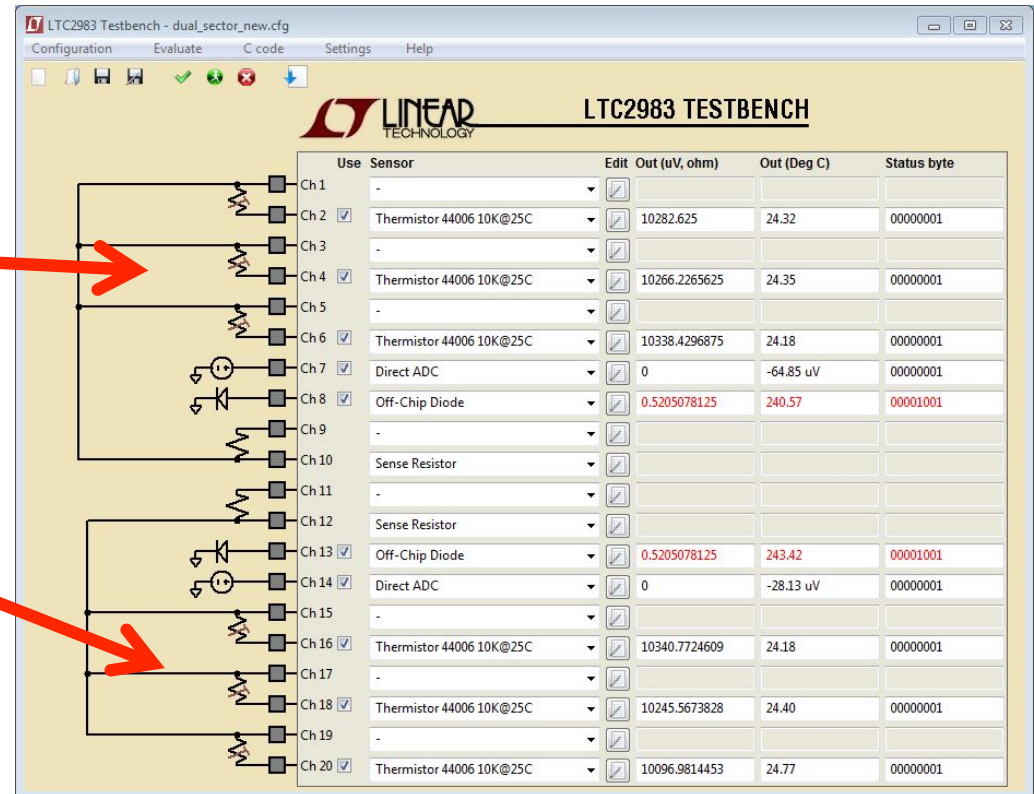
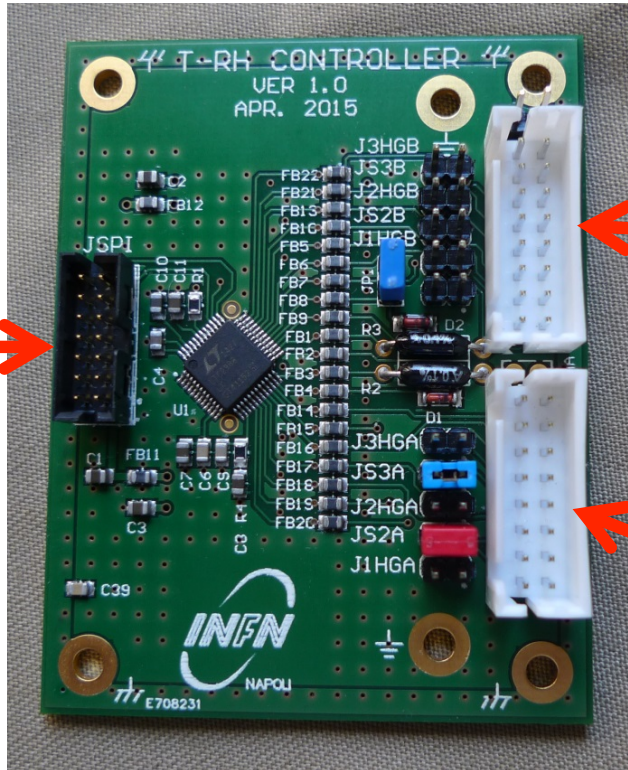


Belle2 EndCap Test Station at Fuji Exp. Hall, KEK

\*ECL talk from C. Cecchi on Wed

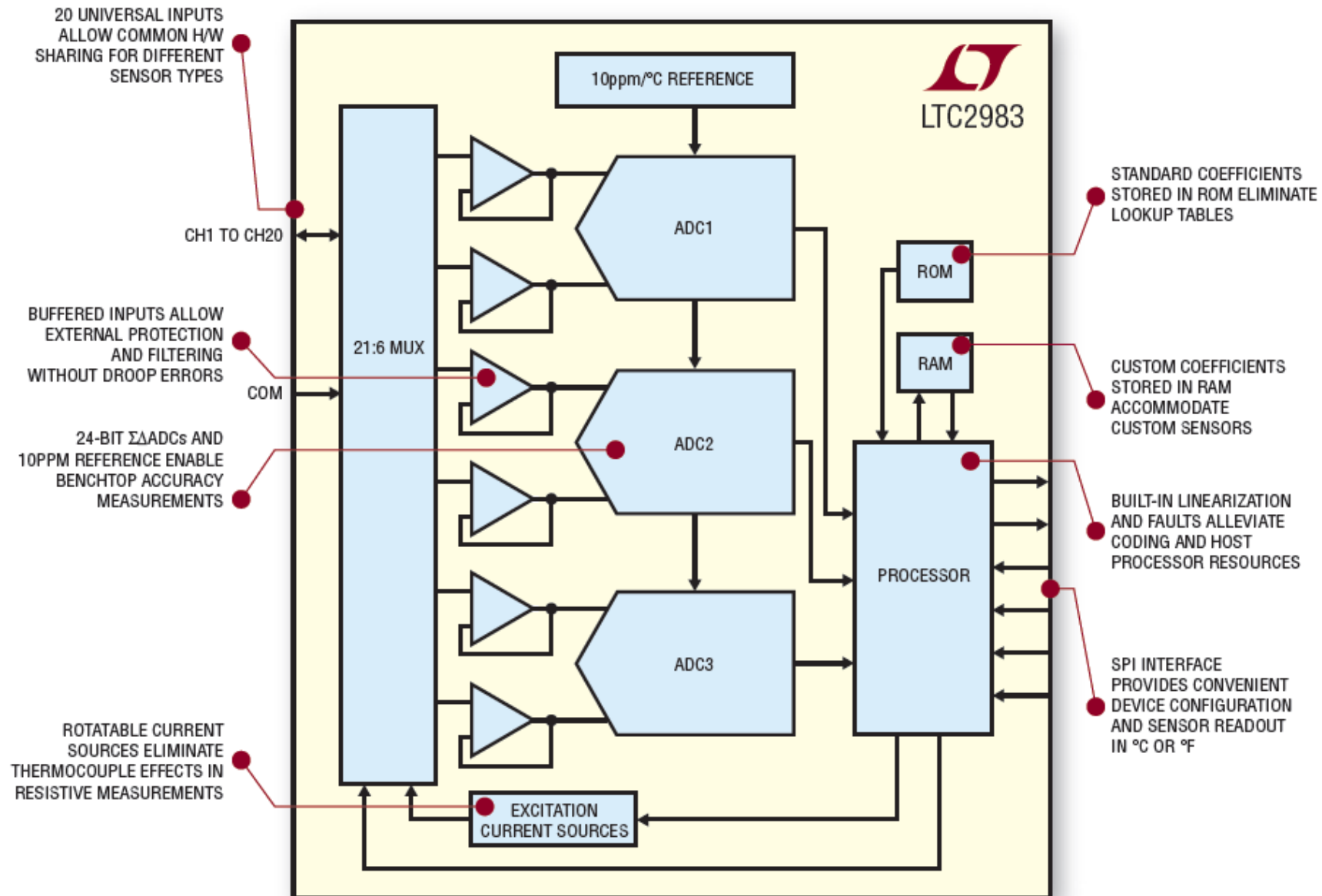
# The T-Rh Controller board (LTC2983)

To uSOP (via SPI)



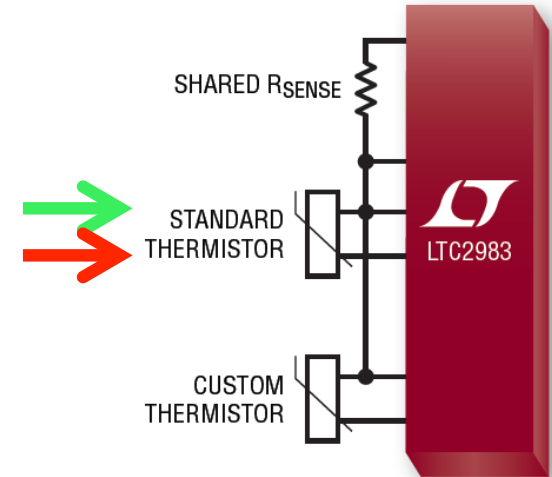
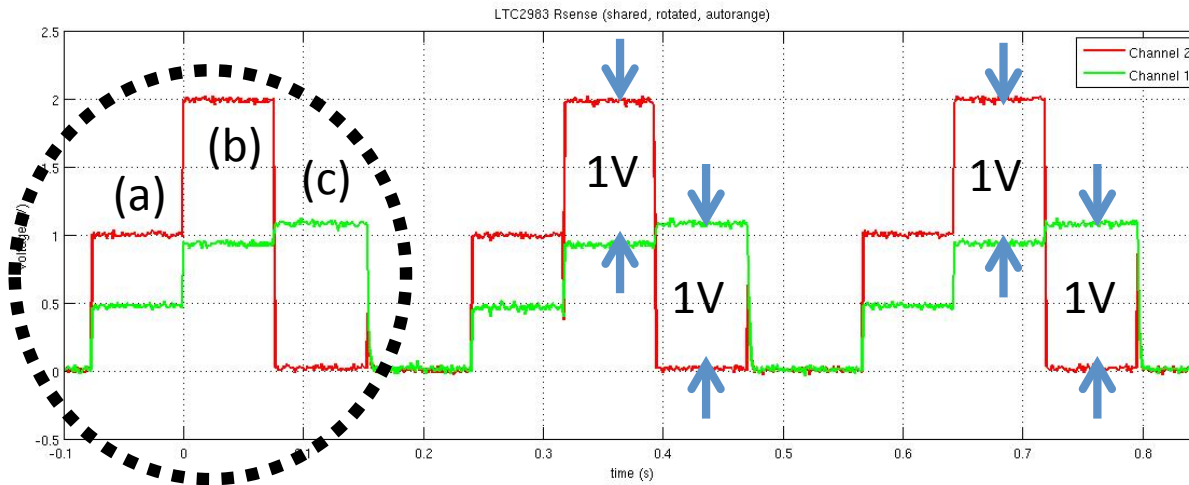
- Dual channel architecture, custom designed for the endcap readout
- each controller reads out two forward sectors (3x T, 1x Rh probes powered by uSOP) with galvanic isolation

# T-Rh Controller



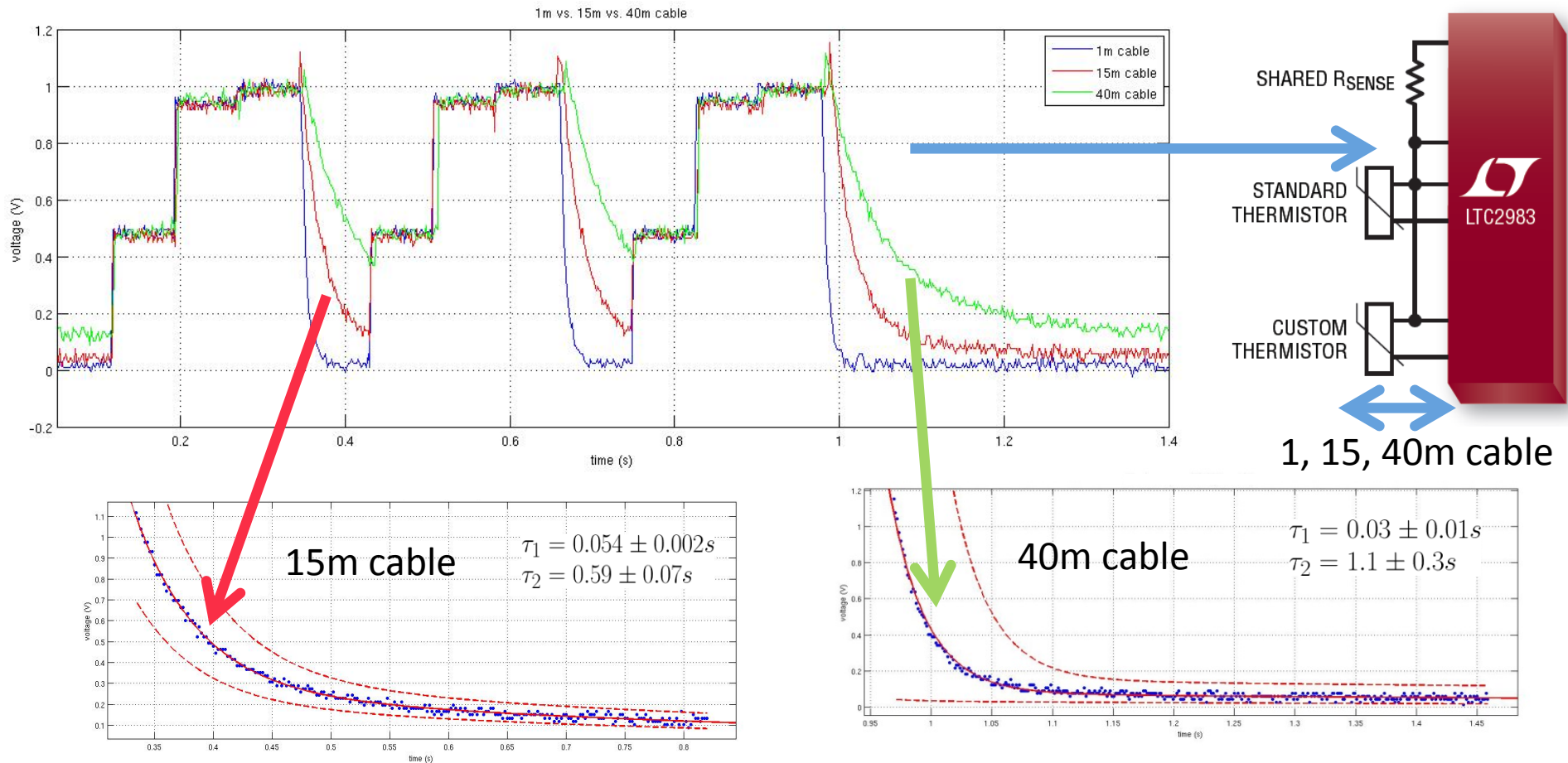


# Cycles



- We have programmed the on-chip uP to perform a 3-cycle measurement and processing :
  - (a) Inject current in Rsense and probe  $\Delta V$  across thermistor
  - (b) Set the current to obtain  $\Delta V \sim 1V$  (best ADC performance, low self-heating)
  - (c) Invert  $\Delta V$  polarity and take a second measurement, to cancel parasitic thermocouple effect by averaging

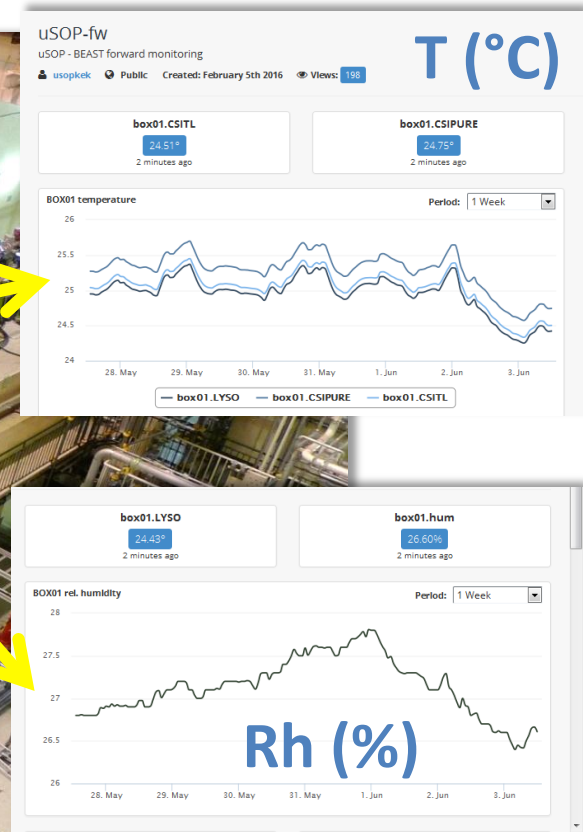
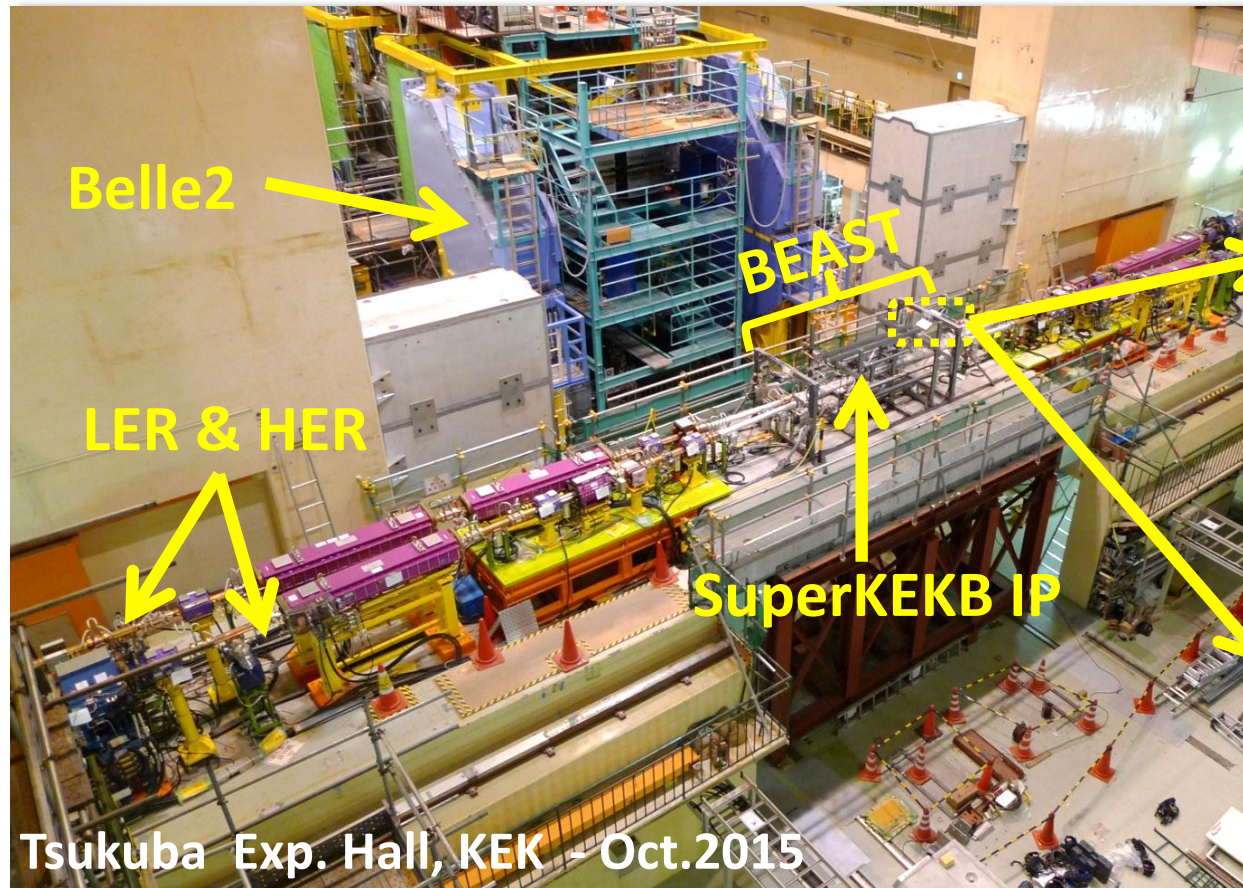
# Signal Integrity



- 3 Hz read out speed achievable with good signal integrity up to 40m cable length
- Double exponential decays: full discharge in  $O(1s)$

# uSOP @ BEAST

Beebotte Dashboard



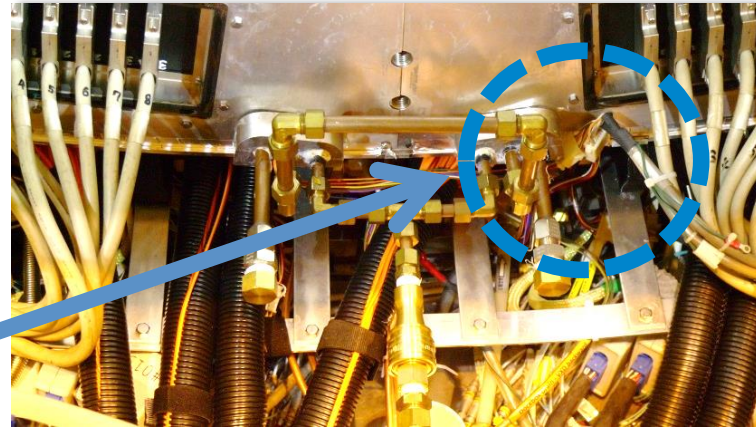
- BEAST2 (phase 1) is a detector that has taken data at SuperKEKB Interaction Point, to study beam background (see [P. Lewiss talk](#))
- uSOP has been used to monitor T and Rh of the 18 BEAST2 crystals (LYSO, CsI, CsI(Tl)). Data available via EPICS and cloud display (Beebotte)
- uSOP used also to monitor upset in FPGA exposed to beam background (see [R. Giordano talk](#))



uSOP minicrate for BEAST



# ECL backward installation



Monitor cables

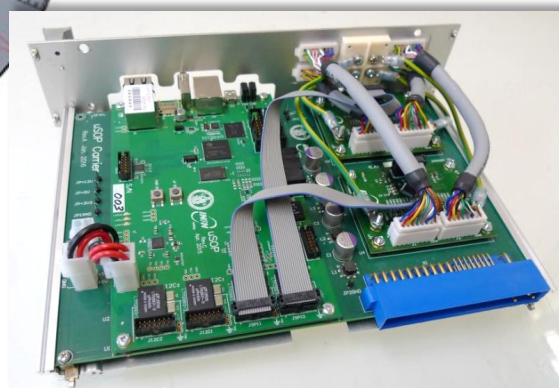
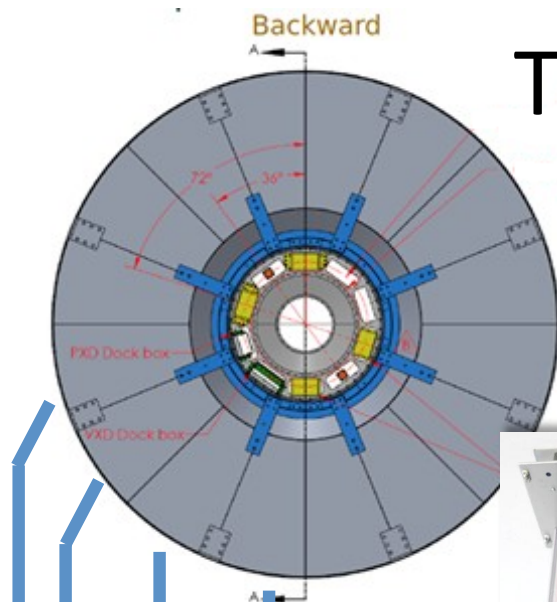
- ECL backward installed in January 2017
- uSOP monitoring connected



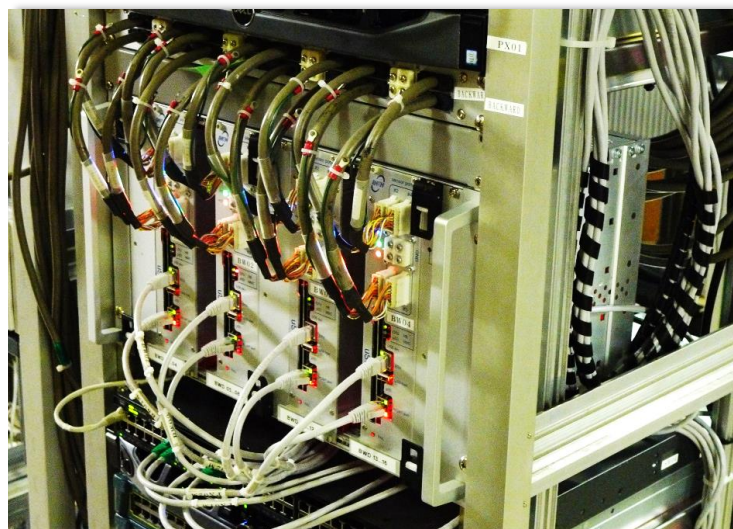


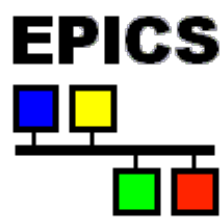
# The ECL EndCap monitoring system

- The final monitoring system has been installed at KEK during 2016
- Forward and Backward ECL:
  - 2112 CsI(Tl) crystals, 32 sectors
  - T and Rh monitor, 128 analog channels (96 thermistors + 32 Rh probes)
- Features:
  - 3-wire read-out to cancel the 40m cable stray resistance
  - Stray thermocouple effects cancellation
  - 4 uSOP boards, 8 T controllers with 24 bit ADCs for each endcap
  - 6U, 12HP form factor, shielded
  - Selective ground scheme to avoid loops
  - Read-out and controls via network



uSOP board wiring scheme

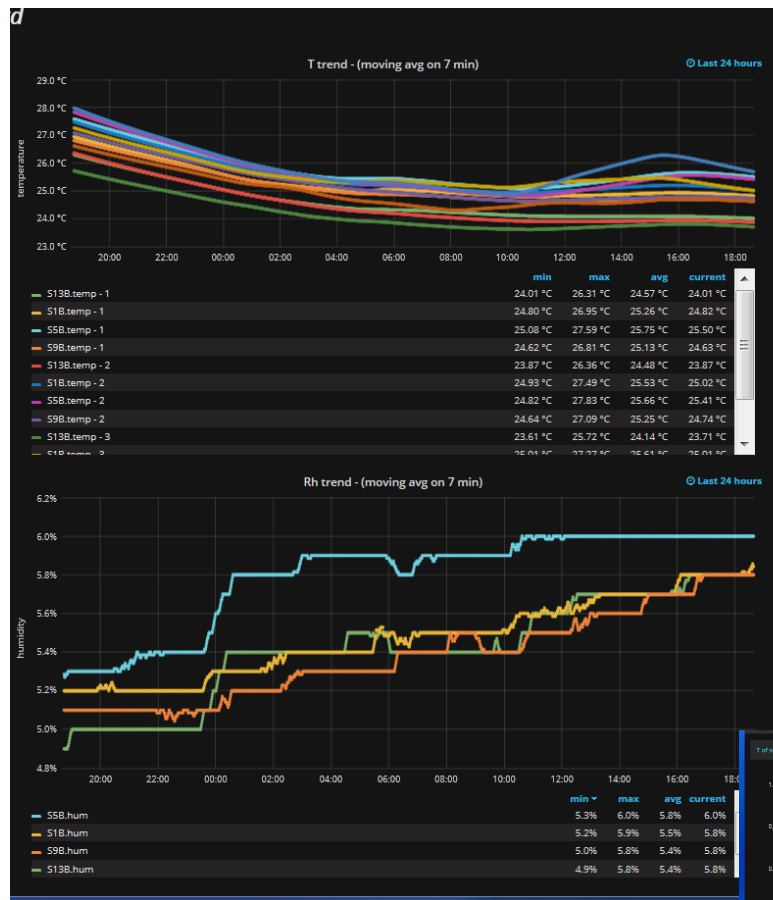




# Experimental Physics and Industrial Control System

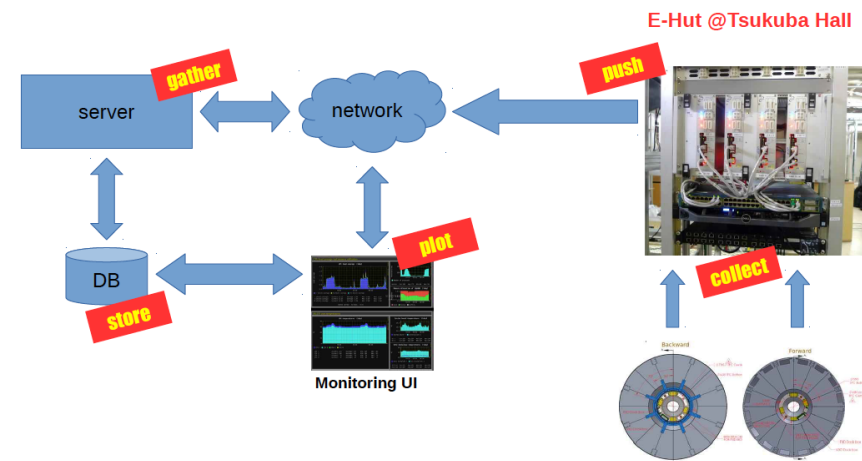
- EPICS (<http://www.aps.anl.gov/epics/>) is a set of Open Source software tools, libraries and applications developed collaboratively and used worldwide to create distributed soft real-time control systems for scientific instruments such as a particle accelerators, telescopes and other large scientific experiments.
  - On uSOP:
    - Straightforward compilation on ARM
    - Variety of EPICS extensions available on board:
      - ALH (ALarm Handler)
      - PV gateway
      - Asyn
      - StreamDevice
      - Autosave
    - IOCs for:
      - Linear LTC2499 (I2C)
      - Linear LTC2983 (SPI )
      - Sitara ADC (parallel)

# Displaying variables



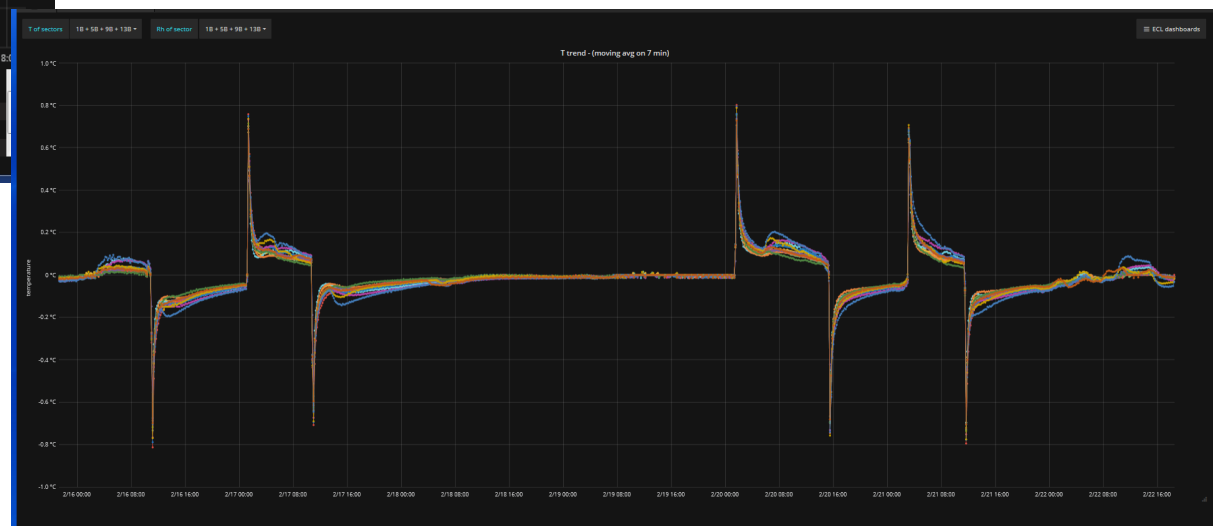
T

## Data publishing architecture



Rh

## Grafana metrics dashboards fist derivative over one week



# Conclusions

- uSOP has been intensively tested at KEK, starting from Apr. 2015
- Stable and reliable LINUX platform, with uptime  $\approx$  2 years
- Hardware controllers for all most common serial busses
- Fully (re)configurable and managed remotely (from brick to fully functional)
- Designed to work as a stand-alone unit, yet easy to deploy in complex control infrastructures
- EPICS compliant, IOCs developed for all the needed DAQ units





# BACKUP

# Cortex A Cores (32bit)

Cortex-A (32-bit)	ARMv7-A	Cortex-A5 <sup>[23]</sup>	Application profile, ARM / Thumb / Thumb-2 / DSP / SIMD / Optional VFPv4-D16 FPU / Optional NEON / Jazelle RCT and DBX, 1–4 cores / optional MPCore, snoop control unit (SCU), generic interrupt controller (GIC), accelerator coherence port (ACP)	4-64 KB / 4-64 KB L1, MMU + TrustZone	1.57 DMIPS/MHz per core
		Cortex-A7 <sup>[24]</sup>	Application profile, ARM / Thumb / Thumb-2 / DSP / VFPv4-D16 FPU / NEON / Jazelle RCT and DBX / Hardware virtualization, in-order execution, <a href="#">superscalar</a> , 1–4 SMP cores, MPCore, Large Physical Address Extensions (LPAE), snoop control unit (SCU), generic interrupt controller (GIC), ACP, architecture and feature set are identical to A15, 8-10 stage pipeline, low-power design <sup>[25]</sup>	8-64 KB / 8-64 KB L1, 0–1 MB L2, MMU + TrustZone	1.9 DMIPS/MHz per core
		Cortex-A8 <sup>[26]</sup>	Application profile, ARM / Thumb / Thumb-2 / VFPv3 FPU / NEON / Jazelle RCT and DAC, 13-stage <a href="#">superscalar</a> pipeline	16-32 KB / 16–32 KB L1, 0–1 MB L2 opt ECC, MMU + TrustZone	Up to 2000 (2.0 DMIPS/MHz in speed from 600 MHz to greater than 1 GHz)
		Cortex-A9 <sup>[27]</sup>	Application profile, ARM / Thumb / Thumb-2 / DSP / Optional VFPv3 FPU / Optional NEON / Jazelle RCT and DBX, <a href="#">out-of-order speculative issue superscalar</a> , 1–4 SMP cores, MPCore, snoop control unit (SCU), generic interrupt controller (GIC), accelerator coherence port (ACP)	16–64 KB / 16–64 KB L1, 0–8 MB L2 opt parity, MMU + TrustZone	2.5 DMIPS/MHz per core, 10,000 DMIPS @ 2 GHz on Performance Optimized TSMC 40G (dual-core)
		Cortex-A12 <sup>[28]</sup>	Application profile, ARM / Thumb-2 / DSP / VFPv4 FPU / NEON / Hardware virtualization, <a href="#">out-of-order speculative issue superscalar</a> , 1–4 SMP cores, Large Physical Address Extensions (LPAE), snoop control unit (SCU), generic interrupt controller (GIC), accelerator coherence port (ACP)	32-64 KB / 32 KB L1, 256 KB-8 MB L2	3.0 DMIPS/MHz per core
		Cortex-A15 <sup>[29]</sup>	Application profile, ARM / Thumb / Thumb-2 / DSP / VFPv4 FPU / NEON / integer divide / fused MAC / Jazelle RCT / hardware virtualization, <a href="#">out-of-order speculative issue superscalar</a> , 1–4 SMP cores, MPCore, Large Physical Address Extensions (LPAE), snoop control unit (SCU), generic interrupt controller (GIC), ACP, 15-24 stage pipeline <sup>[25]</sup>	32 KB w/parity / 32 KB w/ECC L1, 0–4 MB L2, L2 has ECC, MMU + TrustZone	At least 3.5 DMIPS/MHz per core (up to 4.01 DMIPS/MHz depending on implementation) <sup>[30]</sup>
		Cortex-A17	Application profile, ARM / Thumb / Thumb-2 / DSP / VFPv4 FPU / NEON / integer divide / fused MAC / Jazelle RCT / hardware virtualization, <a href="#">out-of-order speculative issue superscalar</a> , 1–4 SMP cores, MPCore, Large Physical Address Extensions (LPAE), snoop control unit (SCU), generic interrupt controller (GIC), ACP	MMU + TrustZone	?
	ARMv8-A	Cortex-A32 <sup>[31]</sup>	Application profile, AArch32, NEON advanced SIMD	8-64 KB w/optional parity / 8-64 KB w/optional ECC L1 per core, 128 KB-1 MB L2 w/optional ECC shared	

# Beaglebone Black

## BeagleBone Black Development Board

(ACTIVE) BEAGLEBK



Description & Features



Technical Documents



Support & Community



Order Now

### Key Document



• [BeagleBone Black Quick-Start Guide \(external link\)](#)

• [BeagleBone Black System Reference Manual \(external link\)](#)

» [View All Technical Documents \(6\)](#)

### Description

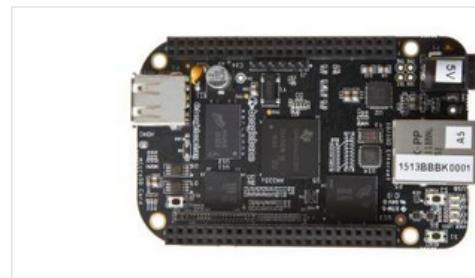
BeagleBone Black is a low-cost, open source, community-supported development platform for ARM® Cortex™-A8 processor developers and hobbyists. Boot Linux in under 10-seconds and get started on Sitara™ AM335x ARM Cortex-A8 processor development in less than 5 minutes with just a single USB cable.

BeagleBone Black ships with the Debian GNU/Linux™ in onboard FLASH to start evaluation and development. Many other Linux distributions and operating systems are also supported on BeagleBone Black including:

- Ubuntu
- Android
- Fedora

BeagleBone Black's capabilities can be extended using plug-in boards called "capes" that can be plugged into BeagleBone Black's two 46-pin dual-row expansion headers. Capes are available for, VGA, LCD, motor control, prototyping, battery power and other functionality. [More information.](#)

[Visit the BeagleBone Black Support Community](#)



BeagleBone Black development board.

The screenshot shows the BeagleBoard.org website. The header includes the logo and navigation links: Start, Discover Boards, Learn, Explore, Collaborate, and a Google Custom Search bar. The main content area is titled "BeagleBone Black" and features a large image of the board on the left. To the right of the image, there is a section titled "What is BeagleBone Black?" which describes it as a low-cost, community-supported development platform. Below this, there are two columns of specifications: "Processor: AM335x 1GHz ARM® Cortex-A8" and "Connectivity". The "Processor" column lists: 512MB DDR3 RAM, 4GB 8-bit eMMC on-board flash storage, 3D graphics accelerator, NEON floating-point accelerator, and 2x PRU 32-bit microcontrollers. The "Connectivity" column lists: USB client for power & communications, USB host, Ethernet, HDMI, and 2x 46 pin headers. Below these, there is a "Software Compatibility" section listing: Debian, Android, Ubuntu, Cloud9 IDE on Node.js w/ BoneScript library, and plus much more. On the right side of the page, there is a yellow banner that says "Fork me on Upverter". At the bottom right, there is an orange "Purchase" button with a shopping cart icon and a dropdown menu labeled "Select a distributor to buy".



# AM5728



AM5728, AM5726  
SPRS953 – DECEMBER 2015

## AM572x Sitara™ Processors Silicon Revision 2.0

### 1 Device Overview

#### 1.1 Features

- For Silicon Revision 1.1 information, see [SPR915](#)
- ARM® Dual Cortex®-A15 Microprocessor Subsystem
- Up to 2 C66x™ Floating-Point VLIW DSP
  - Fully Object-Code Compatible With C67x™ and C64x+™
  - Up to Thirty-two 16 × 16-Bit Fixed-Point Multiplies per Cycle
- Up to 2.5MB of On-Chip L3 RAM
- Two DDR3/DDR3L Memory Interface (EMIF) Modules
  - Supports up to DDR3-1066
  - Up to 2GB Supported per EMIF
- Dual ARM® Cortex®-M4 co-processors
- IVA-HD Subsystem
- Display Subsystem
  - Full-HD Video (1920 × 1080p, 60 fps)
  - Multiple Video Input and Video Output
  - 2D and 3D Graphics
  - Display Controller With DMA Engine and up to Three Pipelines
  - HDMI™ Encoder: HDMI 1.4a and DVI 1.0 Compliant
- 2x Dual-Core Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS)
- 2D-Graphics Accelerator (BB2D) Subsystem
  - Vivante™ GC320 Core
- Video Processing Engine (VPE)
- Dual-Core PowerVR® SGX544™ 3D GPU
- Crypto Hardware Accelerators
  - AES, SHA, RNG, DES and 3DES
- Three Video Input Port (VIP) Modules
- General-Purpose Memory Controller (GPMC)
- Enhanced Direct Memory Access (EDMA) Controller
- 2-Port Gigabit Ethernet (GMAC)
- Sixteen 32-Bit General-Purpose Timers
- 32-Bit MPU Watchdog Timer
- Five Inter-Integrated Circuit (I²C) Ports
- HDQ™/1-Wire® Interface
- Ten Configurable UART/IrDA/CIR Modules
- Four Multichannel Serial Peripheral Interfaces (MCSPIs)
- Quad SPI Interface (QSPI)
- SATA Gen2 Interface
- Multichannel Audio Serial Port (MCASP)
- SuperSpeed USB 3.0 Dual-Role Device
- High-Speed USB 2.0 Dual-Role Device
- PCI-Express® 2.0 Subsystems With Two 5-Gbps Lanes
  - One 2-lane Gen2-Compliant Port
  - or Two 1-lane Gen2-Compliant Ports
- Dual Controller Area Network (DCAN) Modules
  - CAN 2.0B Protocol
- Up to 247 General-Purpose I/O (GPIO) Pins
- Power, Reset, and Clock Management
- On-Chip Debug With CTools Technology
- 28-nm CMOS Technology
- 23 mm × 23 mm, 0.8-mm Pitch, 760-Pin BGA (ABC)

ADVANCE INFORMATION

# Beagleboard X15

 **beagleboard.org**

[f](#) [t](#) [in](#) [You Tube](#) [g+](#)

Start ▾ Discover Boards ▾ Learn ▾ Explore ▾ Collaborate ▾

Google™ Custom Search

BeagleBoard.org > x15

## BeagleBoard-X15

Sign up below for notifications of availability and approved distributors to place orders. Check the [wiki](#) for the latest production update. If you need a board right away and don't care about FCC/CE compliance, you can get an early version of X15 as the processor module of the [AM5728 EVM](#).



### What is BeagleBoard-X15?

BeagleBoard-X15 is the top performing, mainline Linux enabled, power-users' dream board with a core tailored for every computing task and a highspeed interface for every connectivity need. Give your algorithms room to stretch!

Processor: **TI AM5728 2×1.5-GHz ARM® Cortex-A15**

- 2GB DDR3 RAM
- 4GB 8-bit eMMC on-board flash storage
- 2D/3D graphics and video accelerators (GPUs)
- 2×700-MHz C66 digital signal processors (DSPs)
- 2×ARM Cortex-M4 microcontrollers (MCUs)
- 4×32-bit programmable real-time units (PRUs)

### Connectivity

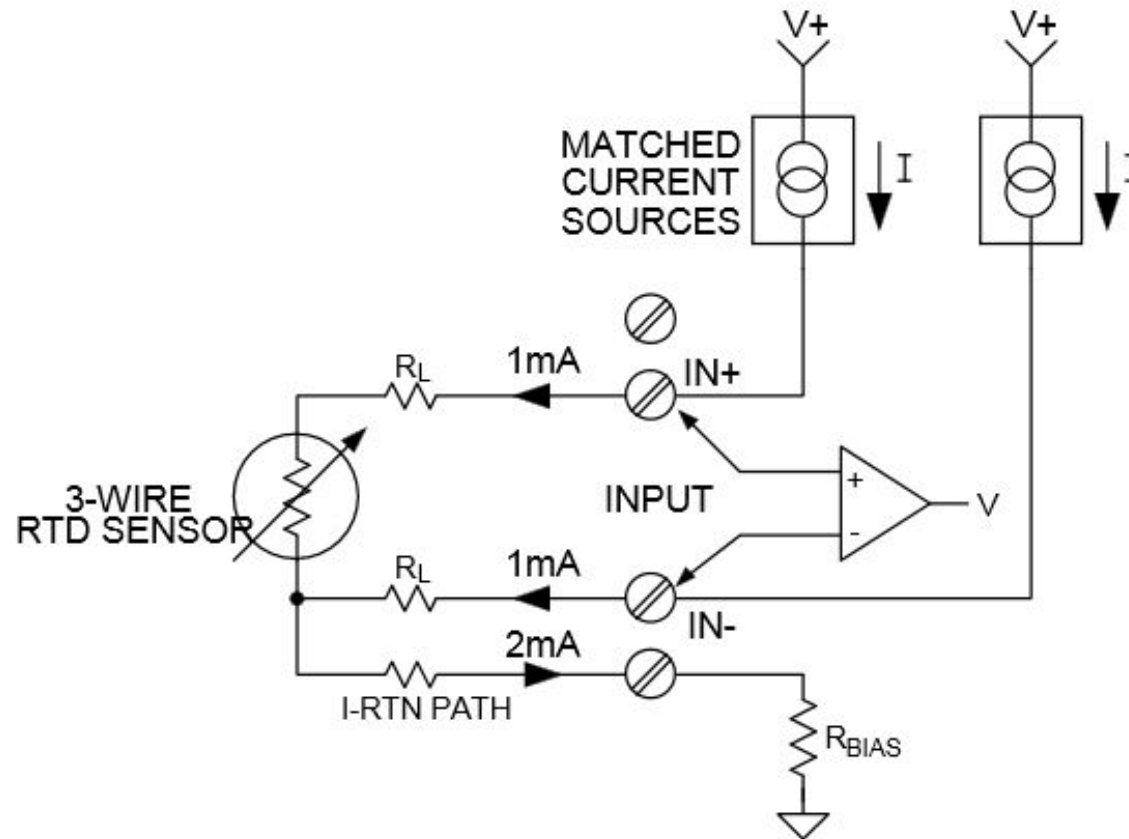
- 2×Gigabit Ethernet
- 3×SuperSpeed USB 3.0 host
- HighSpeed USB 2.0 client
- eSATA (500mA)
- full-size HDMI video output
- microSD card slot
- Stereo audio in and out
- 4×60-pin headers with PCIe, LCD, mSATA
- and much more...

### Software Compatibility

- Debian
- Android
- Ubuntu
- Cloud9 IDE on Node.js
- plus much more

### Register your interest

# 3-WIRE READOUT



3-WIRE SENSOR w/DUAL MATCHED CURRENT EXCITATION.  
CONVERTS WITH A SINGLE DIFFERENTIAL MEASUREMENT.  
ADSELF-COMPENSATES FOR MATCHED +/- LEAD  
RESISTANCES.