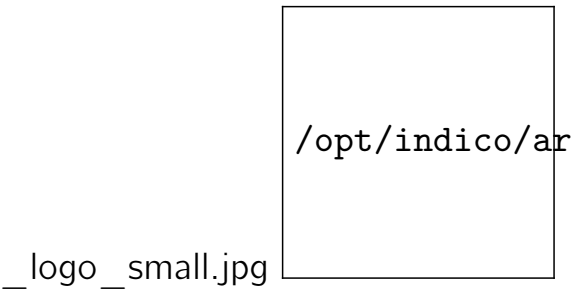

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The 32-channel TDC based on Altera Cyclone III FPGA.

Tuesday, 28 February 2017 17:00 (1:00)

Content

The number of read-out channels in modern experiments can reach very high values. This requires the use of electronics at a low cost per channel. Such result could be achieved through the use of widely available commercial electronic components. In this work we present newly developed TDC (Time-to-Digital Converter) block in the VME-32 standard. The 32-channel block is based on a single FPGA Altera Cyclone III chip. The block captures the events – rising and falling edges of input signal at a sample rate of 840 MHz. Maximum event rate is 210 MHz, until FIFO buffer for 512 events is not overflowed. Data from channel FIFO buffer is going to the shift register and then stored in shared memory, where it can be read on the VME bus. Main parameters of the TDC are: Resolution: 1.19 ns (1/840 MHz) Minimum time interval: 4.76 ns (1/210 MHz, 4 samples) Maximal time interval: 3440 ns (12 bit) It is supposed to use such TDCs in the developed Focusing Aerogel RICH for Super Charm-Tau Factory (BINP, Novosibirsk) and muon detectors read-out of TAIGA gamma-observatory (Tunka valley, Buryatia, Russia).

Summary

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