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Characterisation of novel prototypes of monolithic HV-CMOS pixel detectors for high energy physics experiments

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Content

An upgrade of the ATLAS experiment for the High Luminosity phase of LHC is planned for 2024 and foresees the replacement of the present Inner Detector with a new Inner Tracker completely made of silicon devices.

Depleted Monolithic Active Pixel Sensors (DMAPS) built with High Voltage CMOS (HV-CMOS) technology are investigated as an option to cover large areas in the outermost layers of the pixel detector and are especially interesting for the development of monolithic devices which will reduce the production costs and the material budget with respect to the present hybrid assemblies. For this purpose the H35Demo, a large area HV-CMOS demonstrator chip, was designed by KIT, IFAE and University of Liverpool, and produced in AMS 350 nm CMOS technology. It consists of four pixel matrices and additional test structures. Two of the matrices include both amplifiers and discriminator stages and are thus designed to be operated as monolithic detectors.

In these devices the signal is mainly produced by charge drift in a small depleted volume obtained increasing the bias voltage to the order of 100 V or more. Moreover, this technology allows to enclose the electronics in the same deep n-wells also used as collecting electrodes to enhance the radiation hardness of the chip.

In this contribution the characterisation of H35Demo chips and results of the very first test beam measurements of the monolithic matrices with high energetic pions at CERN SpS will be presented.

Summary

Primary author(s) : Dr. TERZO, Stefano (IFAE)

Co-author(s) : Dr. CASANOVA, Raimon (IFAE); Mr. PUIGDENGOLLES, Carles (IFAE); Mr. FOERSTER, Fabian (IFAE); Dr. LANGE, Joern (IFAE); Dr. GRINSTEIN, Sebastian (IFAE); Mr. CAVALLARO, Emanuele (IFAE)

Presenter(s) : Dr. TERZO, Stefano (IFAE)

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