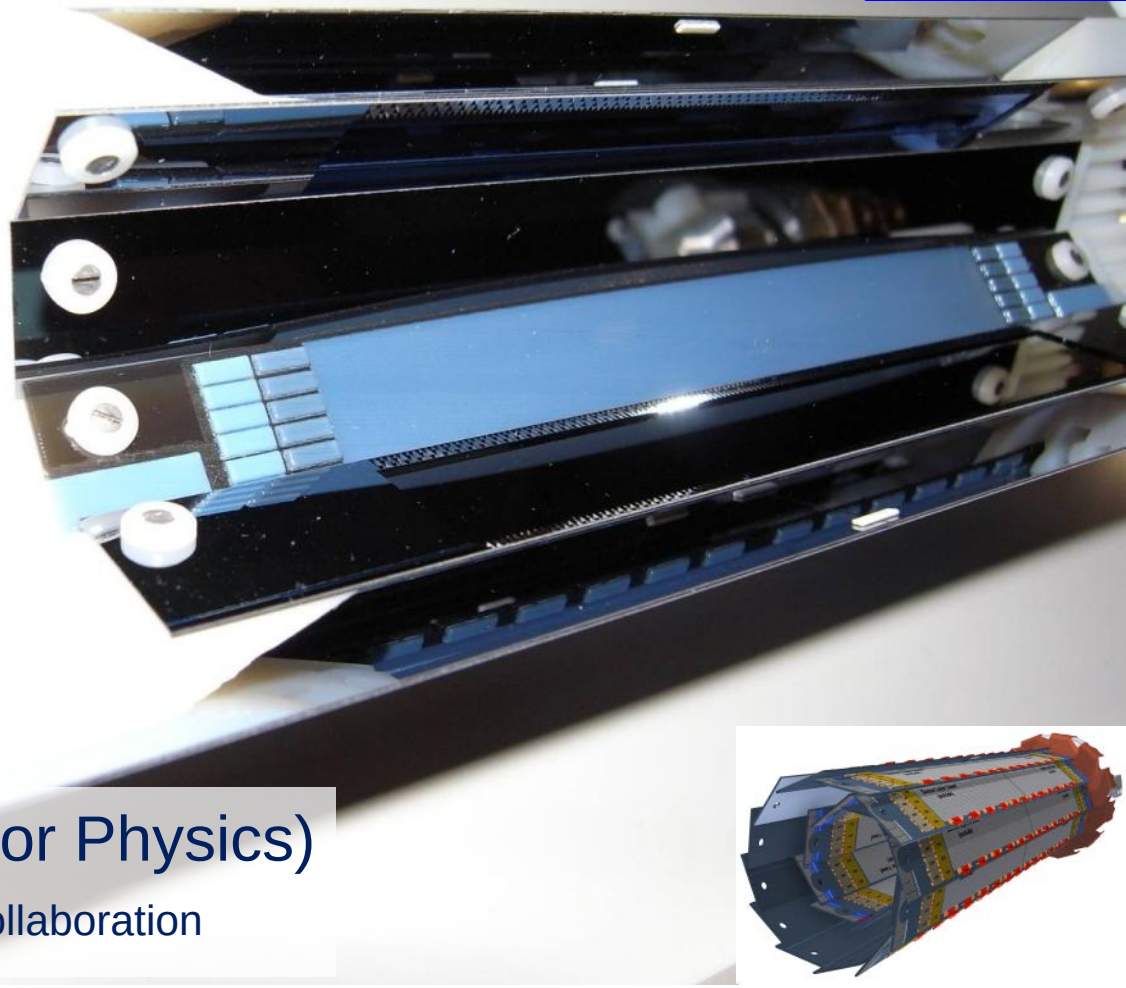
DEPFET at Belle II

The International Conference on Instrumentation for Colliding Beam Physics

February 24 - March 1, 2014
Budker INP
Novosibirsk, Russia



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on behalf of the DEPFET collaboration

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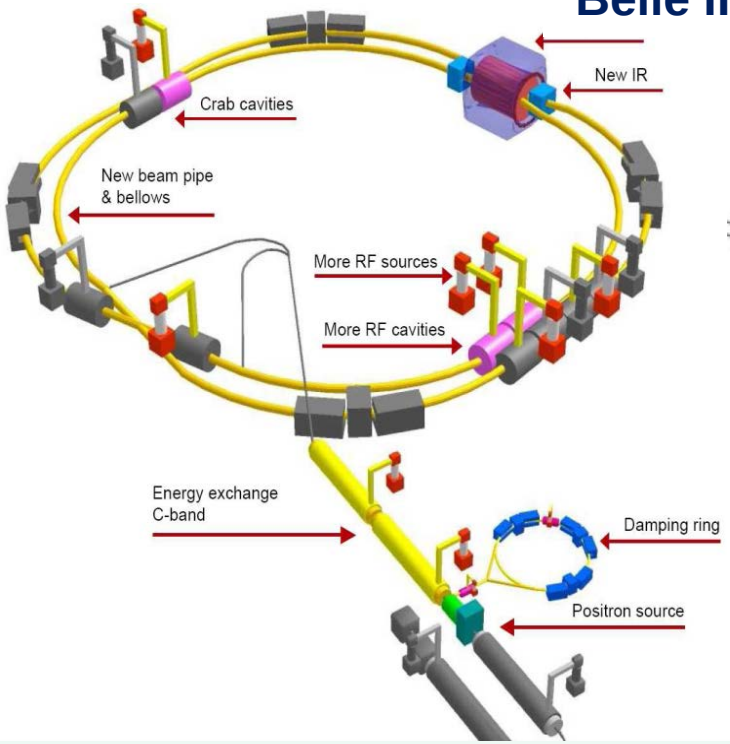
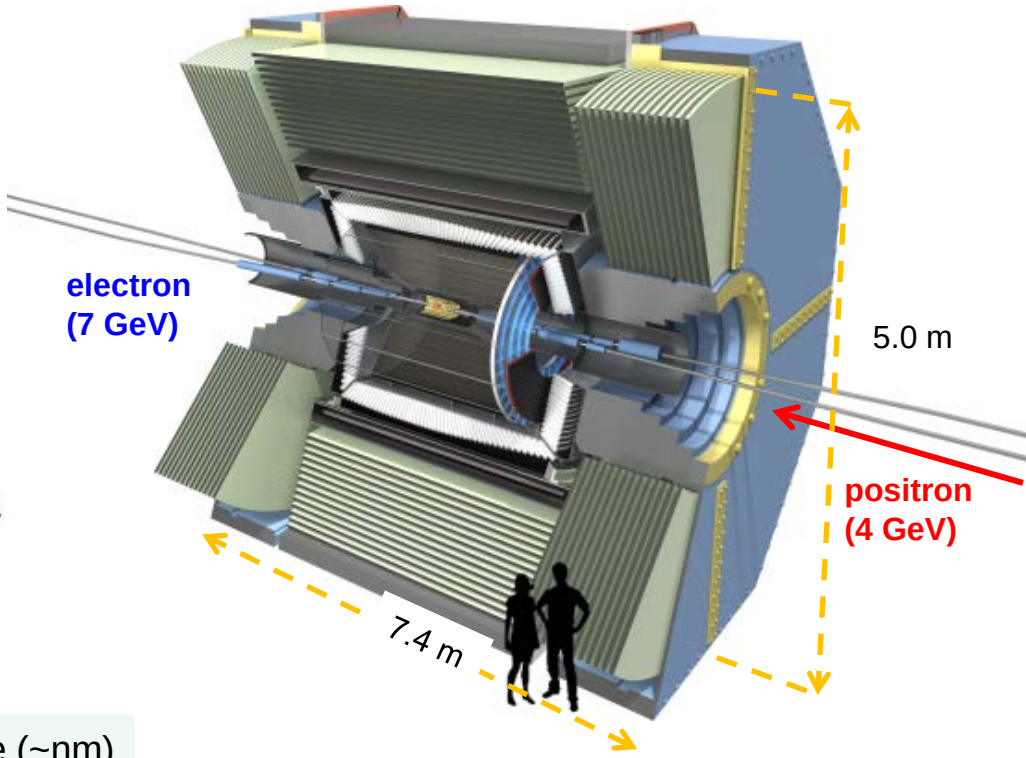
Outline

- SuperKEKB and Belle II
- Vertex Detector (VXD)
- Pixel Detector (PXD) and its characteristics
- DEPFET technology and working principle
- The readout electronics
- Gated Mode Operation
- Production / Technology Issues
- Lab Measurements and TestBeam with PXD6
- Summary and future plans

SuperKEKB upgrade

Belle II





Nano beam scheme → smaller beam size (~nm) & increased beam currents (x2)

- $\mathcal{L}$ = 8 x 10^{35} cm^{-2} s^{-1} (40 times larger than in KEKB)
- E_{e-} = 7 (8) GeV & E_{e+} = 4 (3.5) GeV ($\beta\gamma$ = 0.42 (KEK) → **0.28** (SuperKEK))
- E_{cm} = 10.58 GeV - Υ(4S)

***Changes involving the Vertex Detector (VXD)*:**

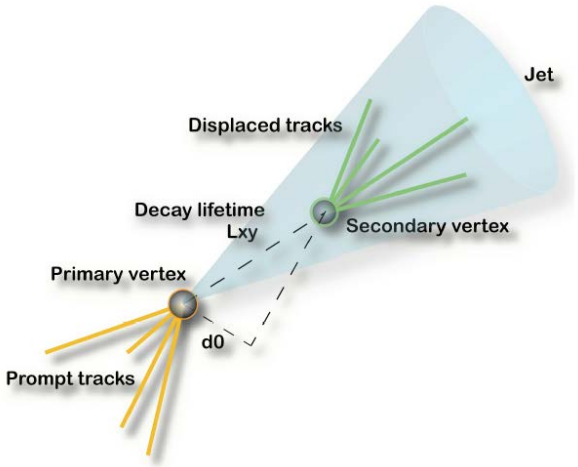
- Four layers of Double Sided Si-Strip Detector (DSSD) with a larger radius
- Two layers of DEPFET pixel detector (PXD)

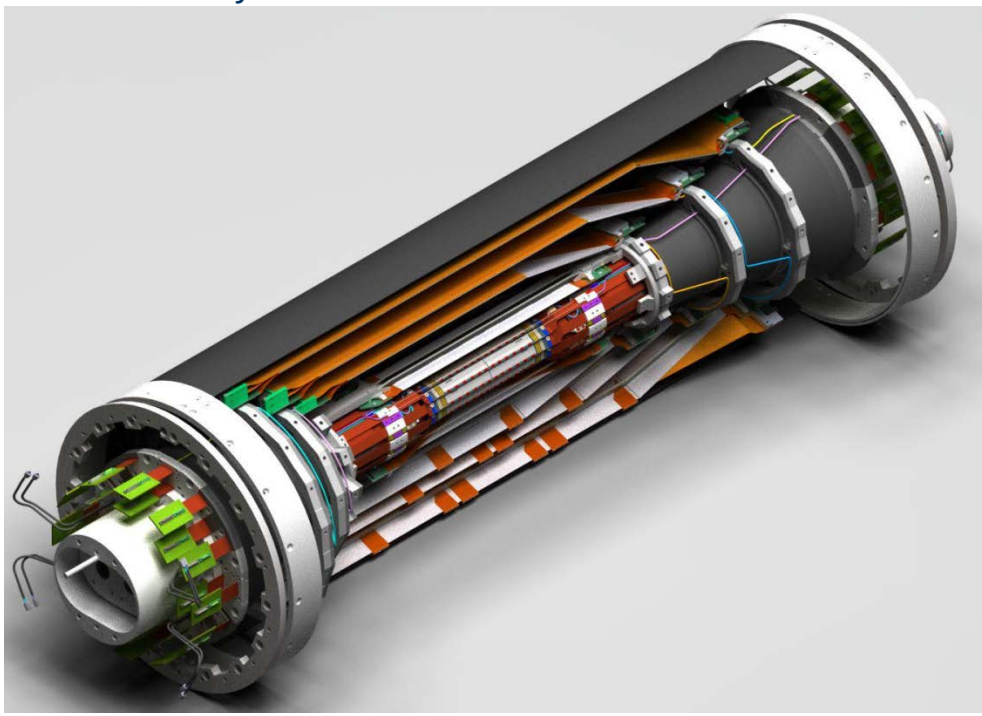
⇒ see talk from Ichiro ADACHI (Status of Belle II and SuperKEKB)

Vertex Detector (VXD)

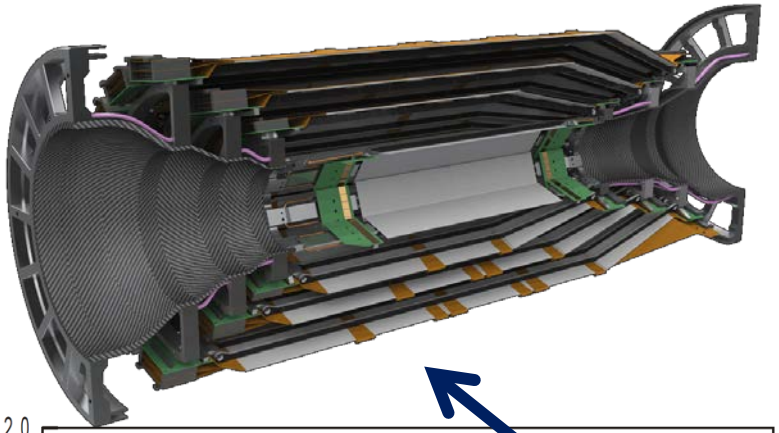
Tasks of the vertex detector:

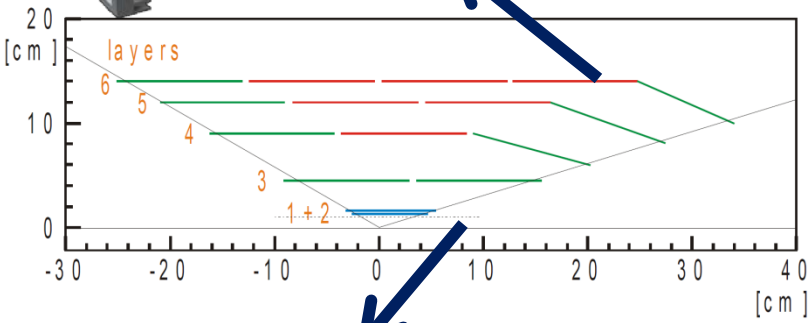
- reconstruction of primary, secondary, … vertices of short-lived particles
  decay of particles is typical in the order of 100 µm from the IP
- detect tracks of low momentum particles (in high B field) which cannot make it to the main tracker
  - → Innermost detector system as close as possible to IP
  - → highly granular pixel sensors; provide most accurate 2D position information
  - → should be massless and still provide a large enough S/N
  - → Design and specifications to a larger extent driven by machine/beam characteristics
    - → Beam background, radiation damage, occupancy …

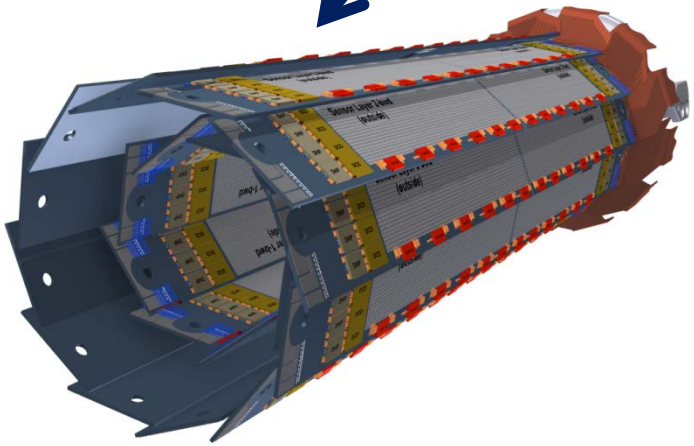




Vertex Detector (VXD)



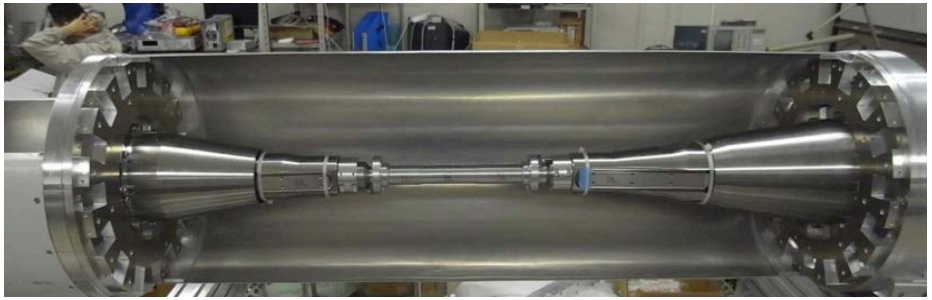




Silicon Vertex Detector (SVD)

4 layers of double sided silicon strip detector

R= 3.8 cm, 8.0 cm, 11.5 cm, 14 cm

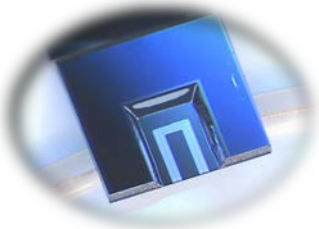


Pixel Detector (PXD)

2 layers of DEPFET pixels

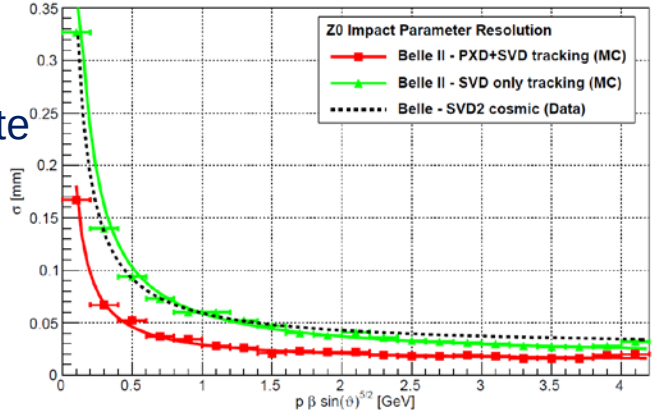
R = 1.4 cm, 2.2 cm

PXD detector requirements

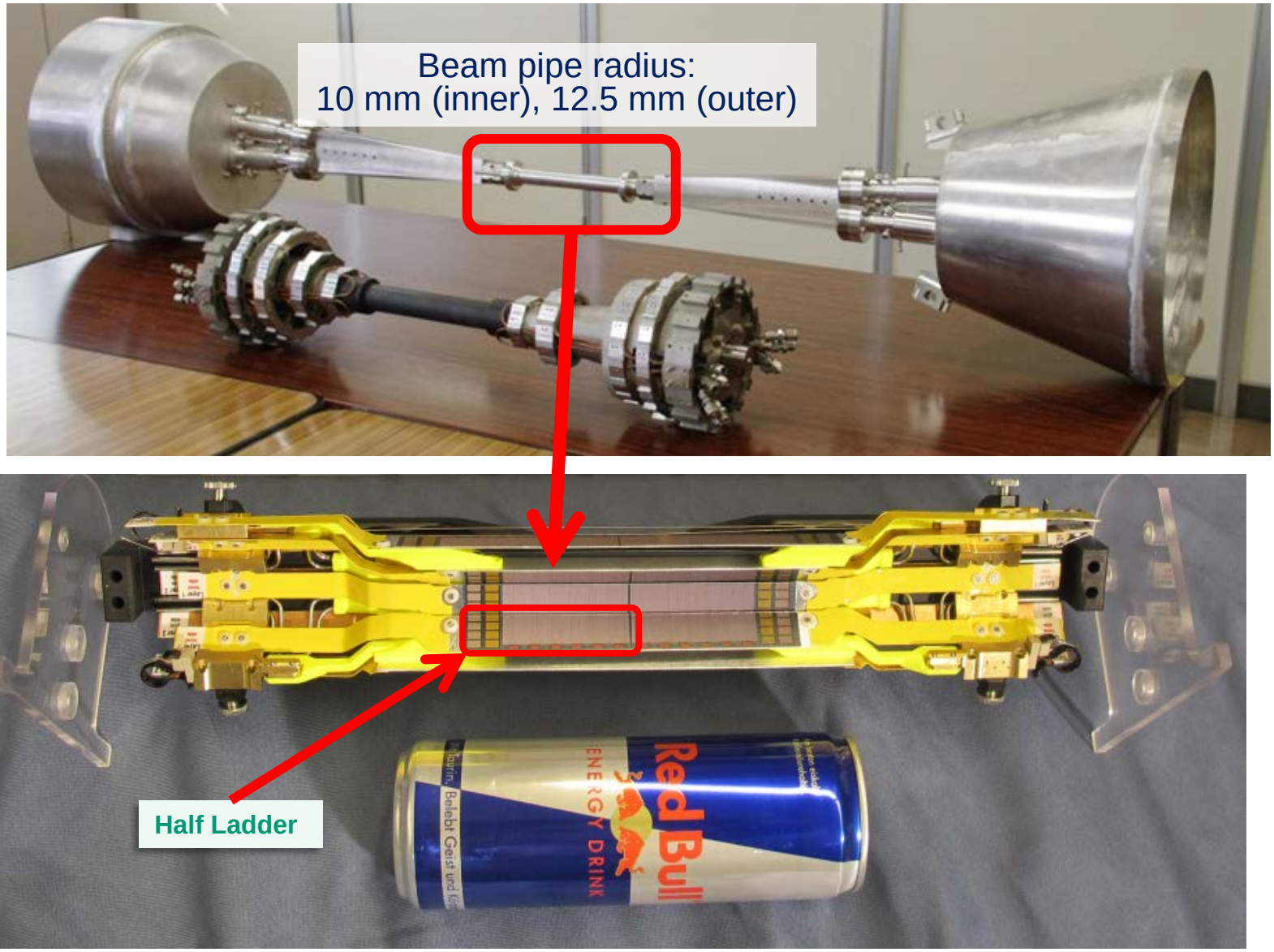


Occupancy	0.1 hits/μm²/s
Frame time	20 μs (rolling shutter mode)
Momentum range	Low momentum (<1GeV)
Acceptance	17°-150°
Radiation	~20 kGy/year, $1 \cdot 10^{10}$ n/ab^{-1}cm²

- Belle II is dominated by low momentum tracks
- Modest intrinsic resolution (15 μm), dominated by multiple scattering → Moderate pixel size (50 x 75 μm²)
- Lowest possible material budget (0.2% X_0/layer) [including ASICs]
- due to higher background (20x-40x): Radiation damage and occupancy, fake hits and pile-up noise
- 10x higher event rate => higher trigger rate
- Replace inner layers of SVD with PXD

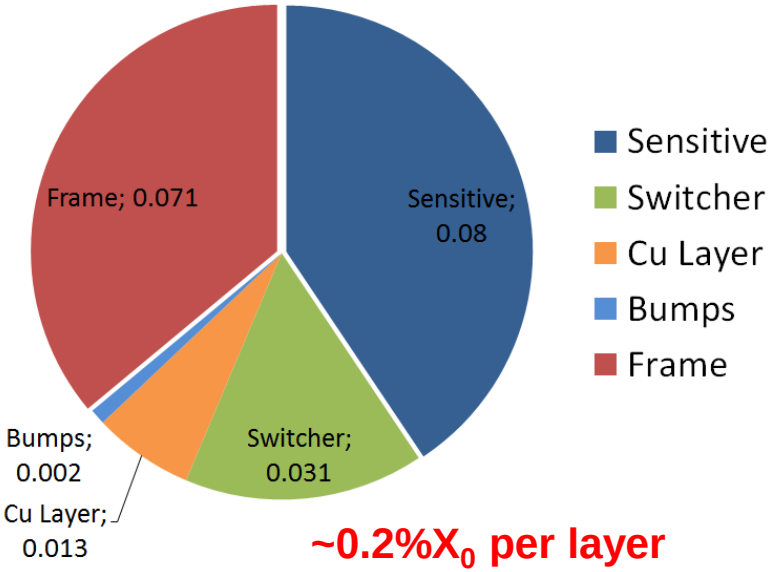


Mockup of the Belle II PXD Detector

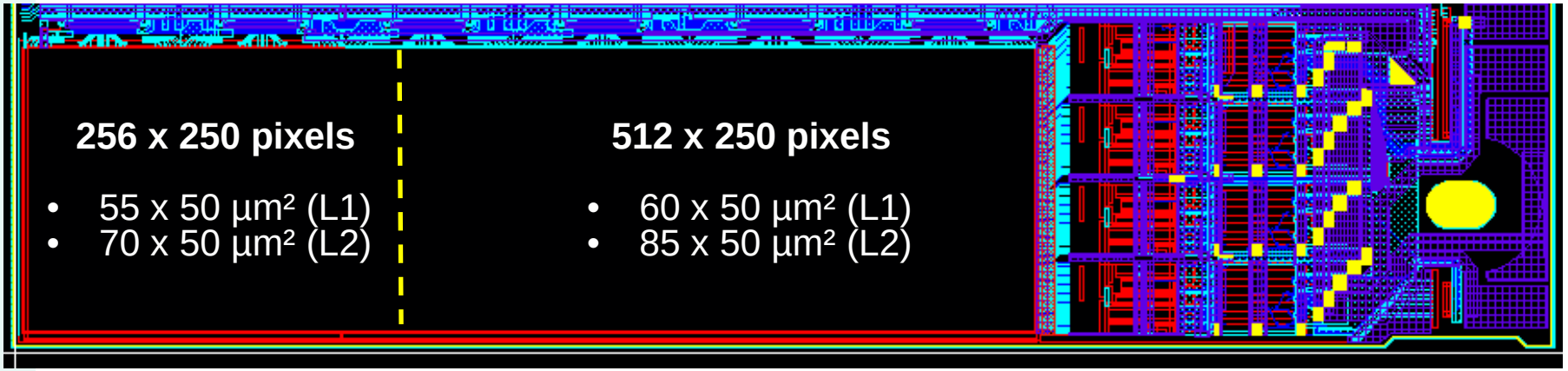


Half Ladder of DEPFET PXD

	Inner layer (L1)	Outer layer (L2)
# modules	8	12
Distance from IP (cm)	1.4	2.2
Thickness (µm)	75	75
Total # pixels	3.072 x 10^6	4.608 x 10^6
Pixel size (µm^2)	55, 60 x 50	70, 85 x 50
Sensitive area (mm^2)	44.8 x 12.5	61.44 x 12.5
Sensor length (mm)	90	123
Frame/Row rate	50 kHz / 10 MHz	50 kHz / 10 MHz

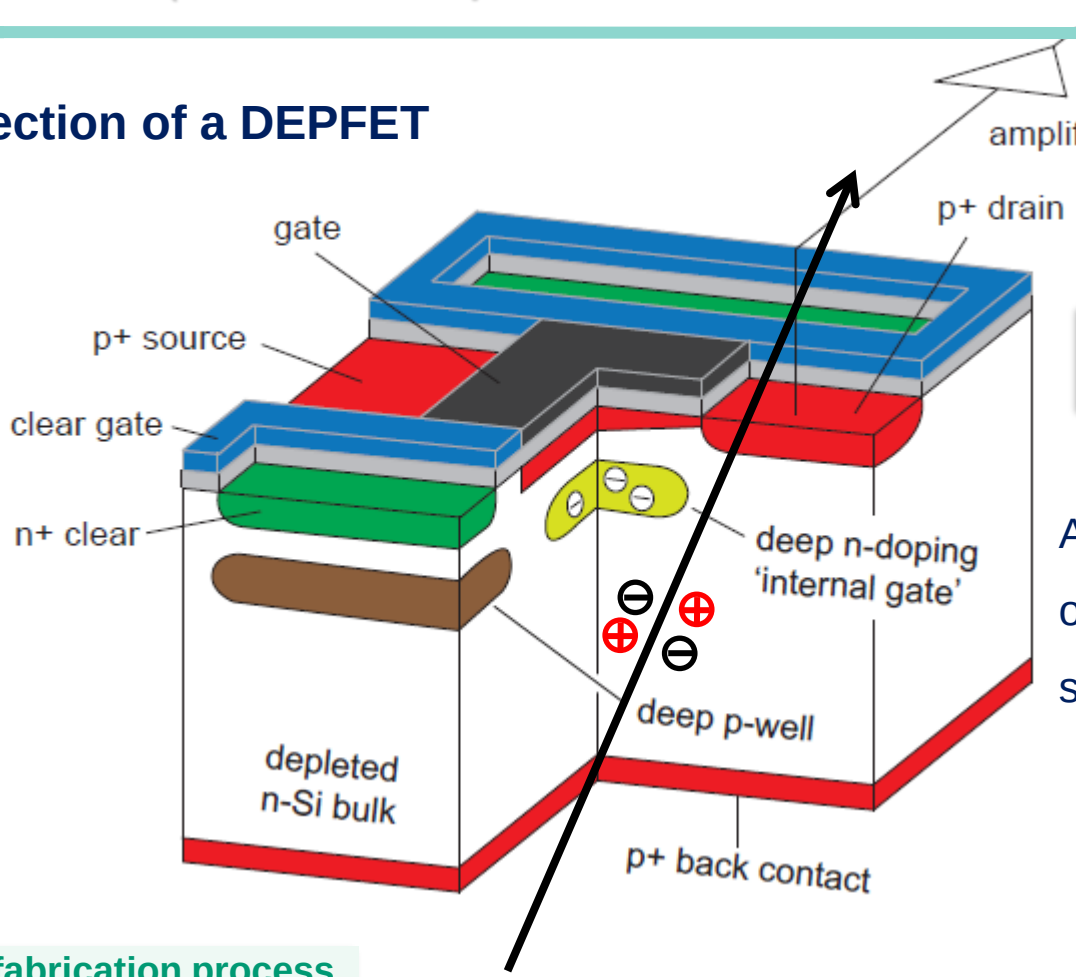


~0.2%X_0 per layer



DEPFET (DEPleted p-channel Field Effect Transistor)

Cross-section of a DEPFET



internal amplification:
$g_q \approx 0.5$ nA/e$^-$

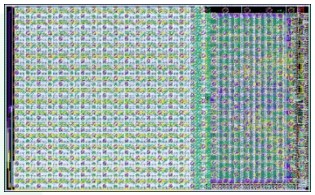
A DEPFET is a MOSFET onto a sideward depleted silicon bulk

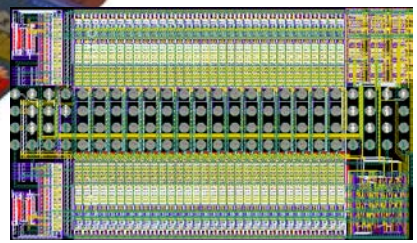
90 steps fabrication process
- 9 Implantations
- 19 Lithographies
- 2 Polysilicon layers
- 2 Aluminum layers
- 1 Copper layer
- Back side processing

→ Low noise
→ Low power
→ High signal/noise-ratio
→ Non-destructive readout

Control and readout electronics

Drain Current Digitizer (DCD)
- Keeps the columns line potential constant
- 8 bit ADCs
- Compensates for pedestal current variation (2bit DAC)
- Programmable gain and BW
- 256 input channels (4 per module)



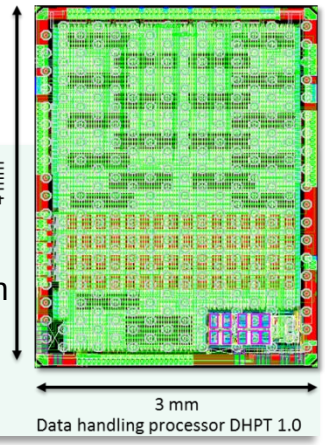


DEPFET

SWITCHER
- Fast voltage pulses up to 20 V to activate gate rows and to clear the internal gate
- JTAG for interconnectivity tests
- 64 output drivers for both gate and clear channels → address 32 matrix segments
- 768 rows → 192 electrical rows → 6 ASICs needed per module

Kapton Flex cable
- Power Supply via soldered contacts and bond wires
- Data transmission via bond wires
- 4 layers, 48 cm

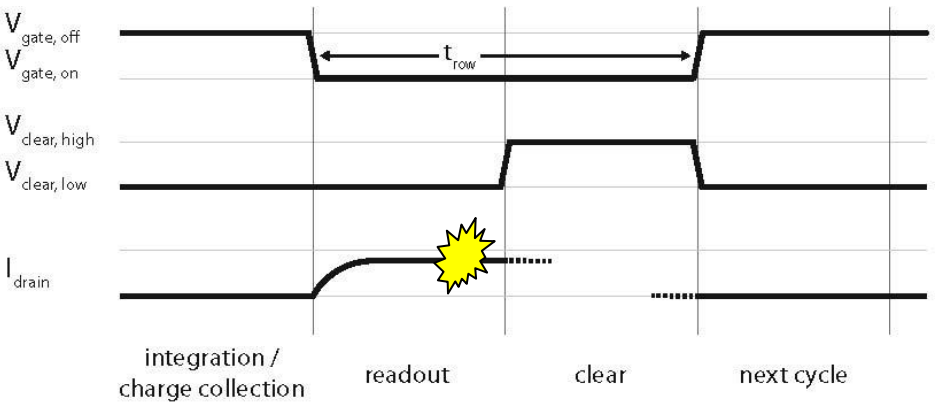
Data Handling Processor (DHP)
- Pedestal correction
- Common mode correction
- Data reduction using the zero suppression
- Triggered readout scheme introduces further data reduction
- Controls the Switcher sequence

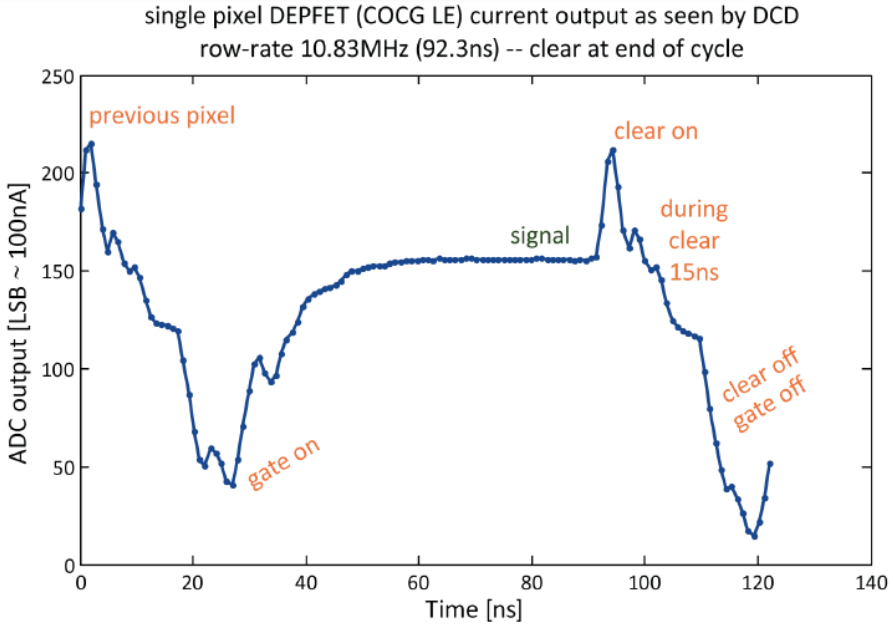


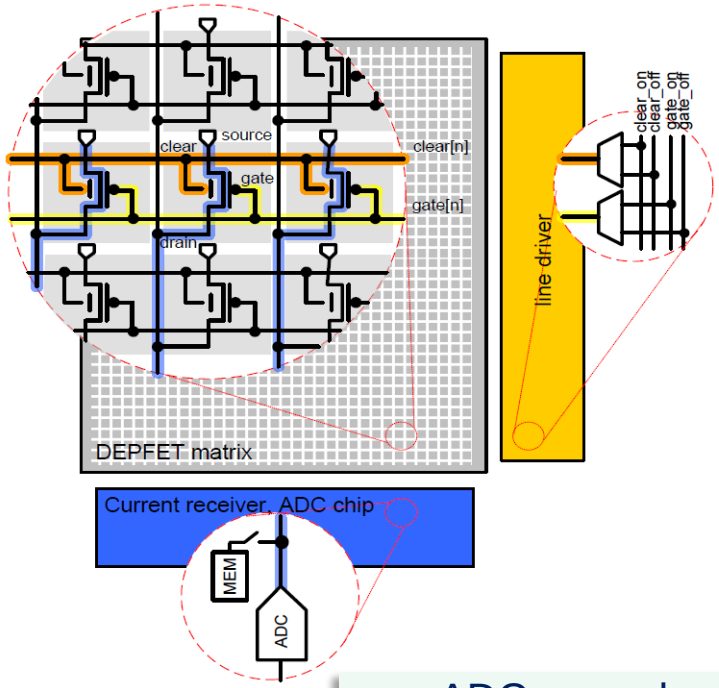
Rolling Shutter Mode - Readout

Rolling Shutter Mode

- Low power consumption; only one row is active; all are sensitive
- Single Sampling (pedestal subtraction and common mode correction)
- Readout time: 20 µs for entire frame (50 kHz)
- Read-Clear cycle: 100 ns

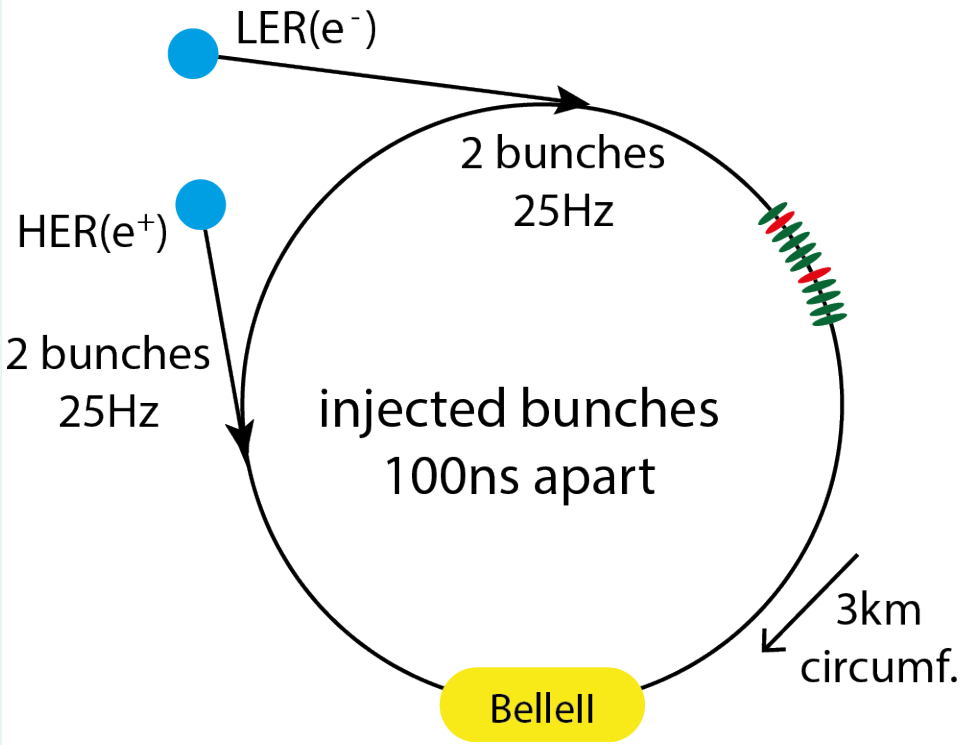


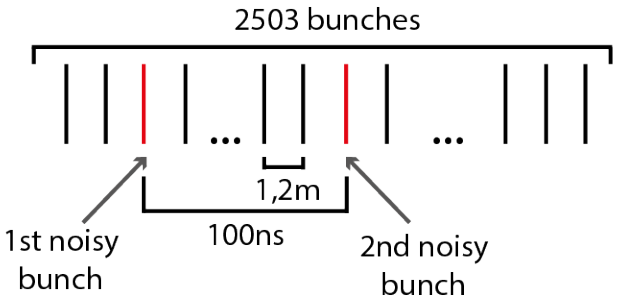


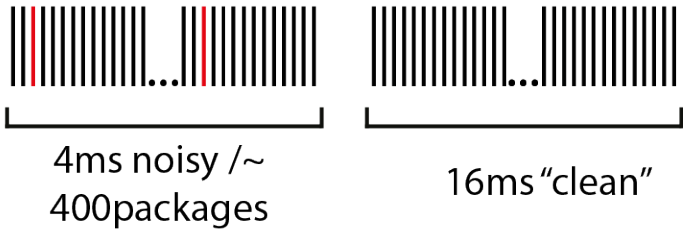


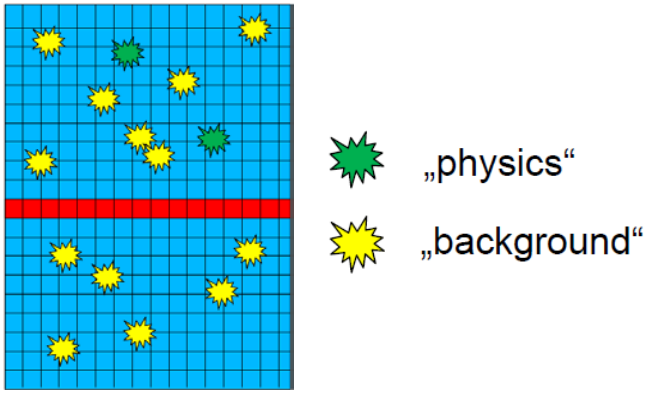
one ADC per column

Gated-Mode Operation









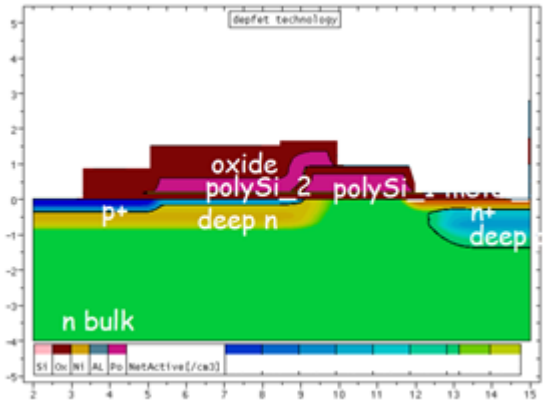
Continuous injection scheme; total rate: 50 Hz

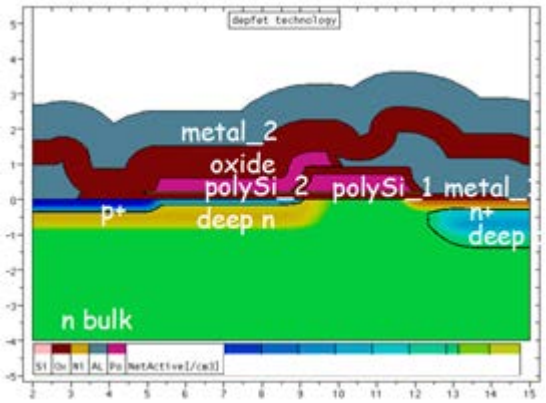
Due to Liouville theorem injected bunches need to cool (4ms); results in „noisy" particles

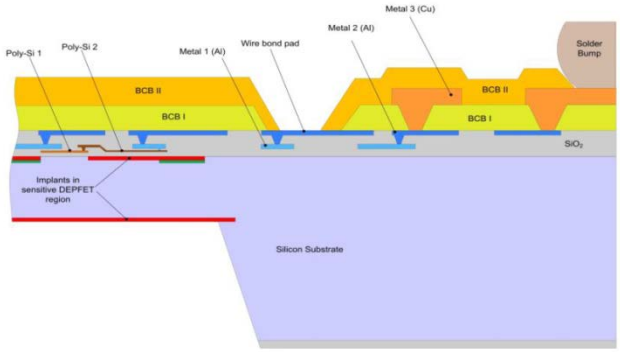
Very large occupancy („junk charge")

If similar damping is assumed for SuperKEKB => 20% deadtime for PXD

Processing







Phase I – before metal

- Implantations
- Polysilicon
- Dielectric depositions

Phase II – Aluminum

- Metal 1
- Isolation
- Metal 2

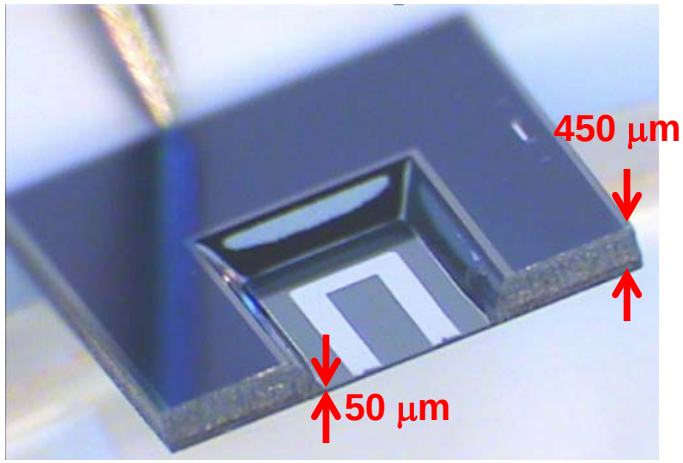
Phase III – Thinning & Copper

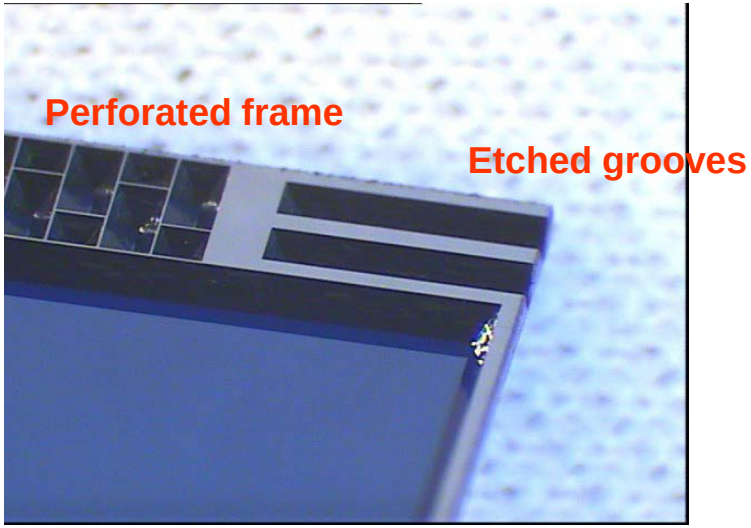
- Handle Wafer Removal
- Dielectric deposition
- Metal 3
- Passivation

front end of line

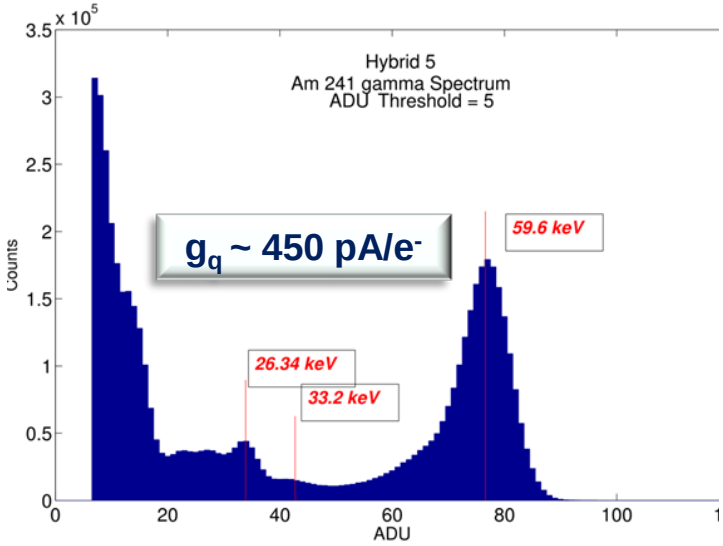
back end of line

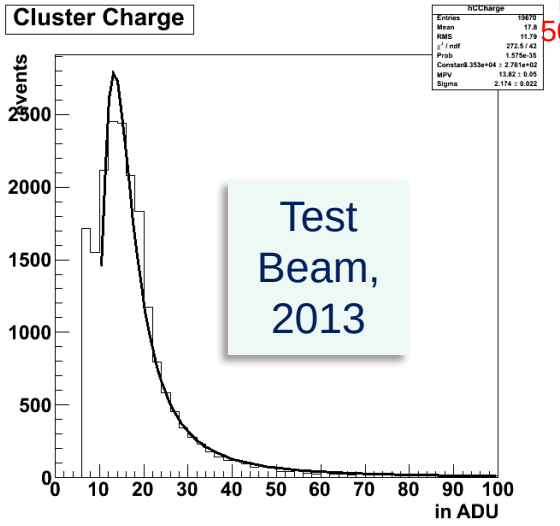
Thinning Technology

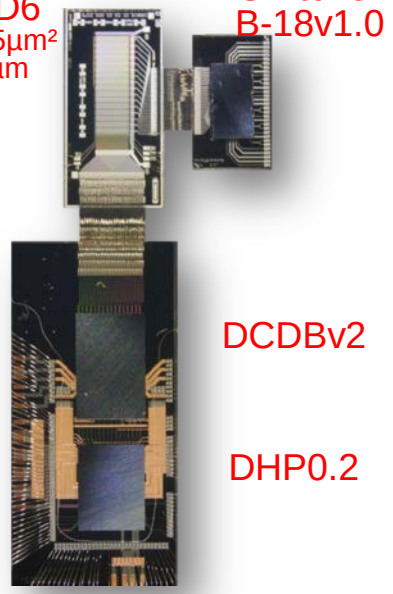




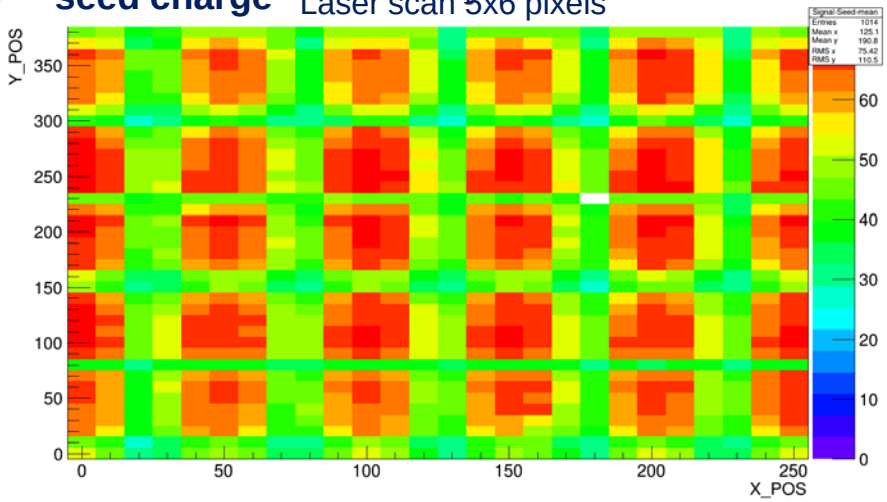
Lab measurements and Beam Test



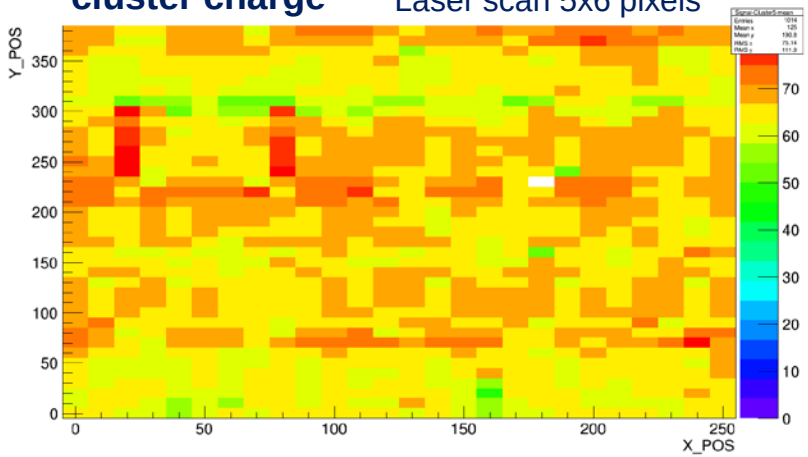




seed charge Laser scan 5x6 pixels

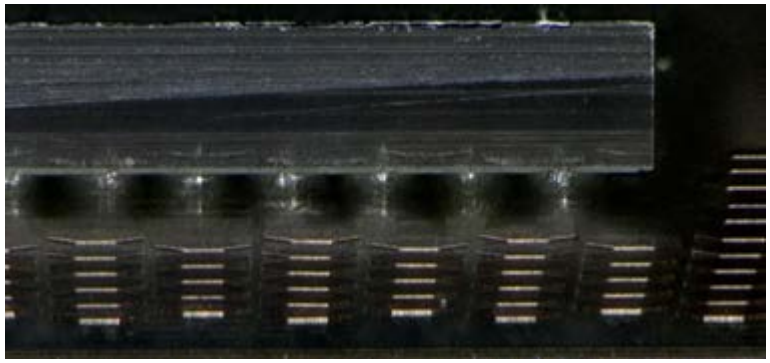


cluster charge Laser scan 5x6 pixels

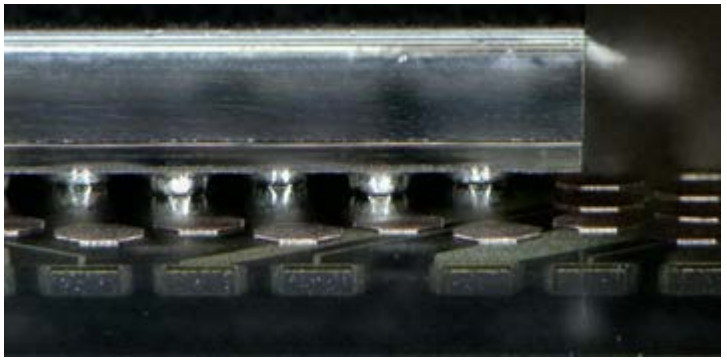


Homogeneous charge collection

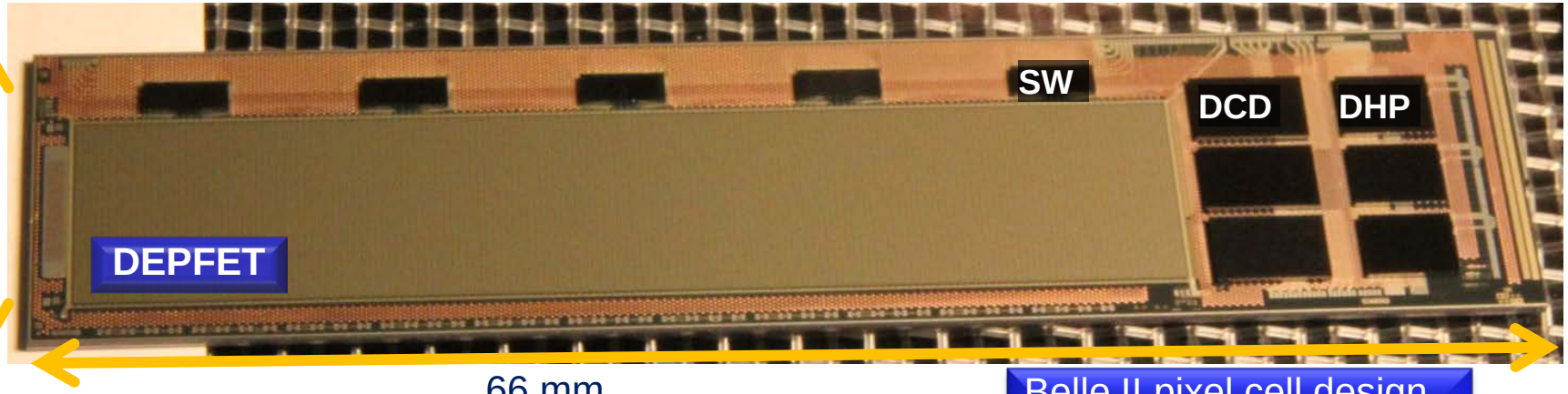
Large PXD6 Prototype Matrix – fully populated module



Switcher-B18v2.0



DCD-Bv2



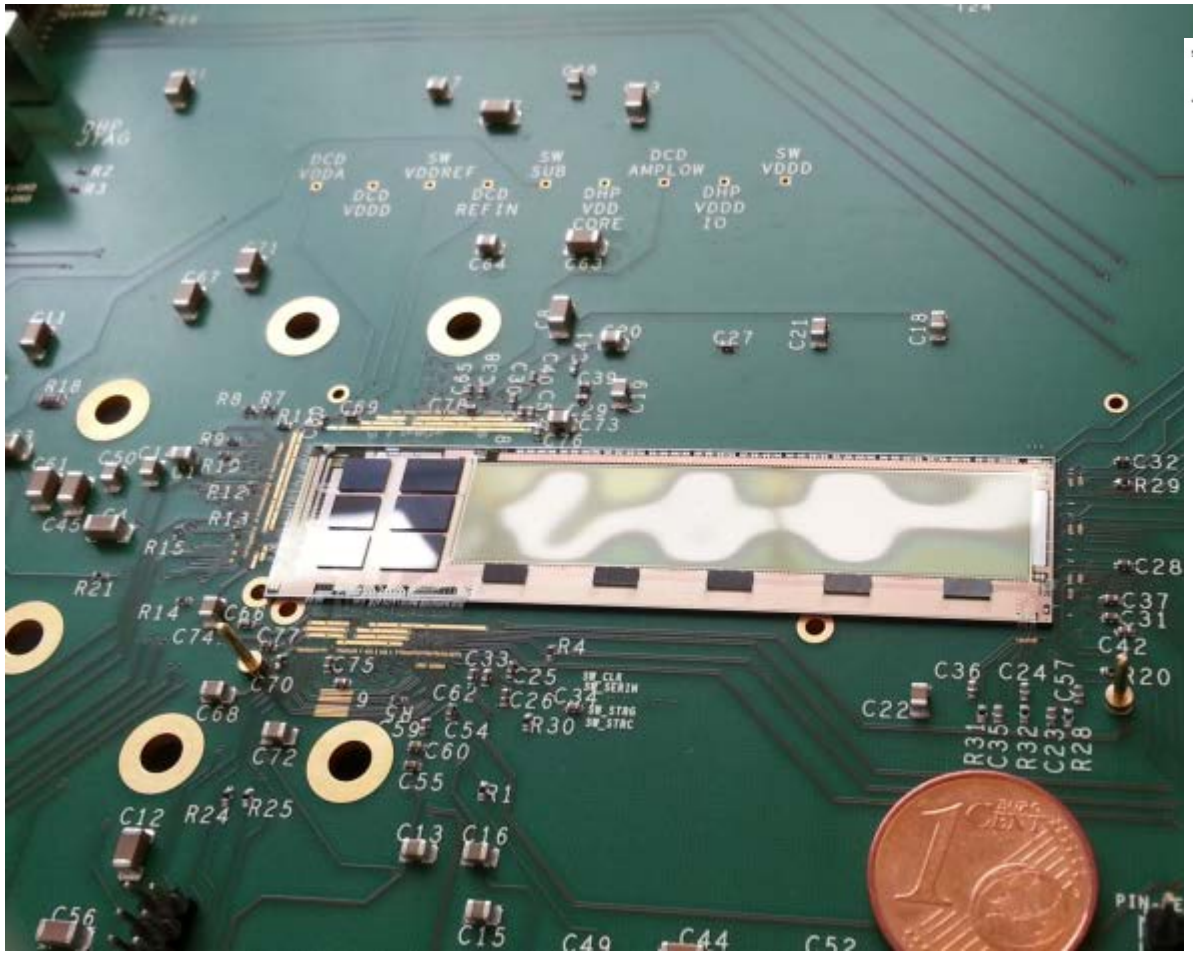
Belle II pixel cell design
640x192 pixels matrix
50x75x50 µm³ pixel cells

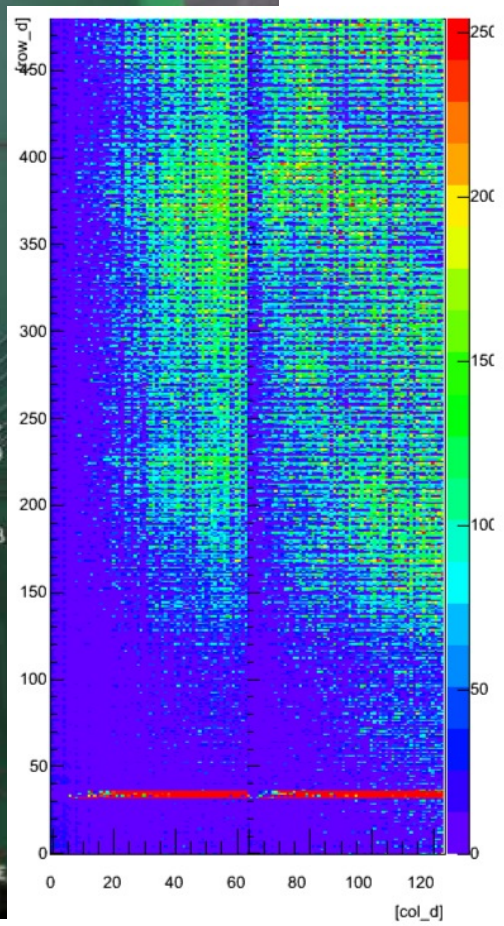
Testbeam 2014 at DESY (Hamburg, GER)

Glue (between PCB and PXD6 module): Epotek 920 EL, cure at 120°C

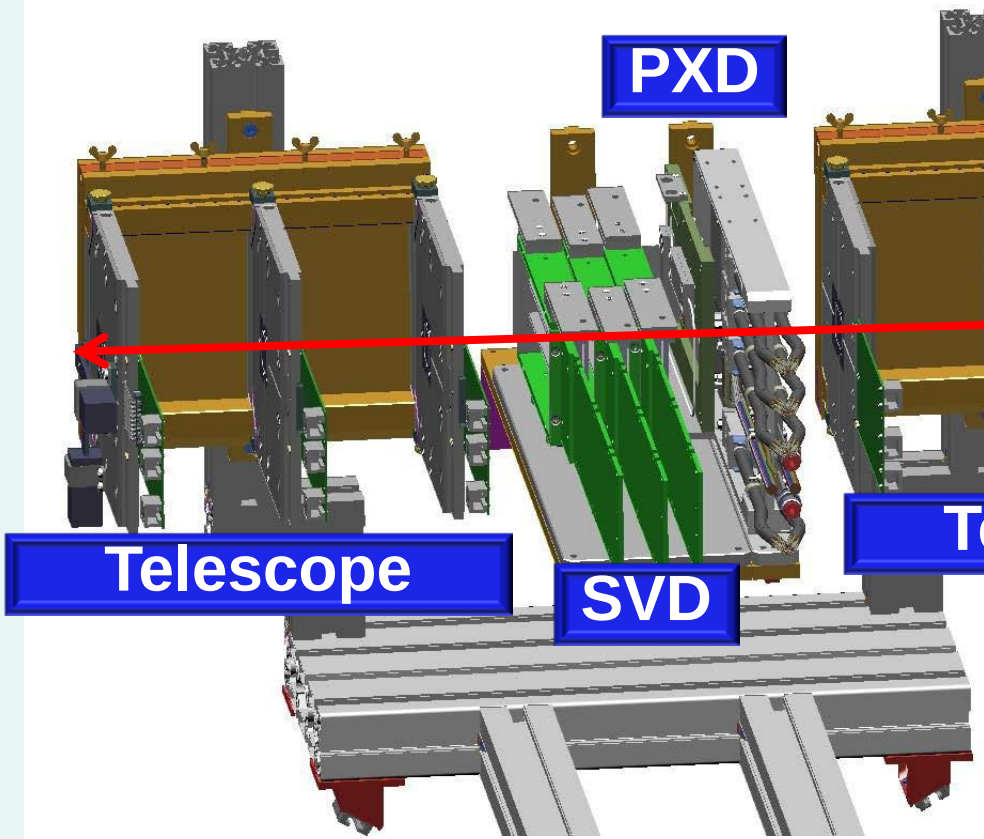
Due to different coefficients of thermal expansion

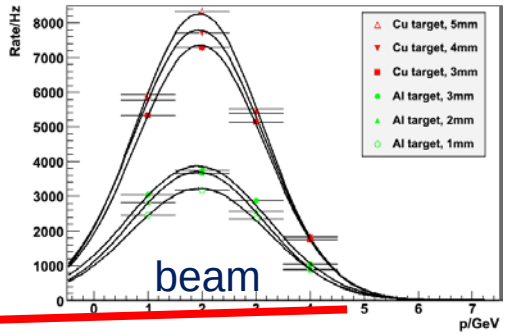
⇒ Bowing of matrix (crest & valley: 80 µm at a distance of 1 cm)

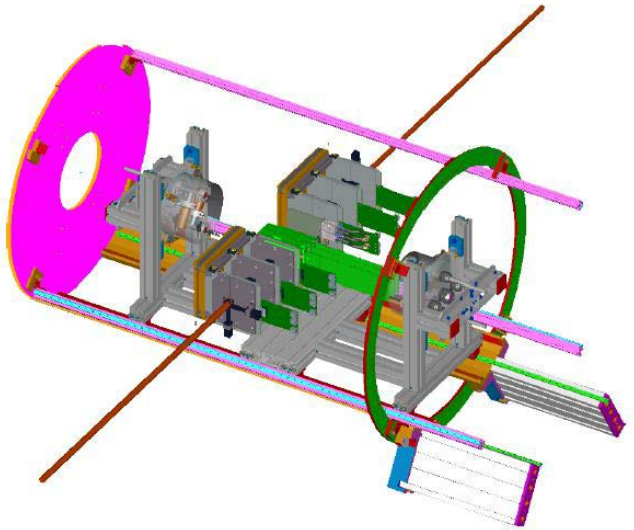




Vertex Detector and AIDA Telescope – Testbeam 2014

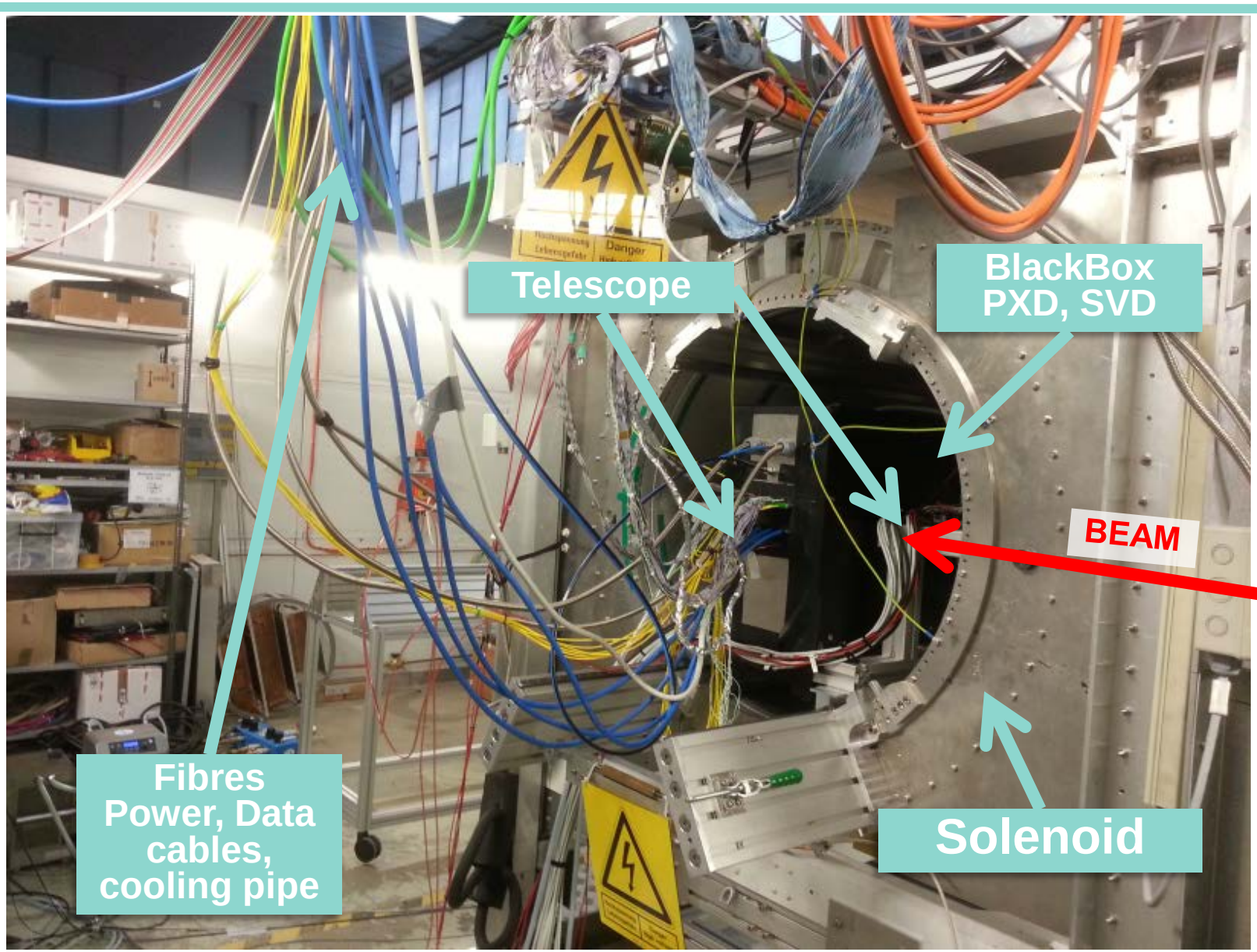






1 Tesla Solenoid Field

Setup – Testeam 2014 – DESY



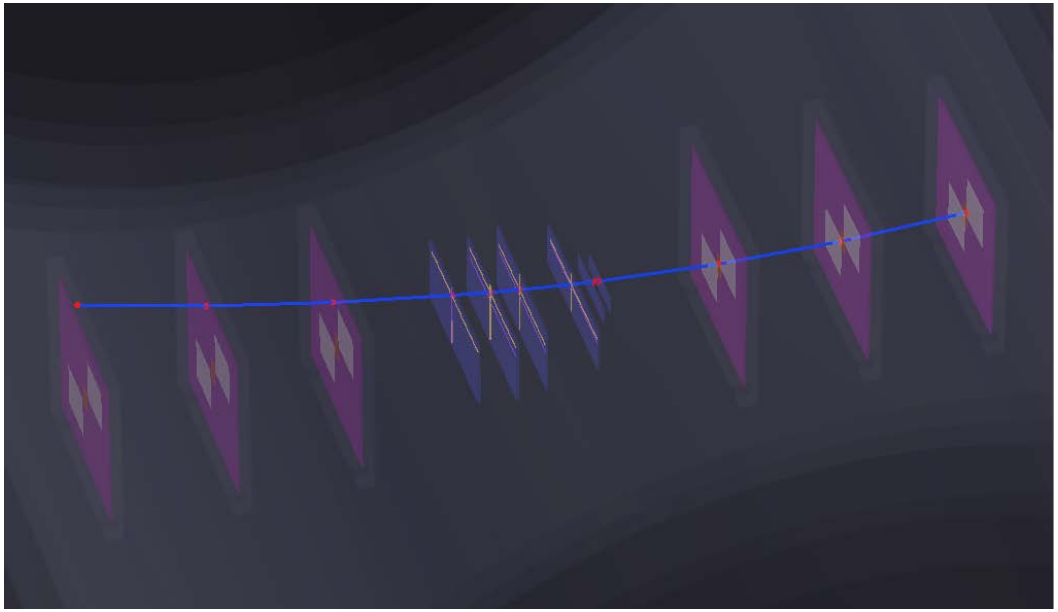
Further Talks related to PXD & Testbeam

Testbeam results, ”DEPFET as a measurement device: simulation and data reconstruction“

⇒ by Peter KVASNICKA; following talk

“The Belle II Pixel Detector DAQ”

⇒ by David MÜNCHOV, Saturday 10:05



DEPFET Collaboration

- CNM/IFAE, Barcelona
- Charles University, Prague
- DESY, Hamburg
- HLL, Munich
- IFCA, Santander
- IFIC, Valencia
- IFJ PAN, Krakow
- IHEP, Beijing
- KEK-PF, Tsukuba
- KIT, Karlsruhe
- LMU Munich
- MPI for Physics, Munich
- TU, Munich
- University of Barcelona
- University of Bonn
- University of Heidelberg
- University of Giessen
- University of Göttingen

Summary

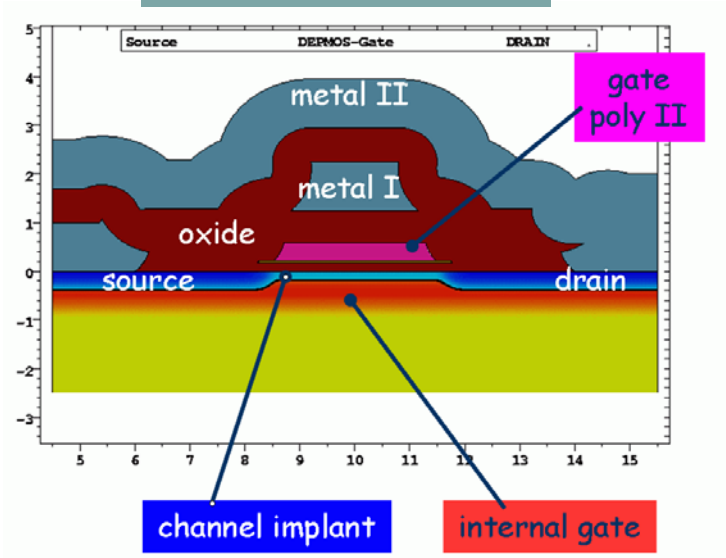
- To fully exploit the high luminosity (increase by factor 40), the detector is currently upgraded
- Excellent *spatial resolution* of ~ 15 μm; *occupancy* ~ 1%, fast readout (50 kHz frame rate), huge number of pixels (~ 8 Mpix) => fits all the requirements for Belle II
- complex DEPFET *technology*; fully functional; successful demonstration in lab and beam tests
- Thinning of sensitive area down to 50μm / 75 μm (0.2% X_0), minimizing multiple scattering;
- Low *power consumption* ~ 18 W per ladder
- ASICs and Sensors close to final version
- Signal to Noise: ~ 40 (including noise from ASICs)
- Many aspects not covered in this talk; though in development by the Collaboration

Backup

Radiation Tolerance

Gate Dielectrics: ~ 200nm

- Radiation field at Belle II dominated by ~MeV electrons/positrons from QED beam background



Ionizing Radiation - Total Ionizing Dose (TID)

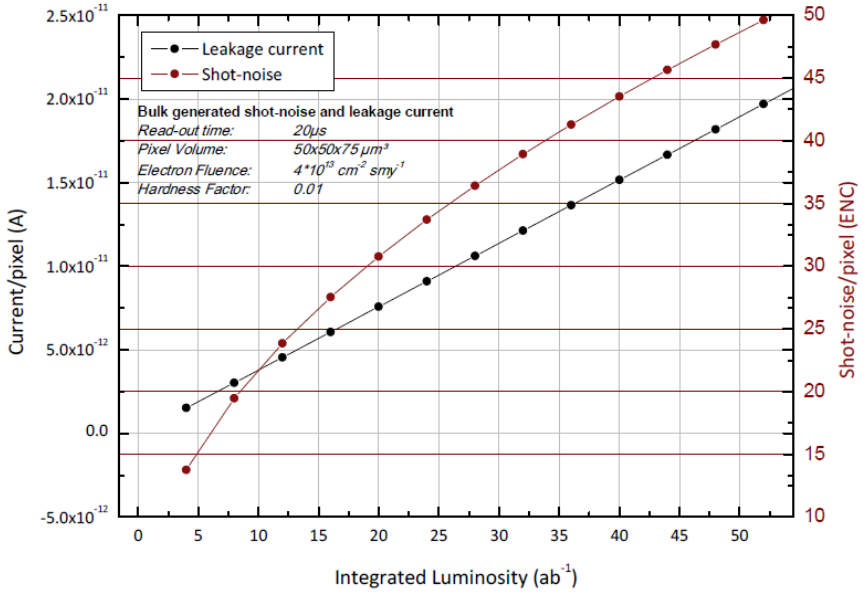
(~2Mrad/a at Belle II)

- Positive fixed oxide positive charge → ΔV_T
- interface trap density →
  - reduced mobility (g_m)
  - higher 1/f noise

Non Ionizing Energy Loss (NIEL)

(10^{12} n_{eq}/cm^2/year at Belle II)

- leakage current increase → shot noise
- trapping not considered to be critical
- Type inversion expected after 10^{14} n_{eq}/cm^2



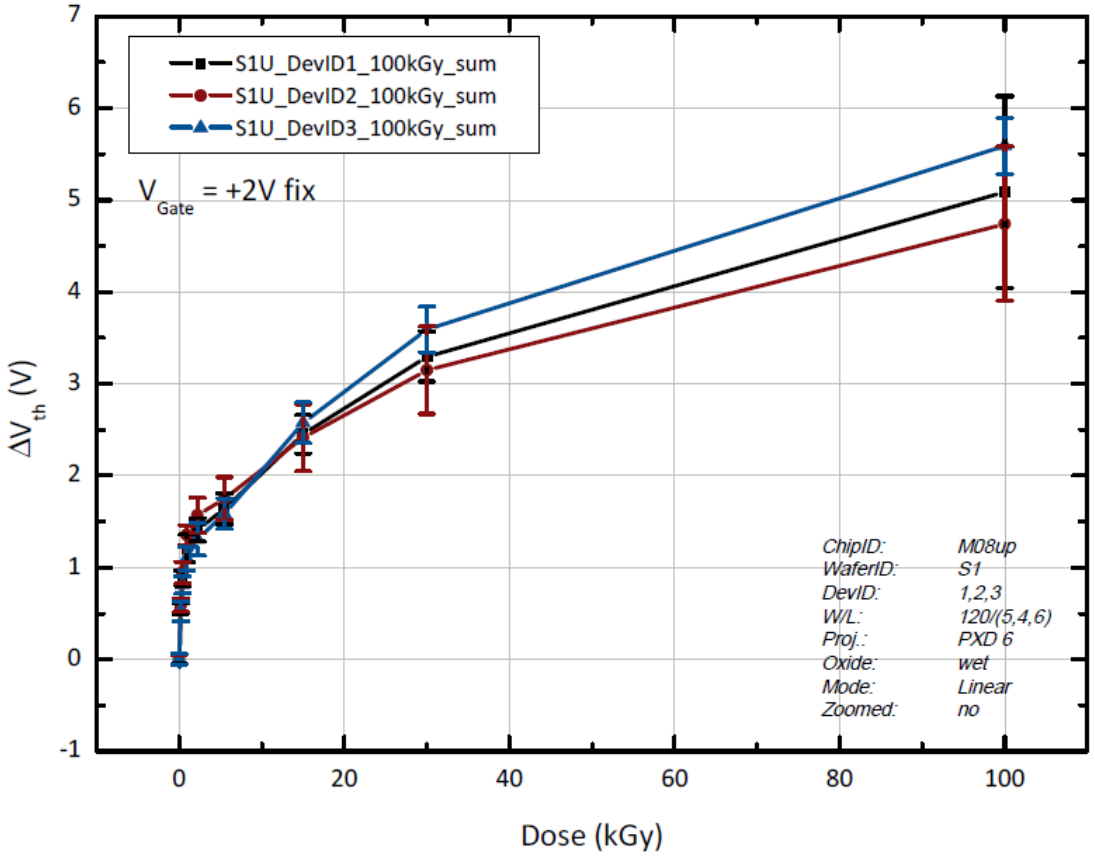
Radiation Tolerance

R&D since 2008:

- Reduce t_{ox}
- Optimize gate dielectric layer

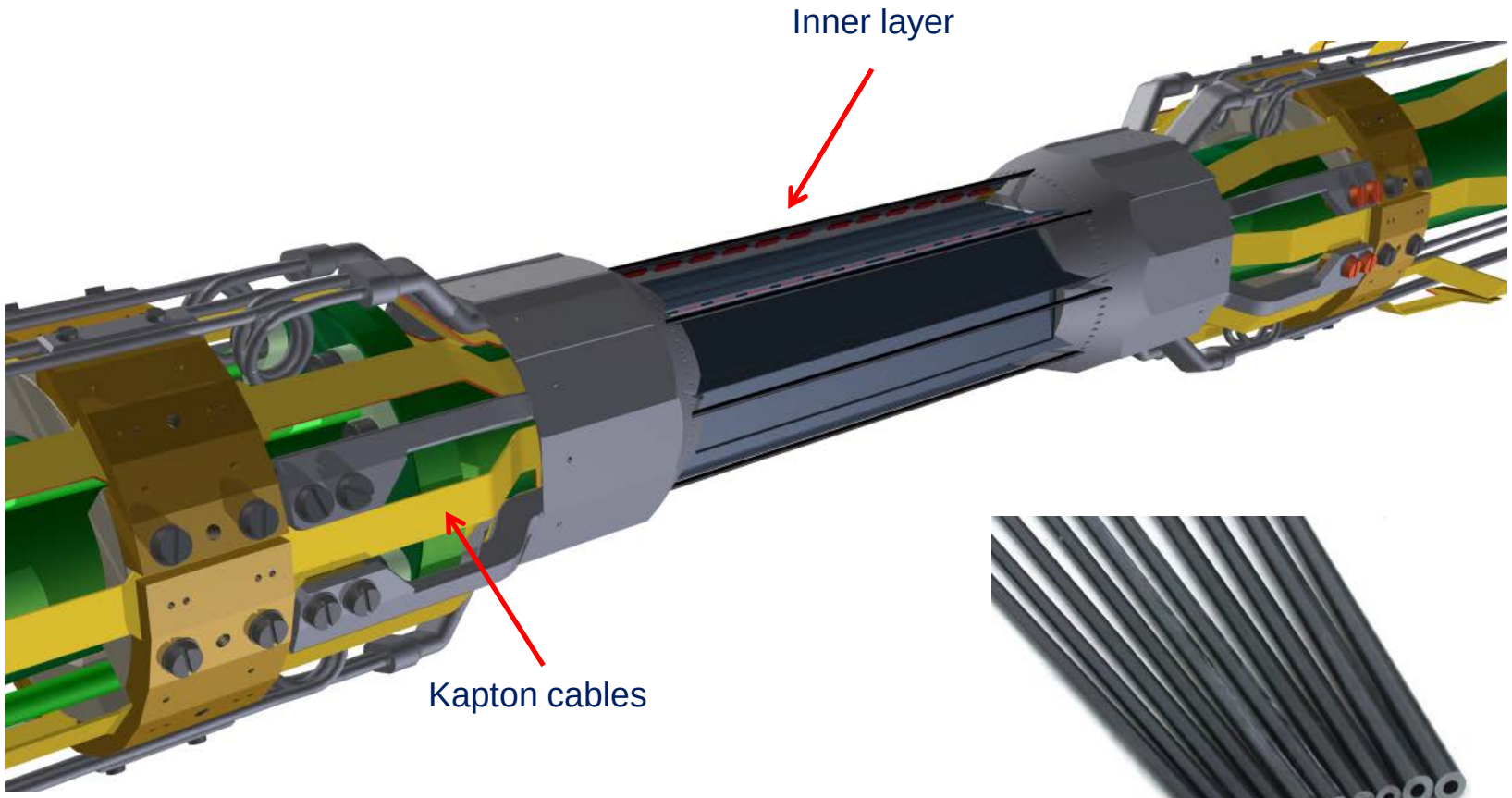
ΔVt(10Mrad): ~15V → 3 V

The remaining small threshold voltage shift can easily be compensated by a shift of the operating voltages of the DEPFET!



→ Safe operation for about 10 years in Belle II

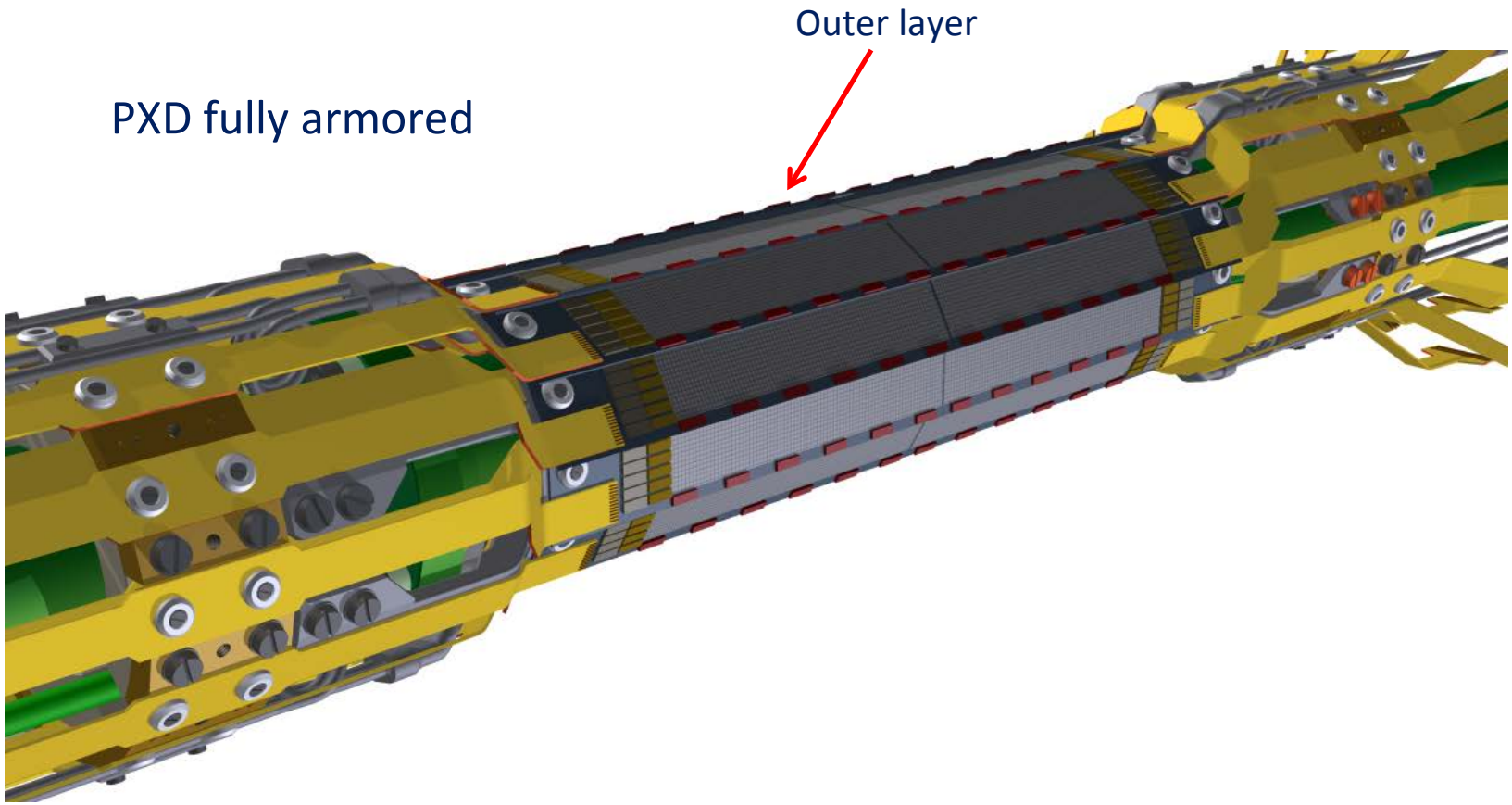
Belle II – Pixel Detector – Inner Layer



Inner layer close to the IP (14mm)

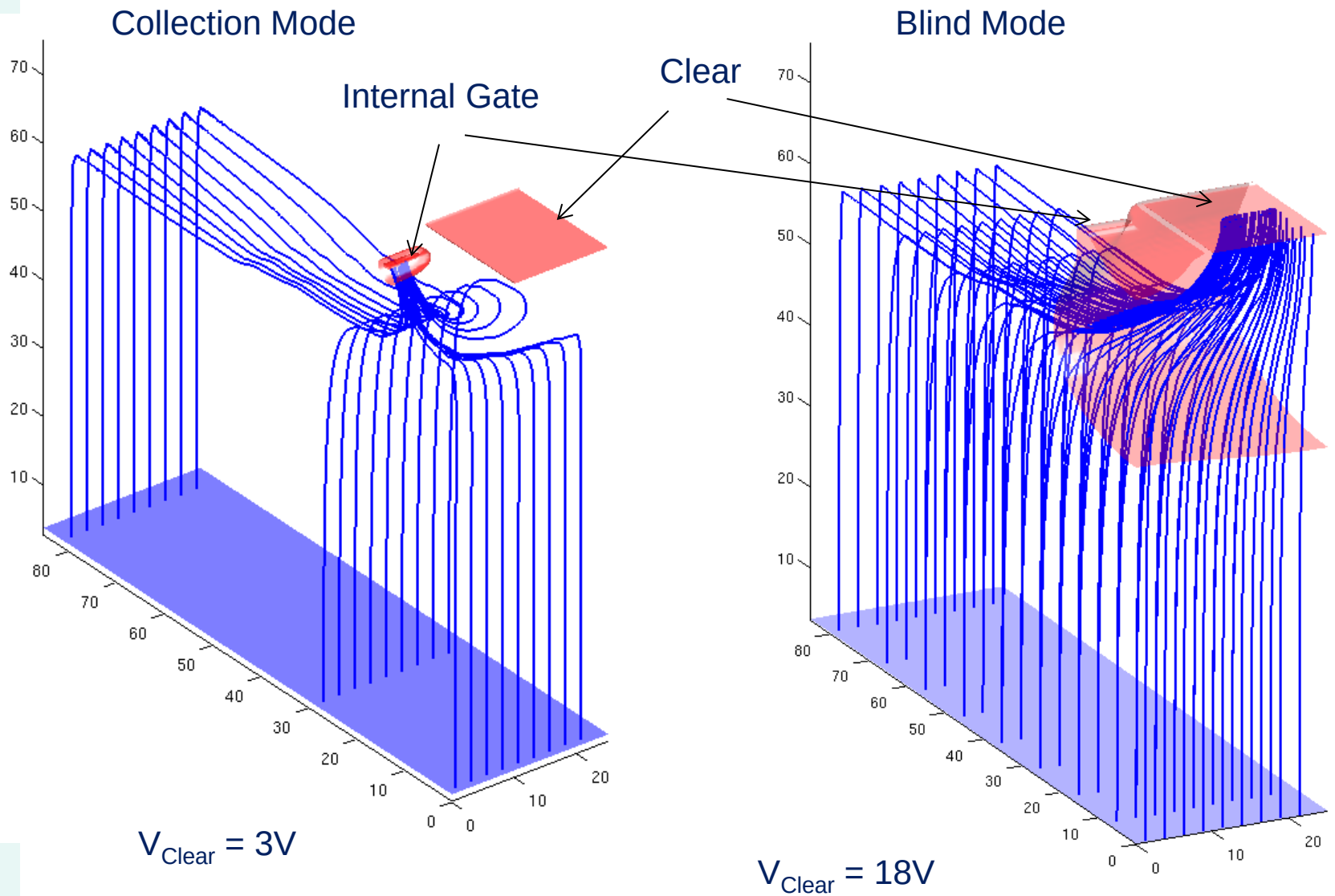
Additional carbon fibers capillaries to cool the Switchers, if needed (not tested yet)

Belle II – Pixel Detector – OuterLayer

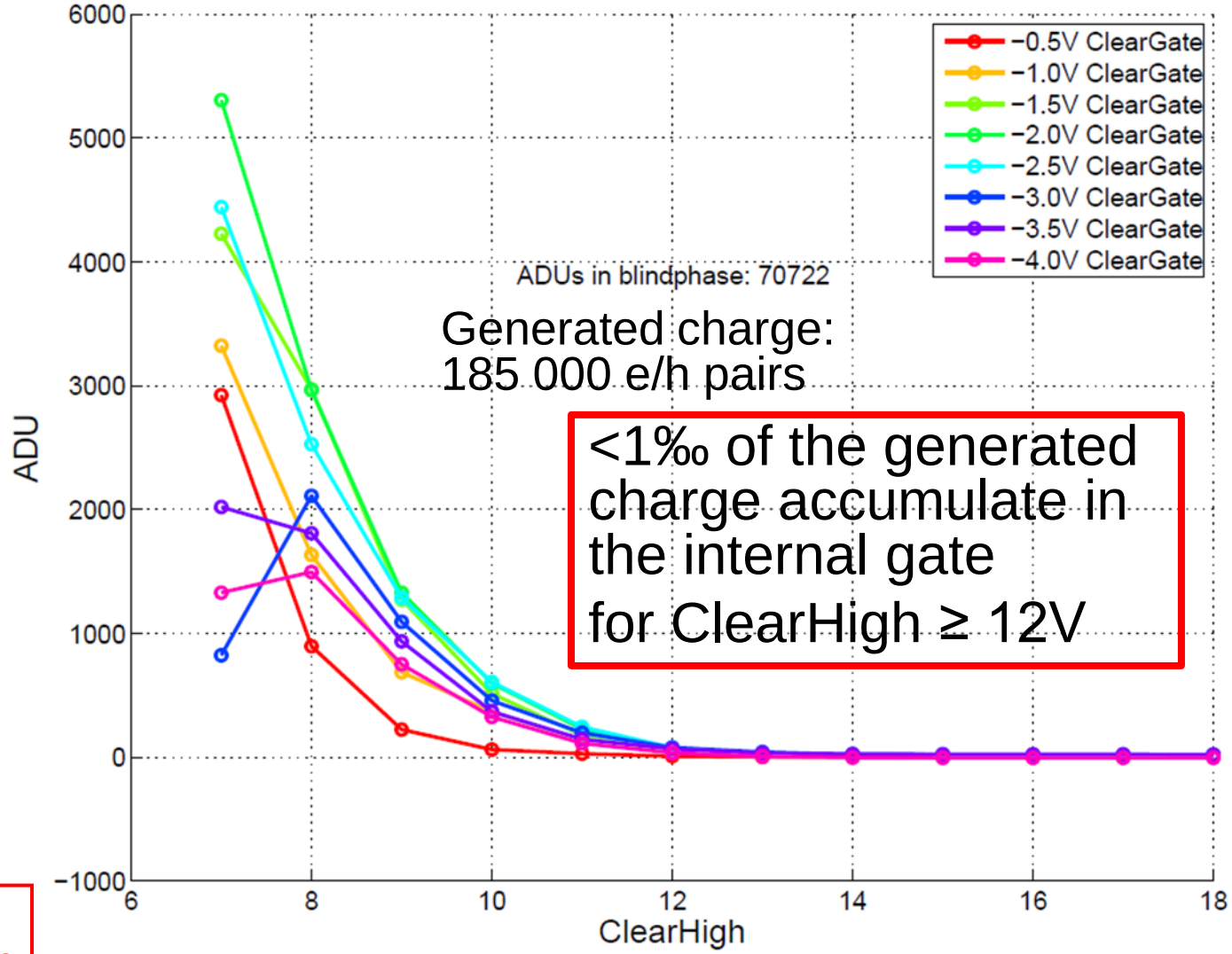


- Low material budget cooling
- Massive structures outside the acceptance to cool down the readout chips
- The center of the ladder rely on cold air

Gated Mode – Simulations – trajectories of electrons

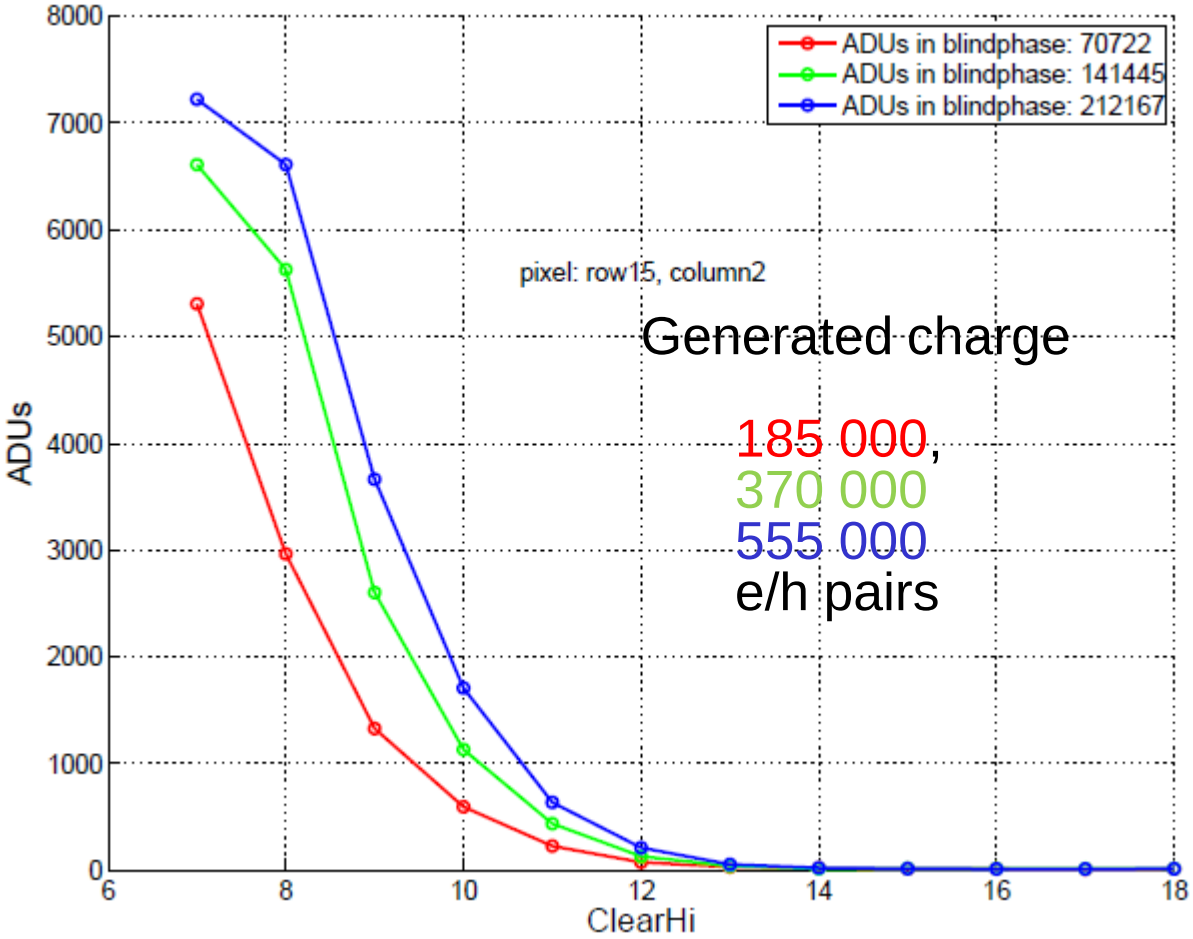


GM: Generation of Junk Charge – CCG dependance



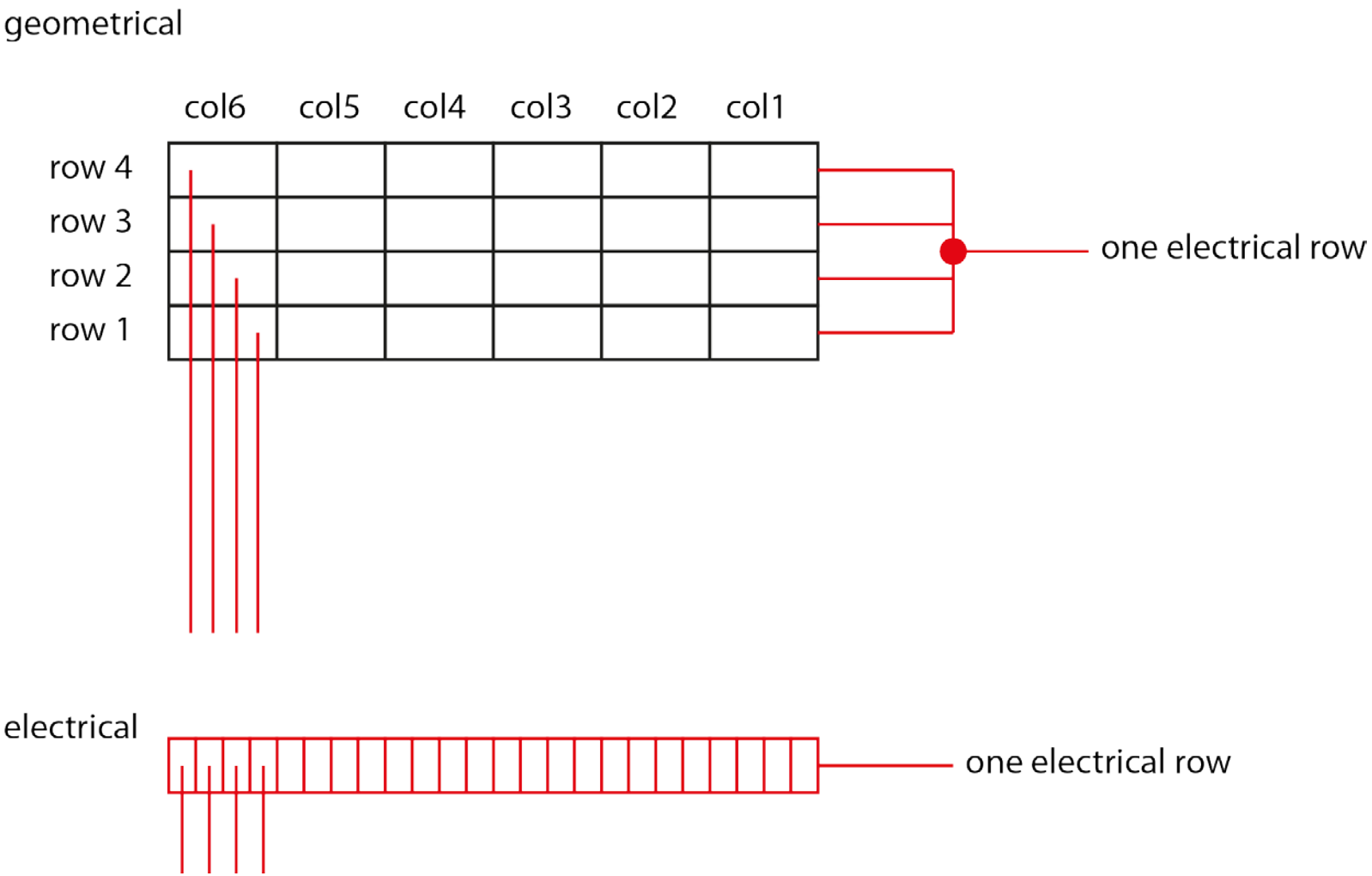
1ADU = 2.61 electrons

GM: Generation of Junk Charge – Laser intensity dependence

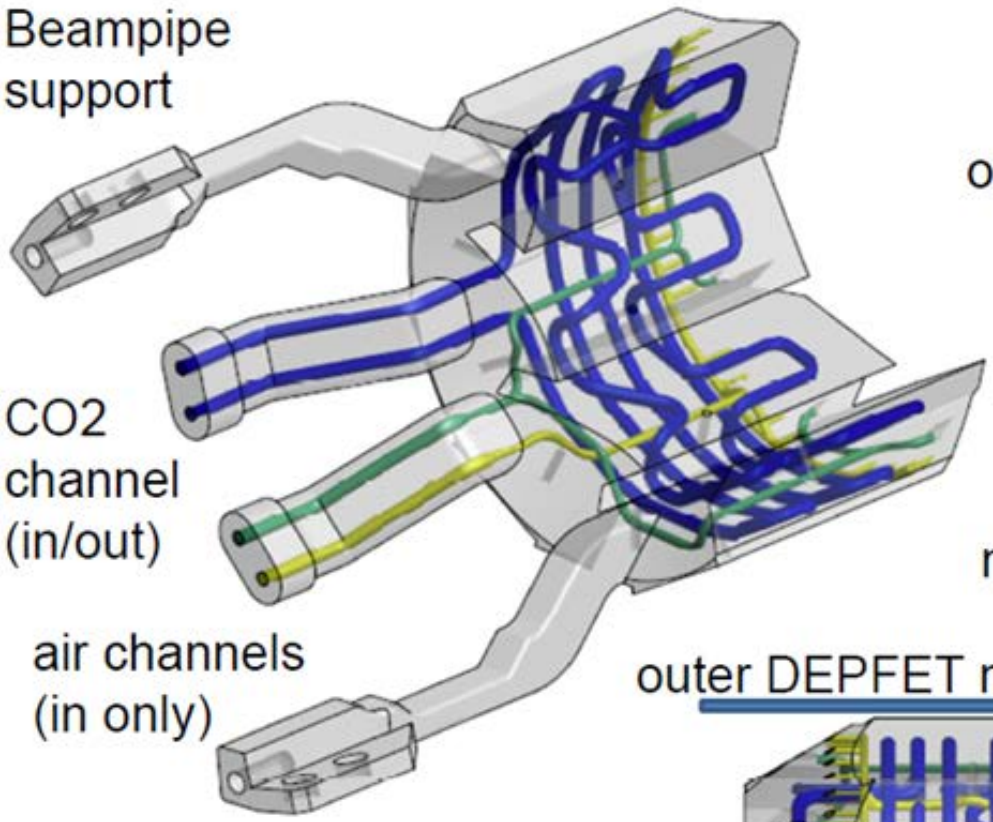


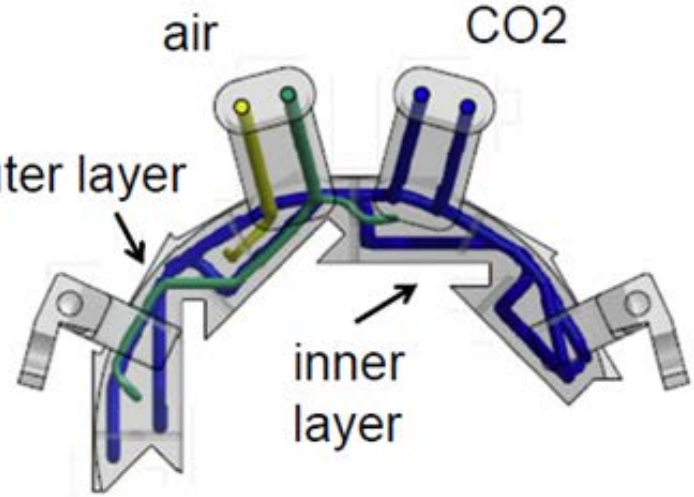
1ADU = 2.61 electrons

Four Fold Readout

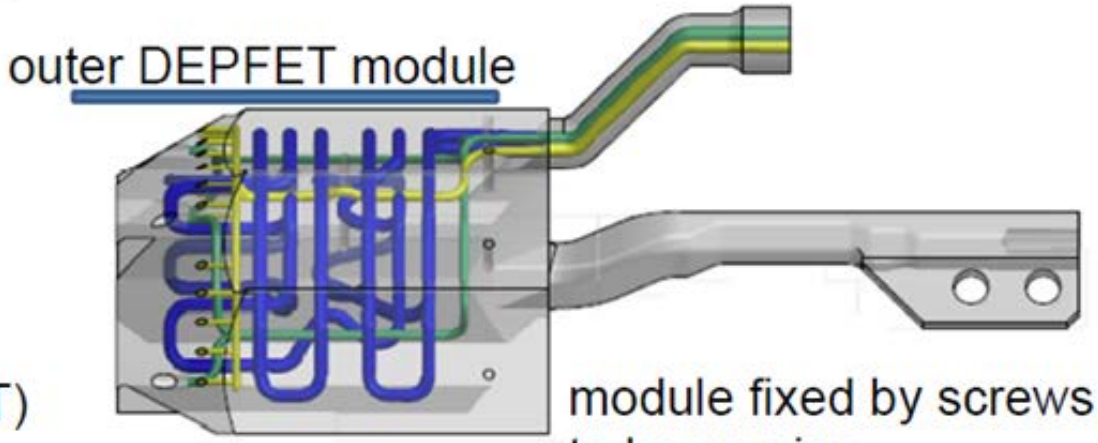


Cooling Issues





material non-magnetic INOX



design: MPI
manufactured by Fruth
Innovative Technology (FIT)

module fixed by screws
to beam pipe