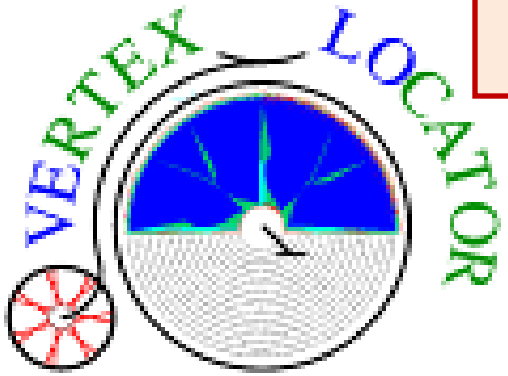
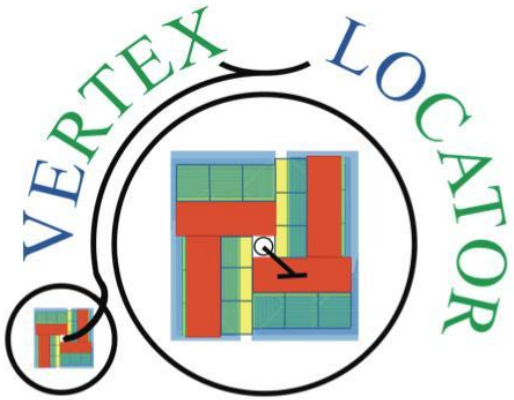


Upgrade of the LHCb Vertex Locator



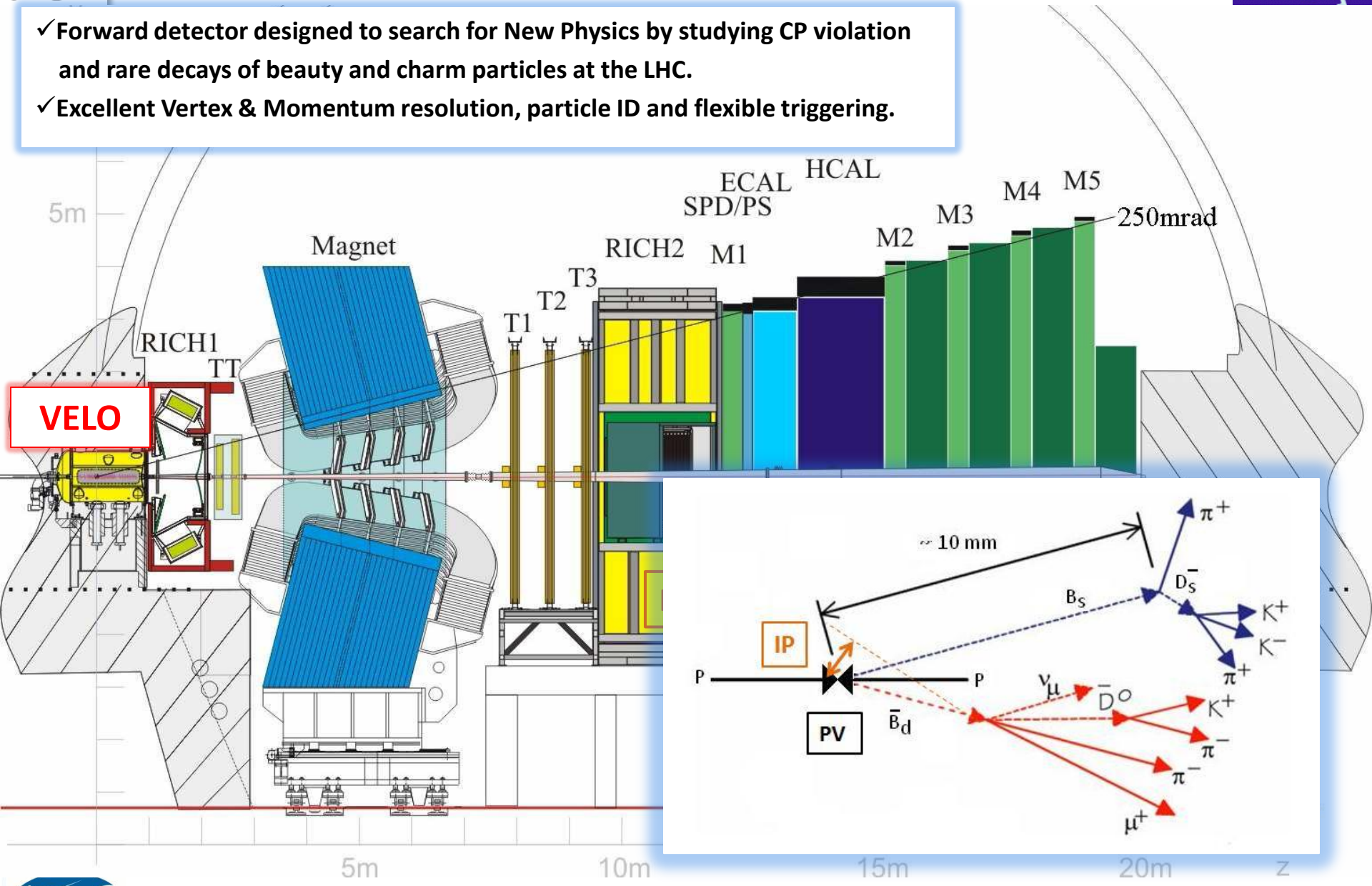
Alexander Leflat - SINP MSU
On behalf of the LHCb VELO Upgrade Group

Contents

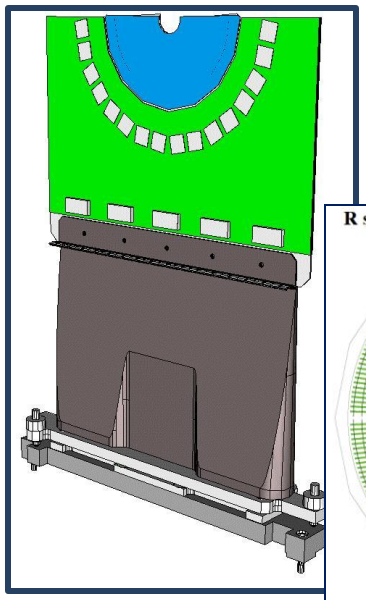
- Introduction to LHCb detector
- Brief VELO Overview
- Upgrade motivation and challenge
- Upgrade in details, R&D
  - Sensors
  - Modules
  - ASIC
  - Data acquisition
  - Cooling
  - RF Box
- Timetable
- Summary

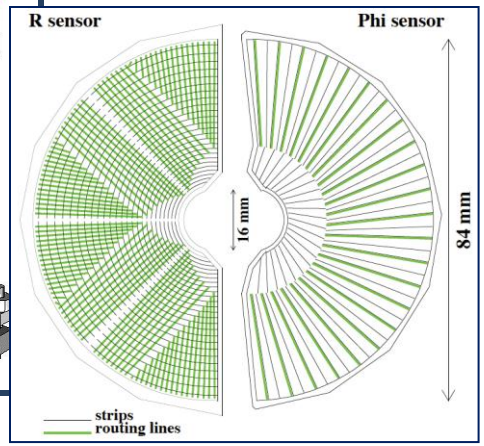
Introduction to LHCb detector

- ✓**Forward detector designed to search for New Physics by studying CP violation and rare decays of beauty and charm particles at the LHC.**
- ✓**Excellent Vertex & Momentum resolution, particle ID and flexible triggering.**



VELO Detector Overview





SENSORS

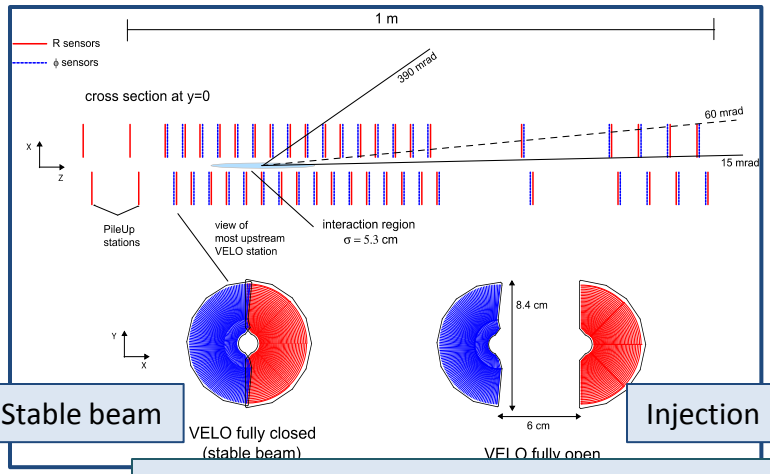
- 300 µm Silicon 42 R and 42 Φ sensors, 2048 strips.
- Active area at 8.2 mm from Beam line.
- Certified up to 700 V Bias voltage.

FE chip Beetle:

- 128 analogue readout channels.
- 40 MHz clock, 1 MHz readout.
- Peaking time < 25 ns.
- S/N = 20.
- Radiation hardness > 10 Mrad.

! Talk by Tim Head , Performance and Radiation Damage Effects in the LHCb Vertex Locator

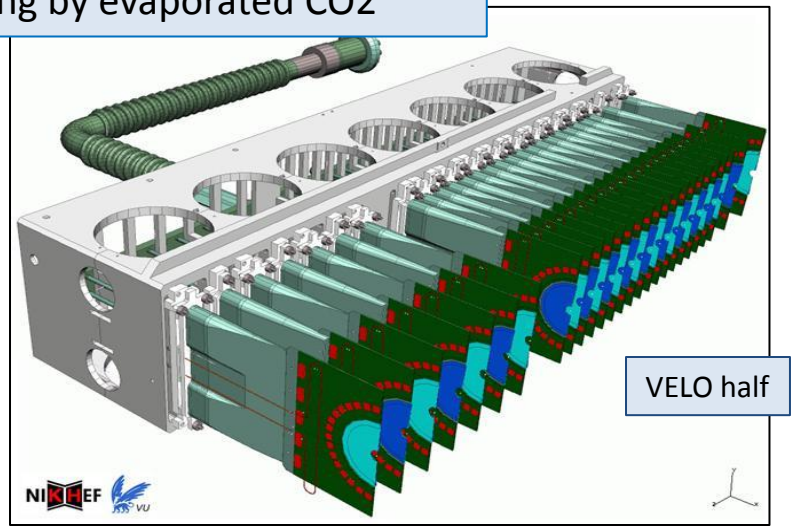
✓ Operation in secondary Vacuum
✓ Corrugated RF foil
✓ Cooling by evaporated CO2



Stable beam

Injection

✓Centers around the beam every fill

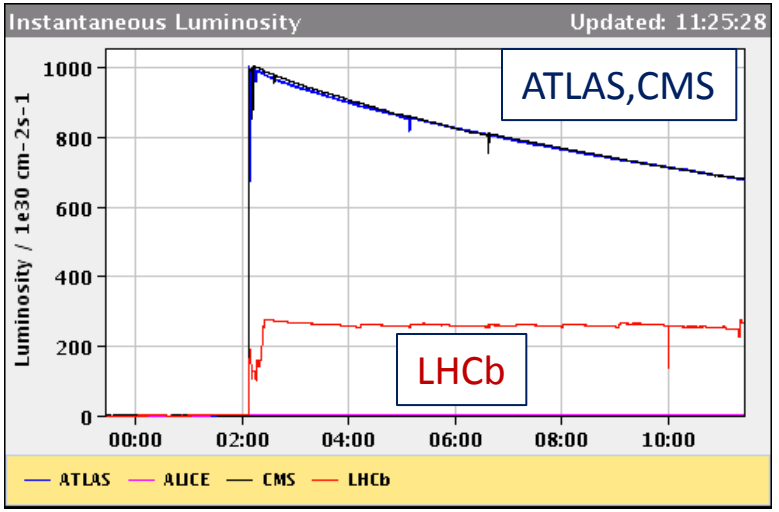


VELO half

Upgrade motivation and challenge

Physics goal:
No deviation observed from the Standard Model ,
more statistics need.

✓LHCb runs at ~20% of ATLAS & CMS Luminosity, may accept more from LHC.
✓LHCb runs at double Luminosity as been designed.



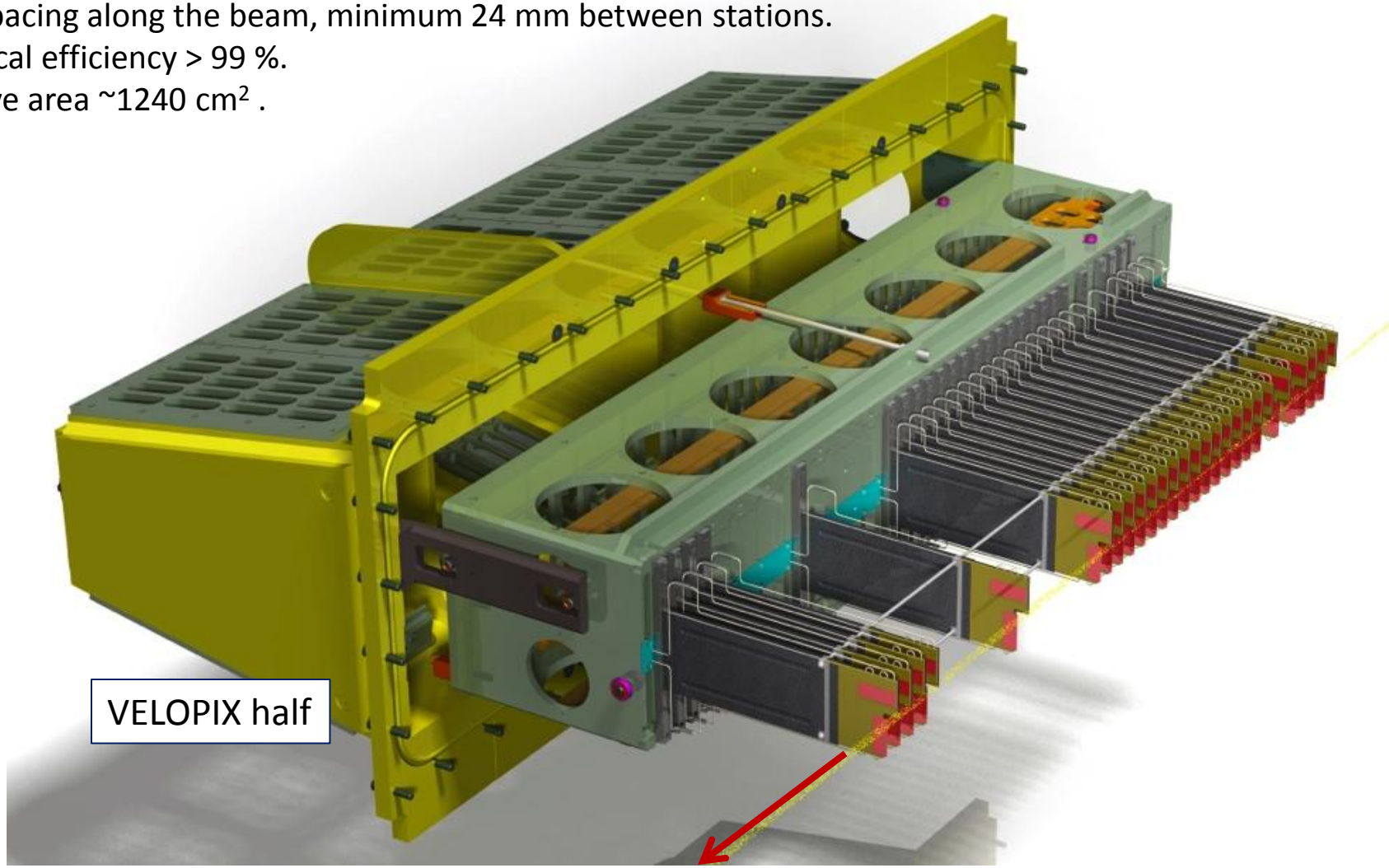
As part of LHCb tracker the VELO should be modified to cope with Luminosity 2×10^{33} cm^{-2} s^{-1}

- Readout whole detector at 40 MHz clock every bunch crossing, 25 ns
- Fully software trigger, no L0 trigger
- Completely new Front End ASIC
- Pixels instead of strips, give faster pattern recognition
- Active area at 5.1 mm from Beam line
- New microchannel cooling system
- New thinned RF foil
- Radiation hardness up to 400 Mrad (10 years)

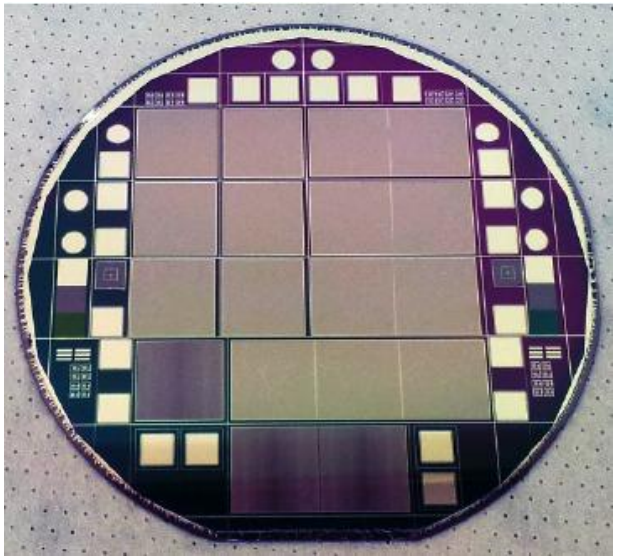
All these points should provide the desired resolution and tracking as well as the necessary data rate

VELOPIX, general view

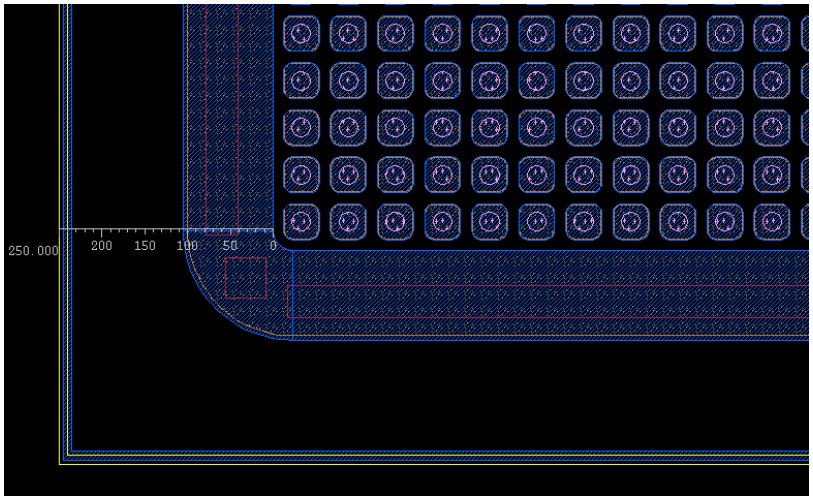
- ✓ Full detector consists of 26 stations.
- ✓ Station consists of two L-shape modules, one on each side of the beam.
- ✓ Varying spacing along the beam, minimum 24 mm between stations.
- ✓ Geometrical efficiency > 99 %.
- ✓ Total active area ~1240 cm^2 .

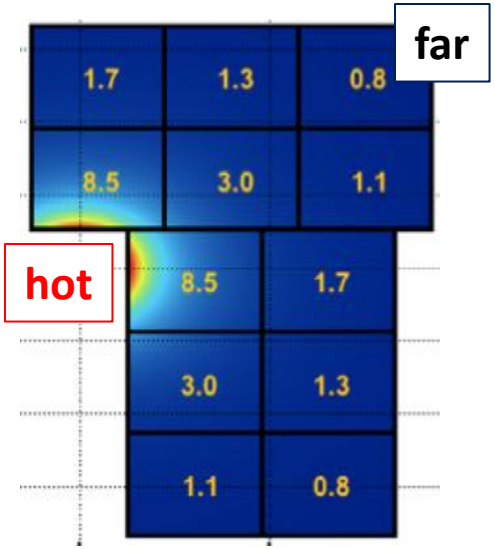


Upgrade in details I, Sensors

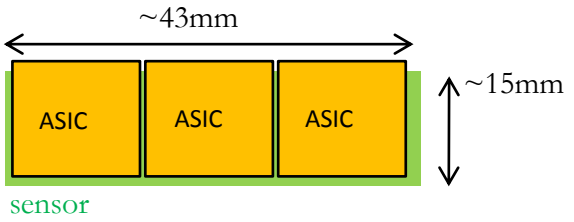


- ✓ Planar Silicon n-in-n or n-in-p.
- ✓ 200 micron thickness.
- ✓ Tile for 3 VeloPix chips: ~ 43 x 14 mm
- ✓ 55 x 55 micron pixel size.
- ✓ Non homogeneous design of Guard rings:
  - Fluence difference factor of ~40 on hot and on far ends.
  - Bias Voltage ~1000V at the end of lifetime, 50 fb^{-1}
  - Guard ring width ~450 micron.
- ✓ Possible vendors – Micron/Hamamatsu



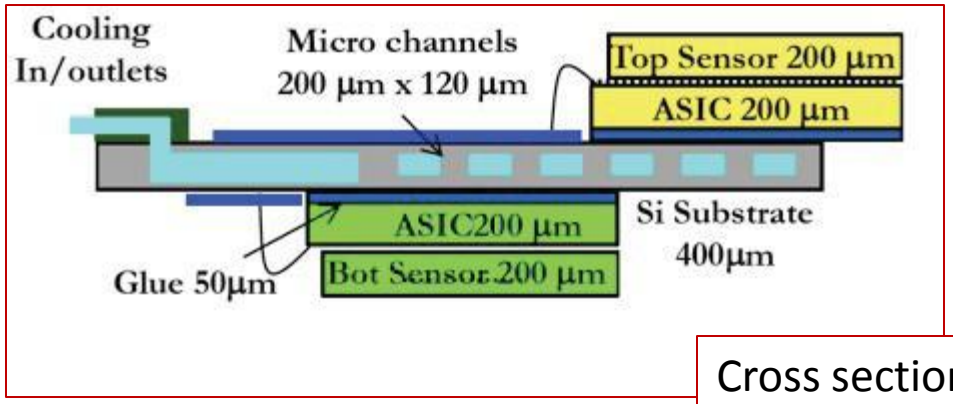


Upgrade in details II, Modules

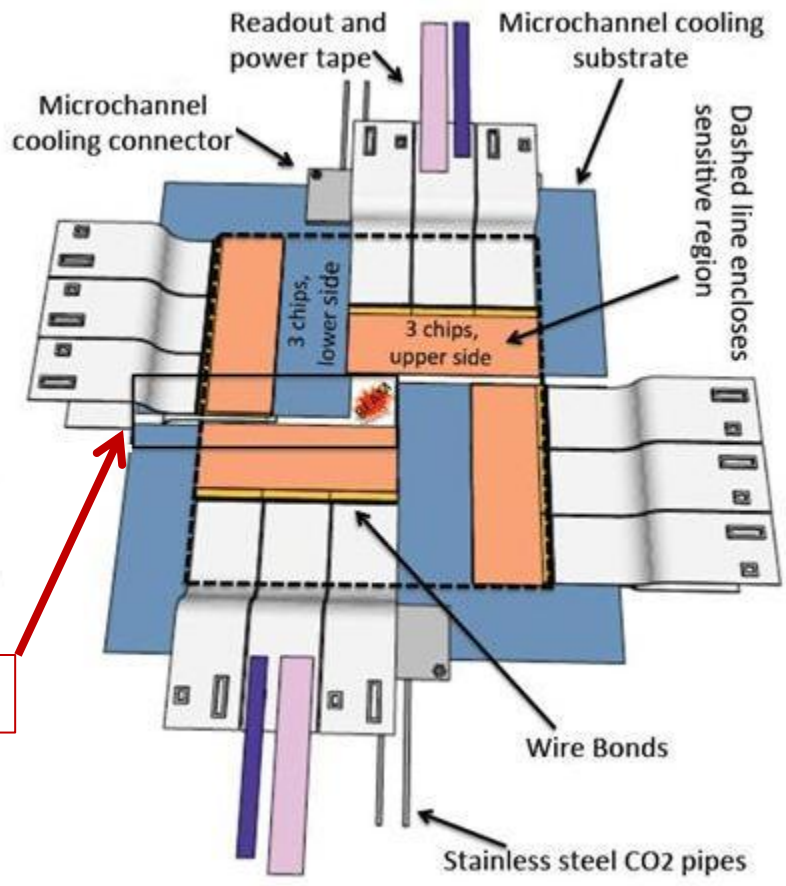


- ✓ 24 ASIC mounted on two L-shape modules.
- ✓ Four sensor tiles, two on each sides of substrate.
- ✓ Power and Readout traces on Kapton flex.
- ✓ Silicon substrate with etched micro-channels for evaporated CO2 cooling.

41 Megapixels in total.



Cross section



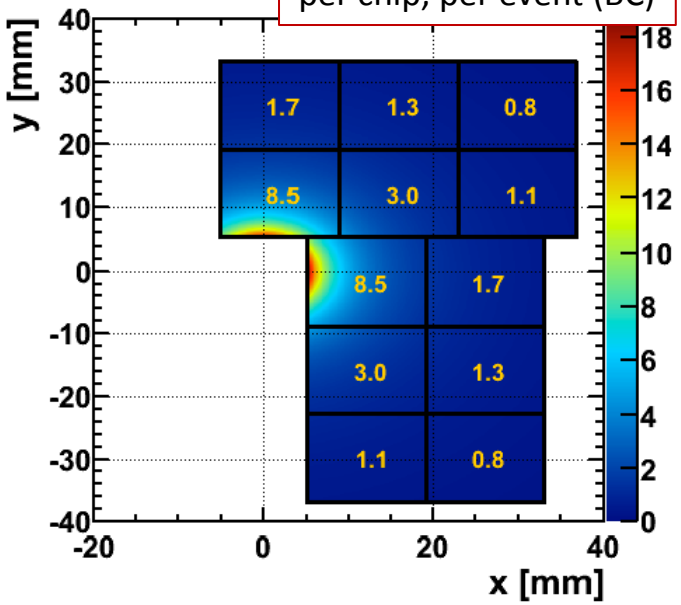
Upgrade in details III, ASIC

- ✓ New **VeloPix** ASIC based on the Medipix family (TimePix, TimePix3).
- ✓ TimePix3 ASIC is used as prototype for Beam tests by VELO group.
- ✓ VeloPix designed by CERN medipix group and Nikhef.
- ✓ Matrix of 256 x 256 pixels , ~14 x 14 mm^2 active area.
- ✓ 130 nm CMOS technology, radiation hardness up to 400 MRad.
- ✓ First submission in summer 2014, production in 2015.

VeloPix features:

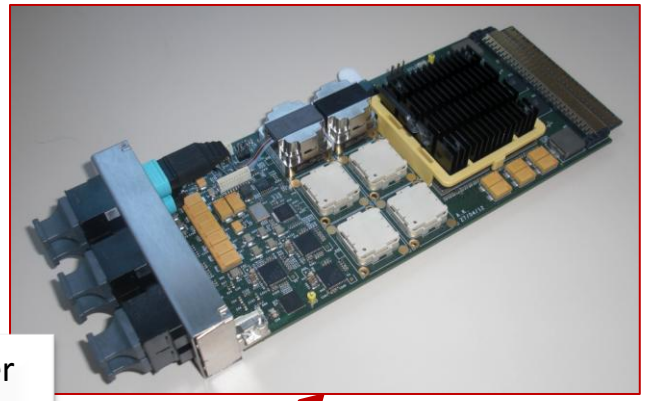
- Data driven readout, hits immediately transferred to the output.
- [4 x 2] pixels with fixed boundaries compose Super-pixel to reduce the data volume. Typical cluster size is 2-4, removes duplicated address and timestamp.
- Time stamp and label of output data (BCID).
- Binary readout.
- Time-of-Arrival and Time-over-Threshold measurements, all hits are ToA, but ToT available at low rate.
- Output bandwidth 13 Gbit/s; 4 links @ 5 Gbit/s.
- Zero suppressed data.
- Fast front-end: Timewalk < 25 ns.
- Power dissipation < 3 Watts per chip @ 1.5V (1.5 W/cm^2).
- Expected threshold ~1000 e-.

Average number of hits per chip, per event (BC)



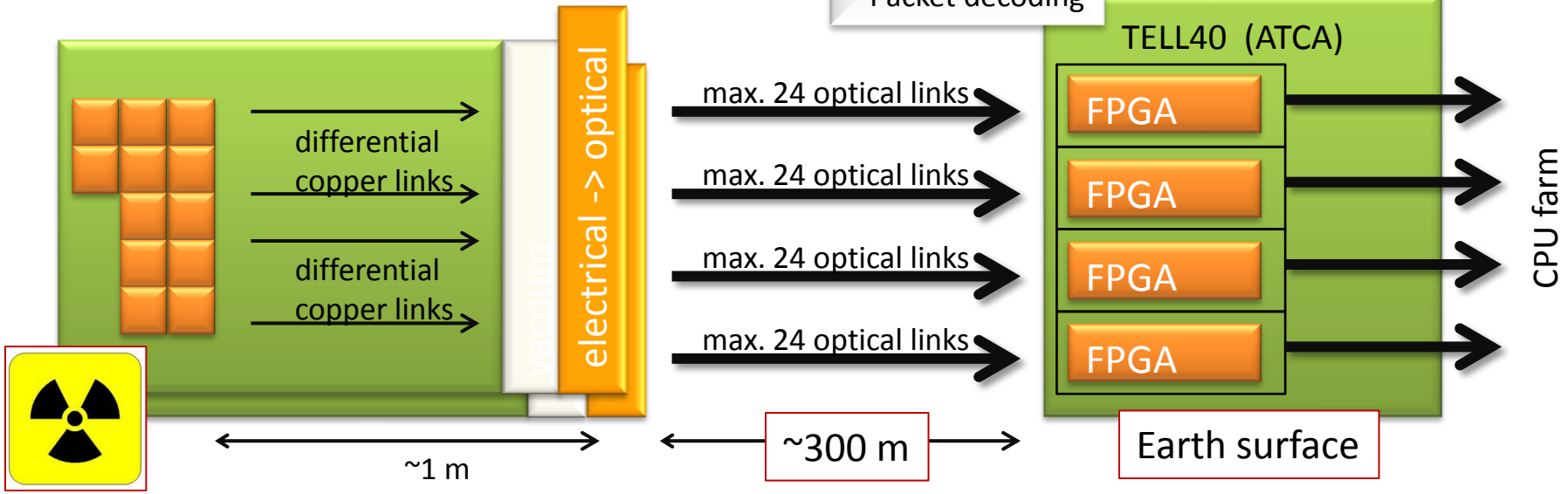
Upgrade in details IV, Data acquisition

- ✓ Differential copper link from ISIC (Kapton ~1 m) inside of vacuum tank .
- ✓ Vacuum feed through.
- ✓ Electrical to optical conversion outside of vacuum tank.
- ✓ Optical link ~300 m long.
- ✓ 4 mezzanines with powerful FPGA (ALTERA, Stratix-V).
- ✓ DAQ module TELL40, common for LHCb, ATCA standard.
- ✓ 12 x 10 Gigabit Ethernet outputs.
- ✓ CPU farm.



Data flow of whole VELO ~ 2.5 Terabit/s

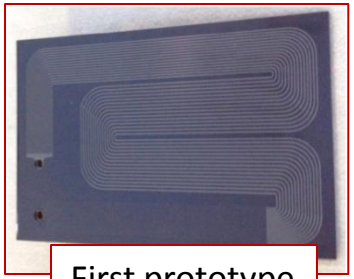
- Packet receiver
- Time ordering
- Event buffering
- Packet decoding



Upgrade in details V, Cooling

Key Fearures

- ✓ Method: evaporated CO_2 flow via **microchannels etched in Silicon substrate**.
- ✓ Bring the coolant directly to power dissipation areas .
- ✓ Keep the sensors at -20 °C to reduce the radiation damage.
- ✓ Good uniformity of material in sensitive region, **no CTE difference**. Less material.
- ✓ Channel cross section 200 x 120 μm^2
- ✓ Detectors in vacuum, hence leakage/breakage is a serious concern.

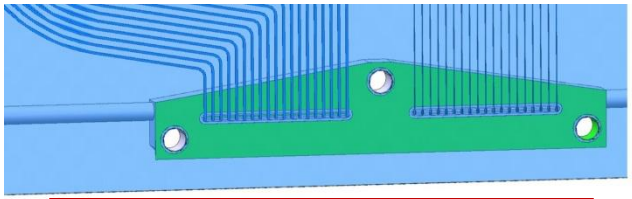


First prototype

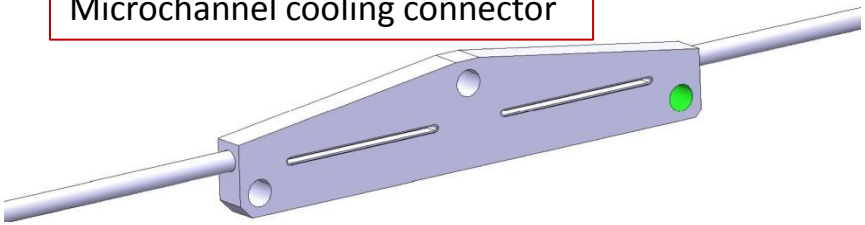
R & D started in summer 2012. After 1.5 year efforts we have **achieved**:

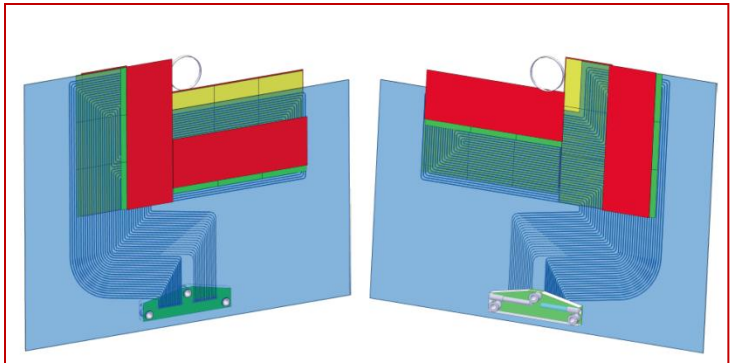
- ✓ Required operational pressure ~15 Bar at -30 °C, and ~60 Bar at room temperature.
- ✓ Withstand on safety limits of 150 Bar.
- ✓ Stress test of samples at ~700 Bar.
- ✓ Thermal and pressure cycling long term tests (-40 .. +40 °C, 0 .. 200 Bar).

Looks promising



Microchannel cooling connector

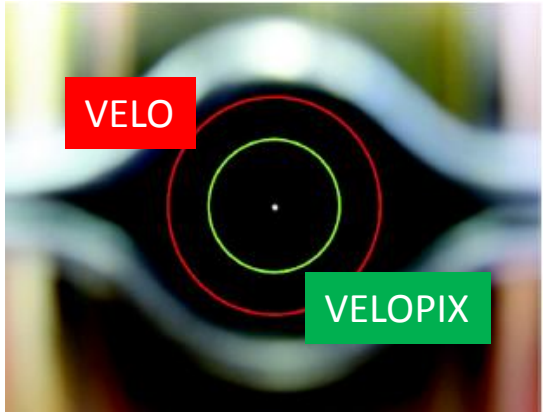




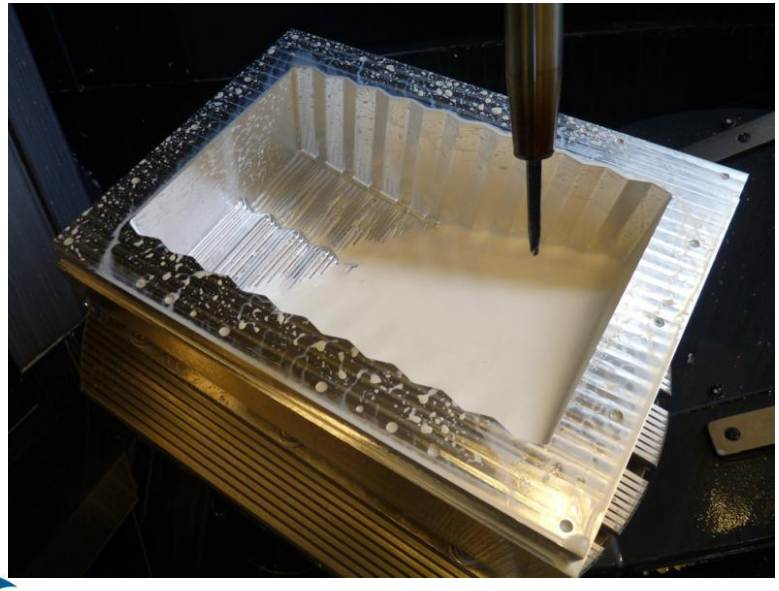
Microchannel Silicon substrates

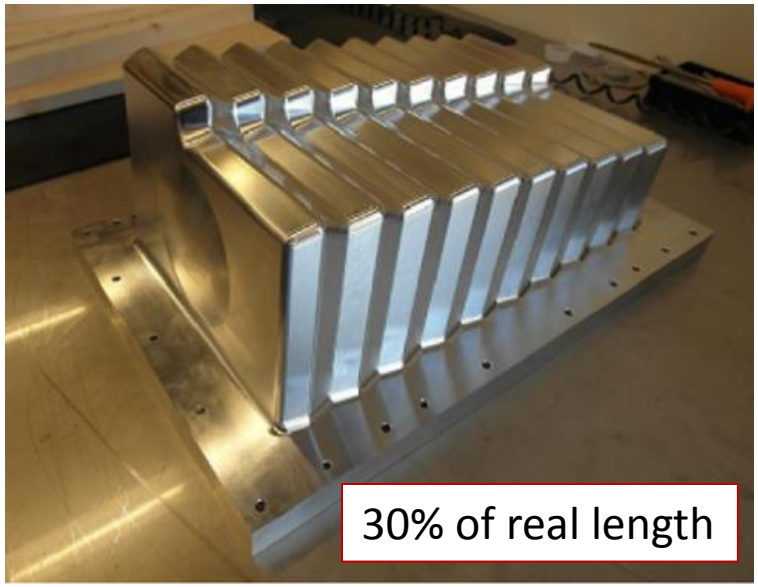
Upgrade in details VI, RF Box

Requirements:
- ✓ Separates Accelerator (10^{-9} mbar) and VELO (10^{-7} mbar) vacua.
- ✓ Vacuum tight, leakage < 10^{-9} mbar l/s.
- ✓ Electrically conductive: guides beam mirror current.
- ✓ Low mass: located at R=3.5 mm from beam line.
- ✓ Thermally stable and thermally conductive.



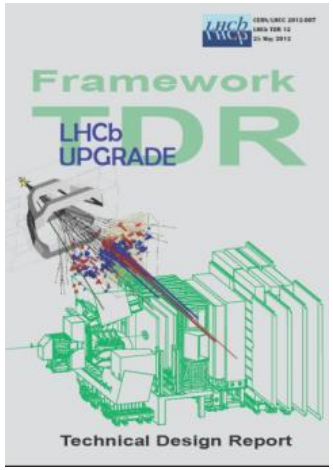
Material and fabrication:
- ✓ Aluminum (AlBeMet) <300 μm thick top foil, 500 μm thick walls.
- ✓ Milled from solid block of Aluminum.
- ✓ Local chemical thinning with NaOH after milling, *under discussion*.





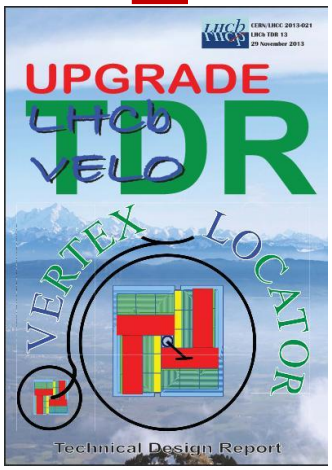
Timetable

Beam Crossing	50 ns			-		25 ns			-		25 ns		
Start up	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022+
√s (TeV):	0.9 - 7		8	LS 1		13 - 14			LS 2				
$\mathcal{L}$ Instant	10^{32}	$3 – 4 \times 10^{32}$				4×10^{32}				LHCb Upgrade	$10 – 20 \times 10^{32}$		
$\mathcal{L}$ Integrated	$3\ fb^{-1}$					$5 - 7\ fb^{-1}$					$> 50\ fb^{-1}$		



http://cds.cern.ch/record/1443882/files/LHCB-TDR-012.pdf

http://cds.cern.ch/record/1333091/files/LHCC-I-018.pdf



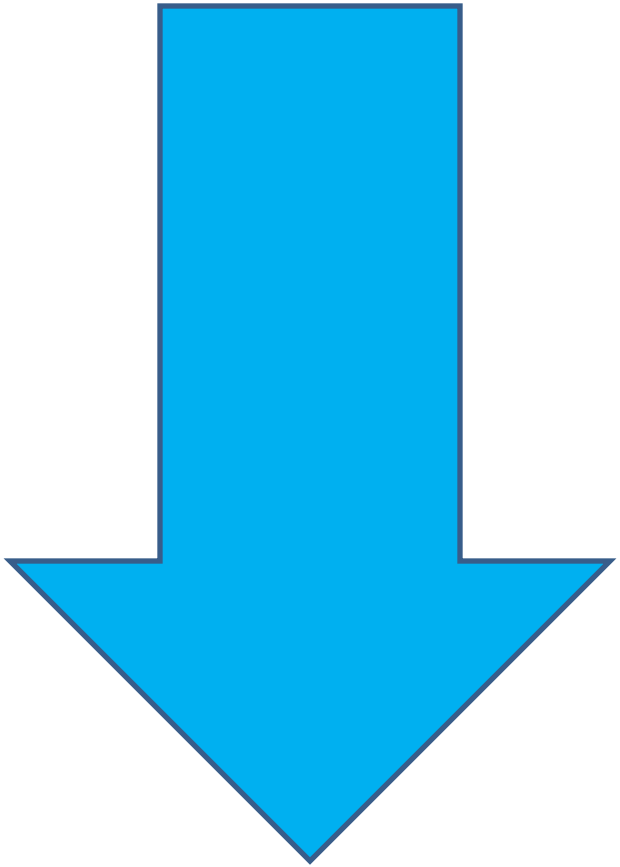
http://cds.cern.ch/record/1624070/files/LHCB-TDR-013.pdf

SUMMARY

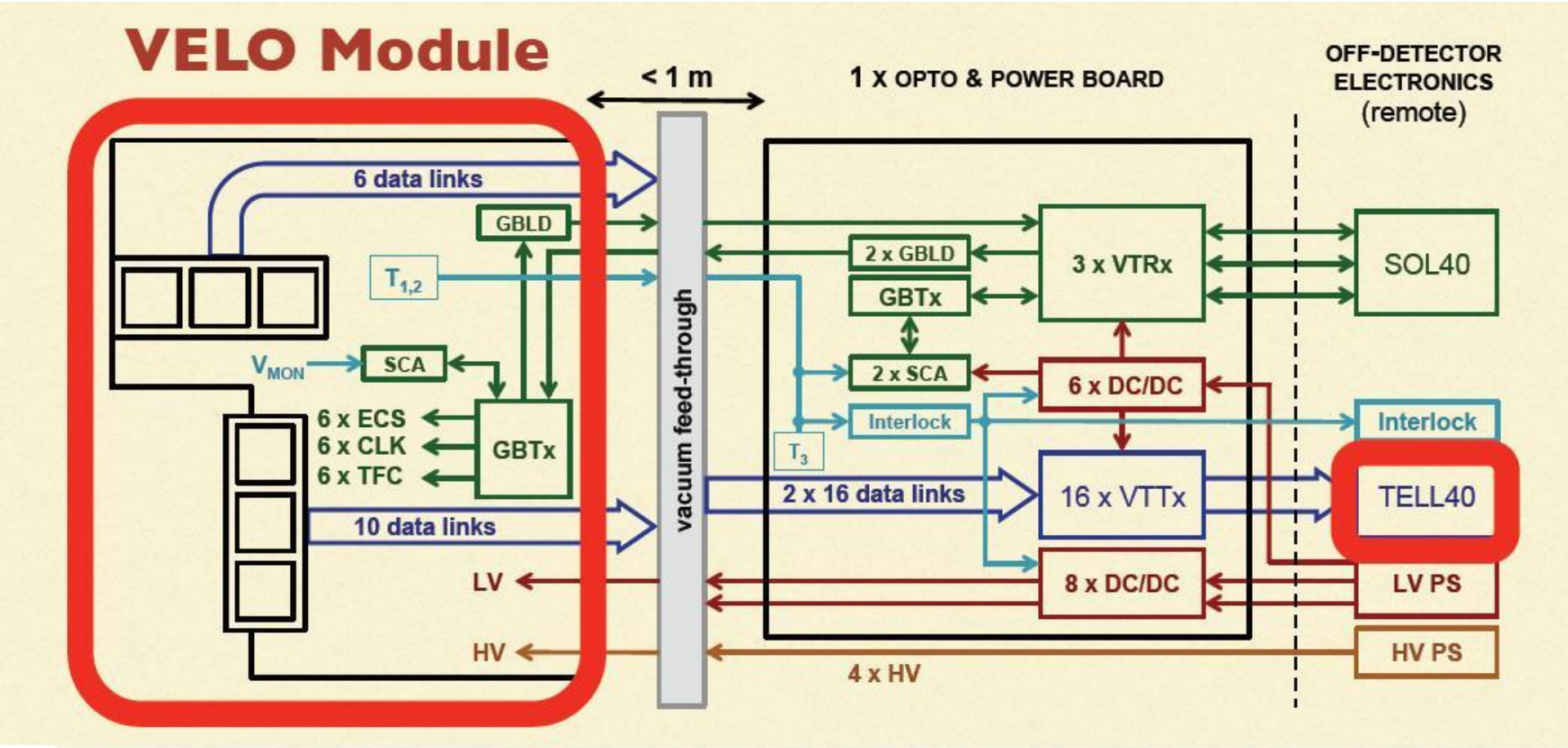
- VELOPIX installation in 2019
- Luminosity 2 x 10^{33} (factor of 5 increase vs current VELO)
- No L0 trigger, all data to CPU farm
- Planar silicon pixels, 55 x 55 μm^2
- Active area at 5.1 mm from the beam
- Fluence at hot end of sensor 8x10^{15} MeV n_{eq} /cm^2
- VELOPIX ASIC based on Medipix Family, 130 nm CMOS
- Data flow: 20 Gbit/s output bandwidth per ASIC
- Evaporative CO_2 cooling in Silicon microchannel substrate
- 300 μm thick RF-box milled from solid block of Aluminum

Upgrade is going well and on schedule, many novel techniques

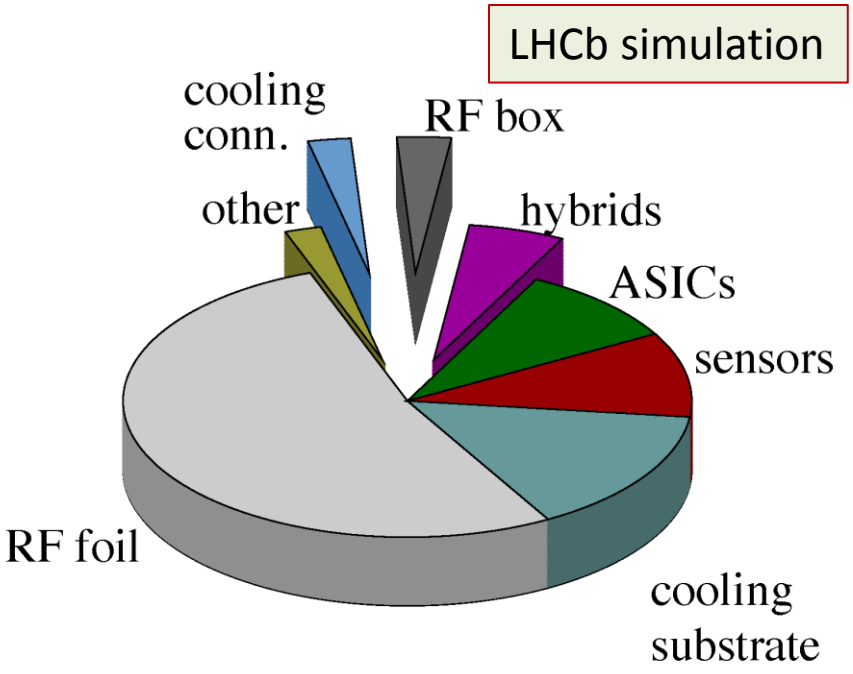
BACKUP



VELOPIX Electronics



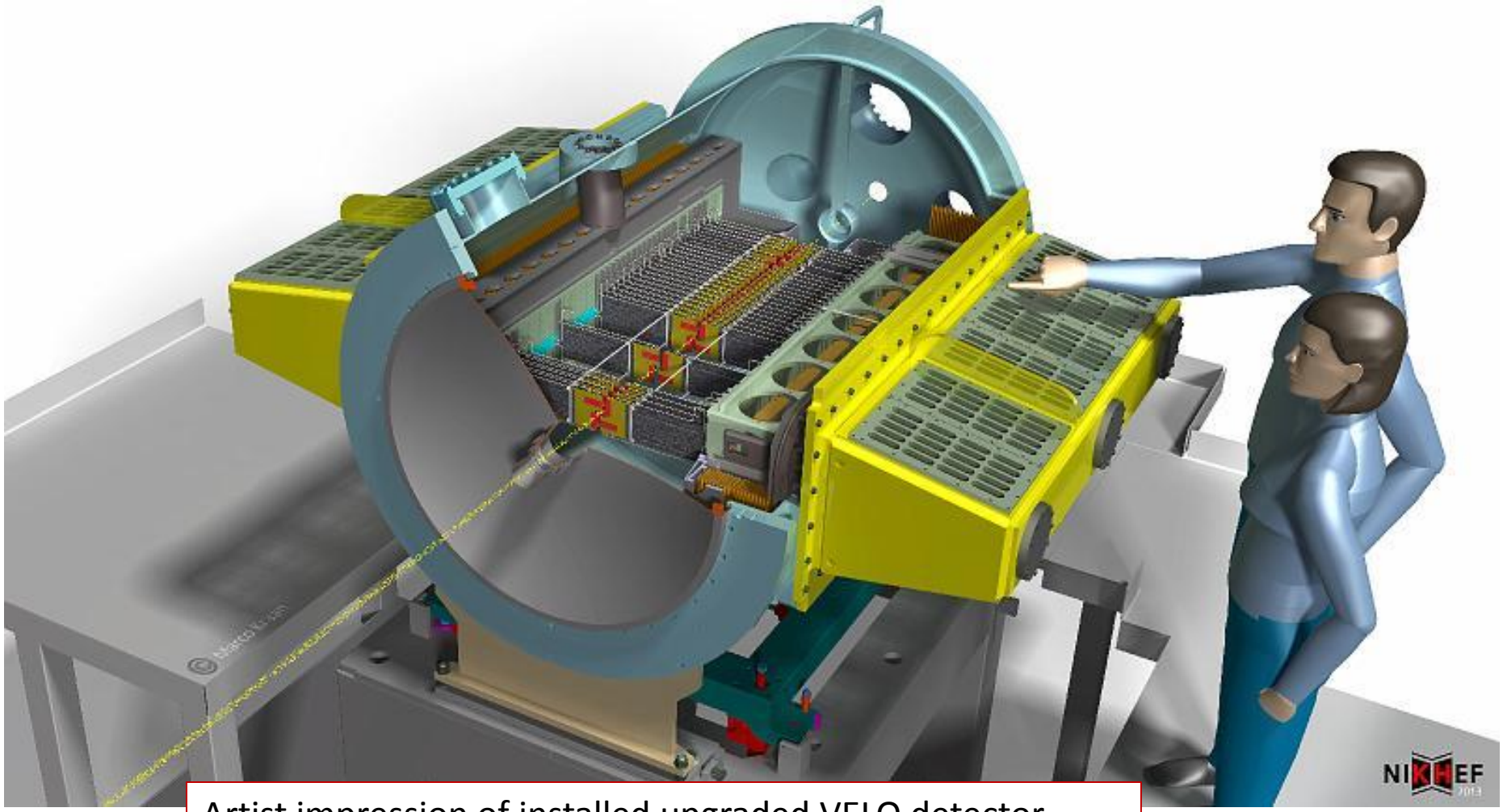
VELOPIX Material budget



total material: $21.3\%X_0$

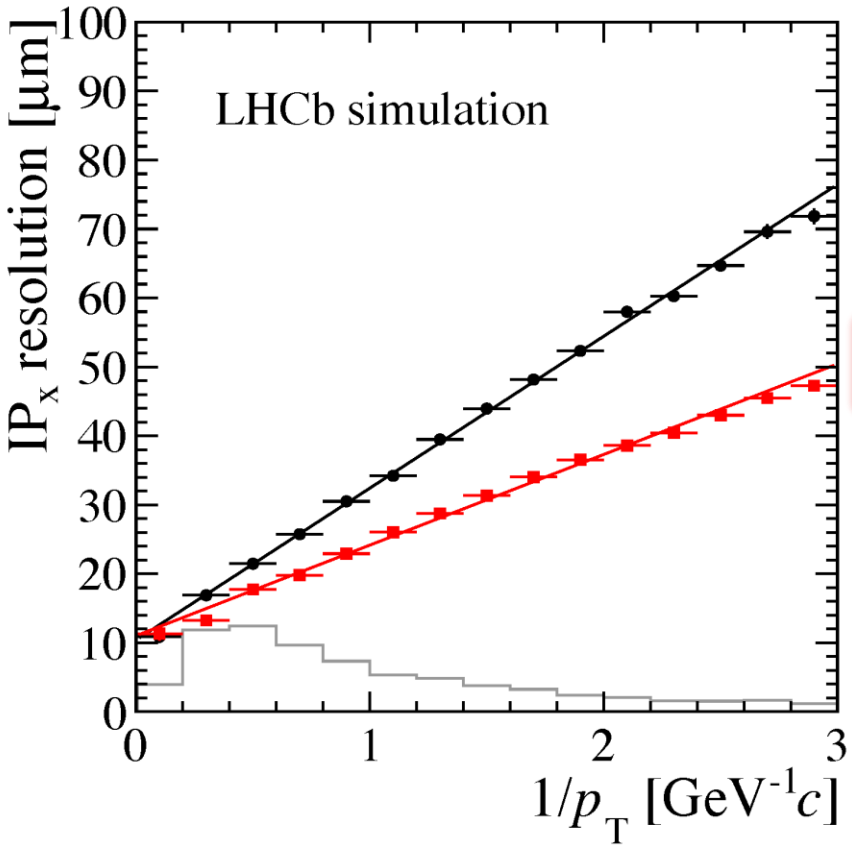
Total Material of Upgrade VELO as described in TDR

VELOPIX Artist Impression



Artist impression of installed upgraded VELO detector, produced by Nikhef Mechanical Engineering Department.

VELOPIX Expectations



Better

IPx resolution for long tracks for VELO Upgrade compared to expected performance of current VELO design in upgrade conditions, as described in TDR.