Performance of the ATLAS Tile Hadronic Calorimeter at LHC in Run I and planned upgrades

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on behalf of the ATLAS Tile Calorimeter

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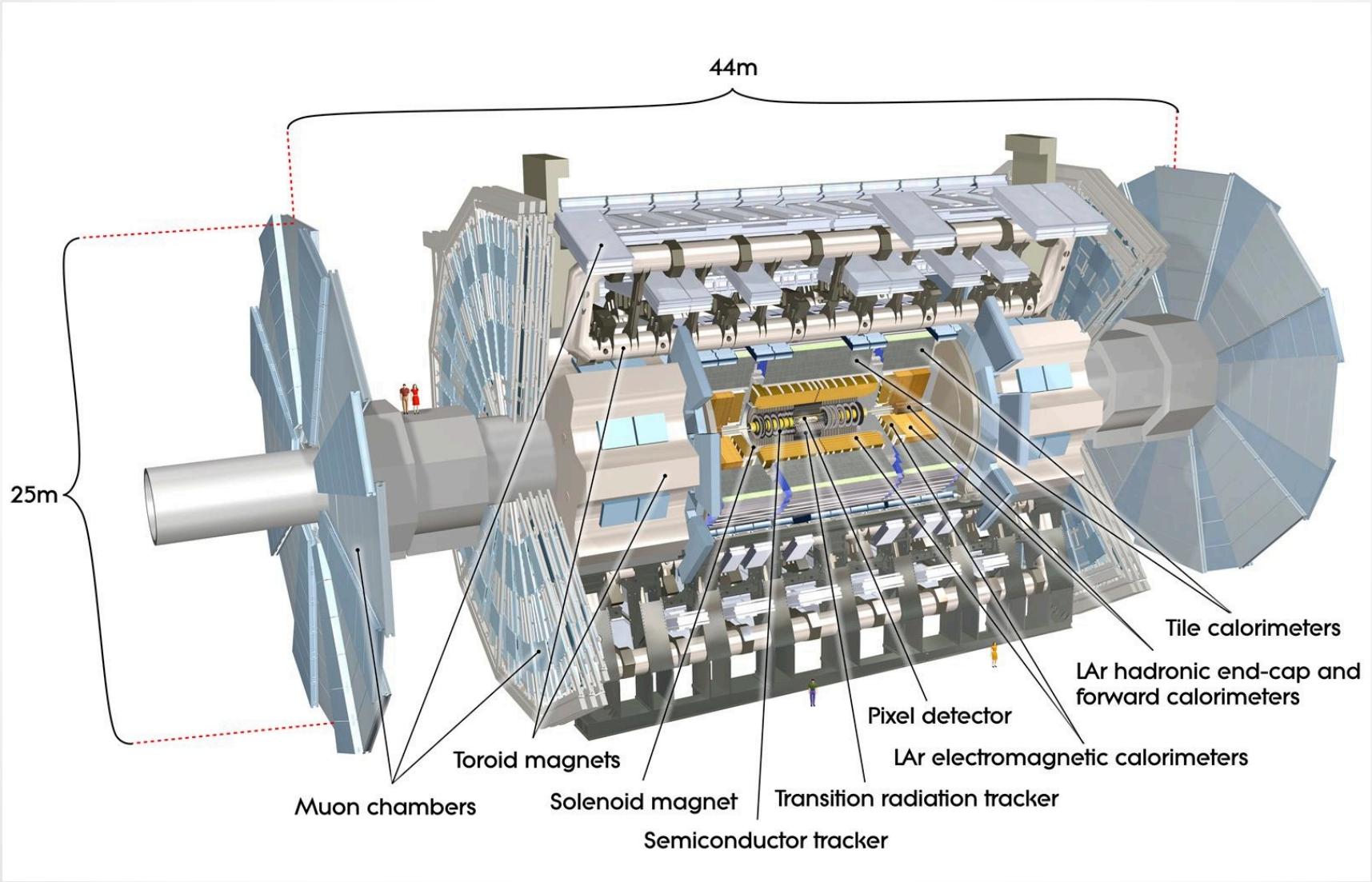
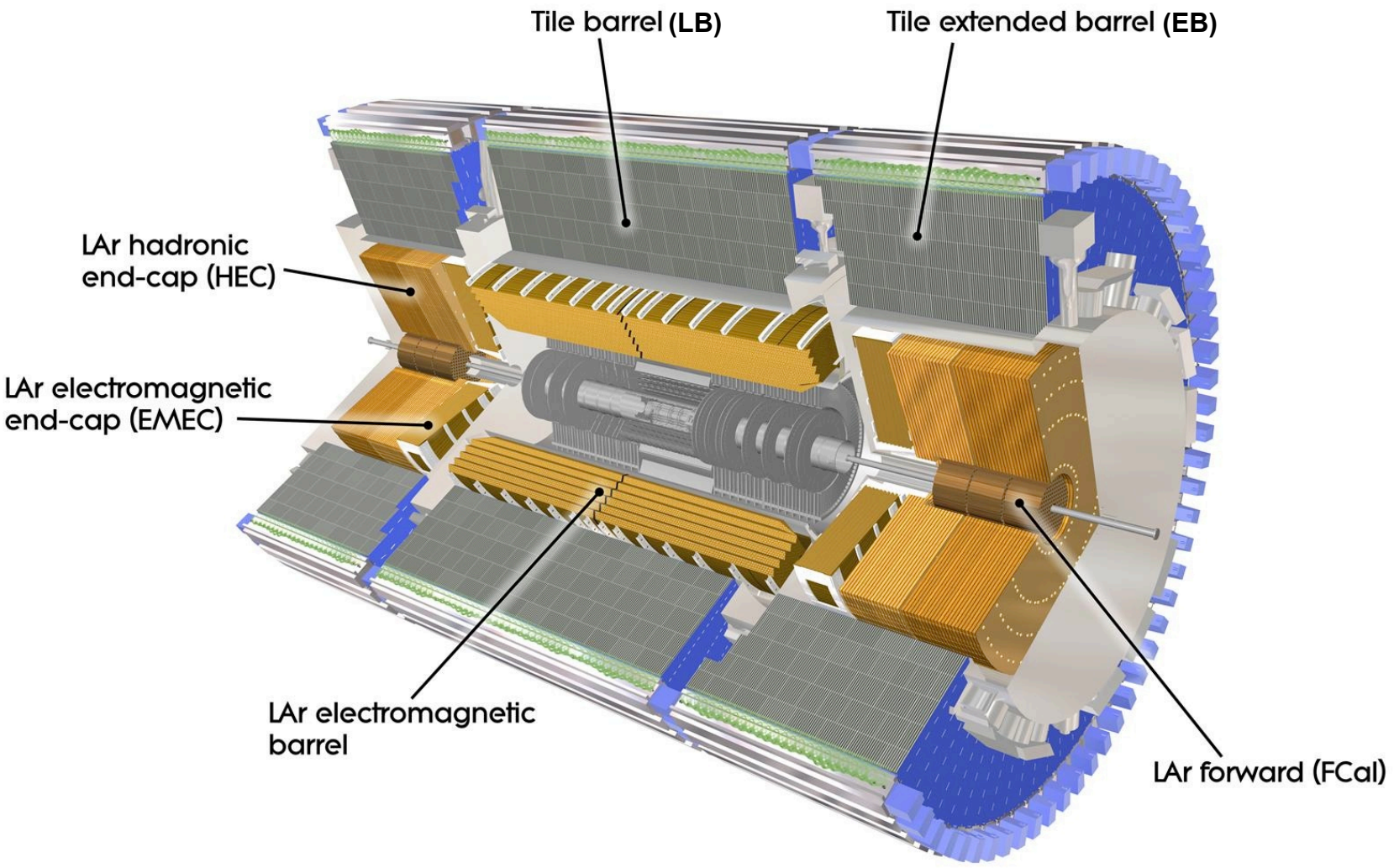
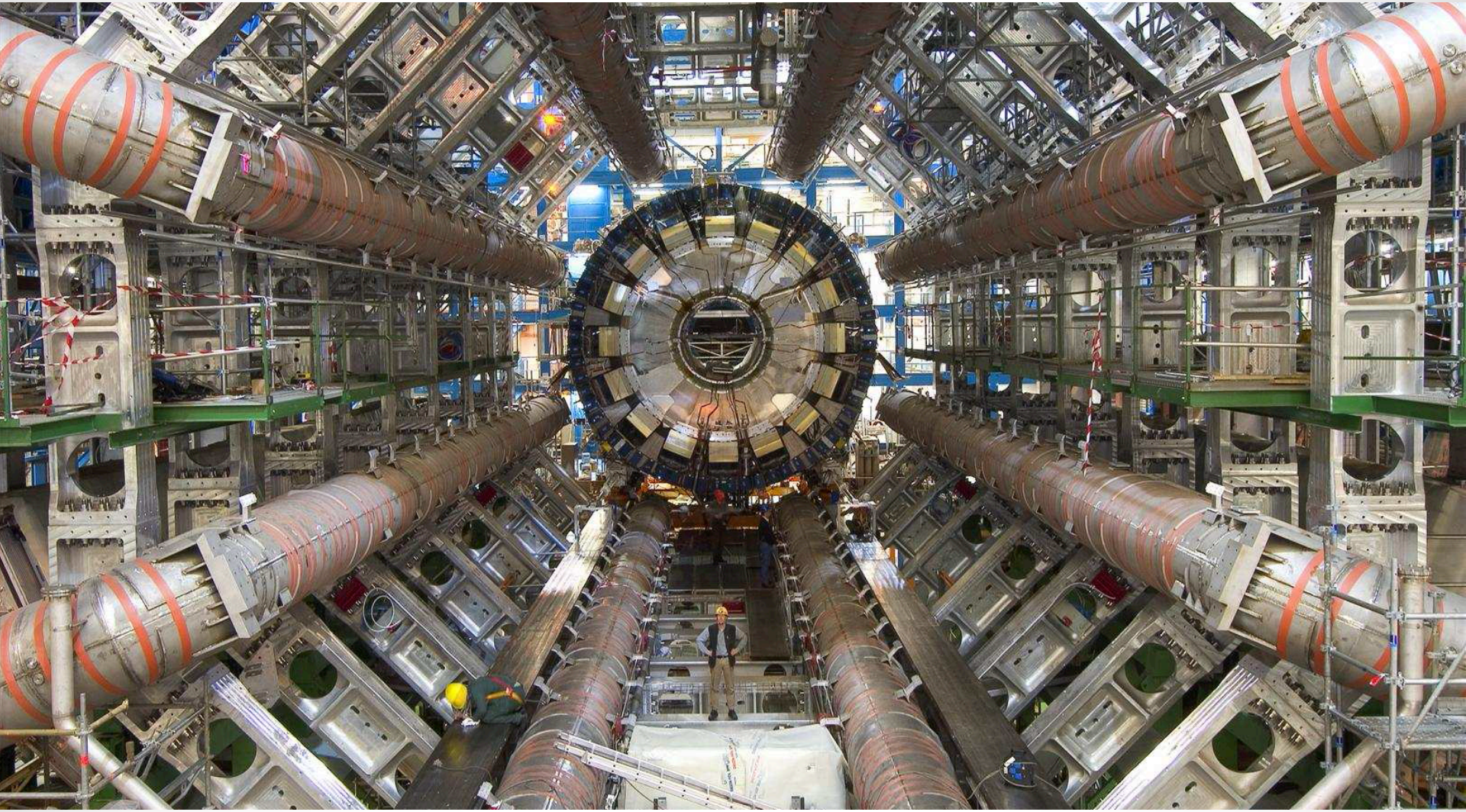
ATLAS Detector



ATLAS Calorimetry

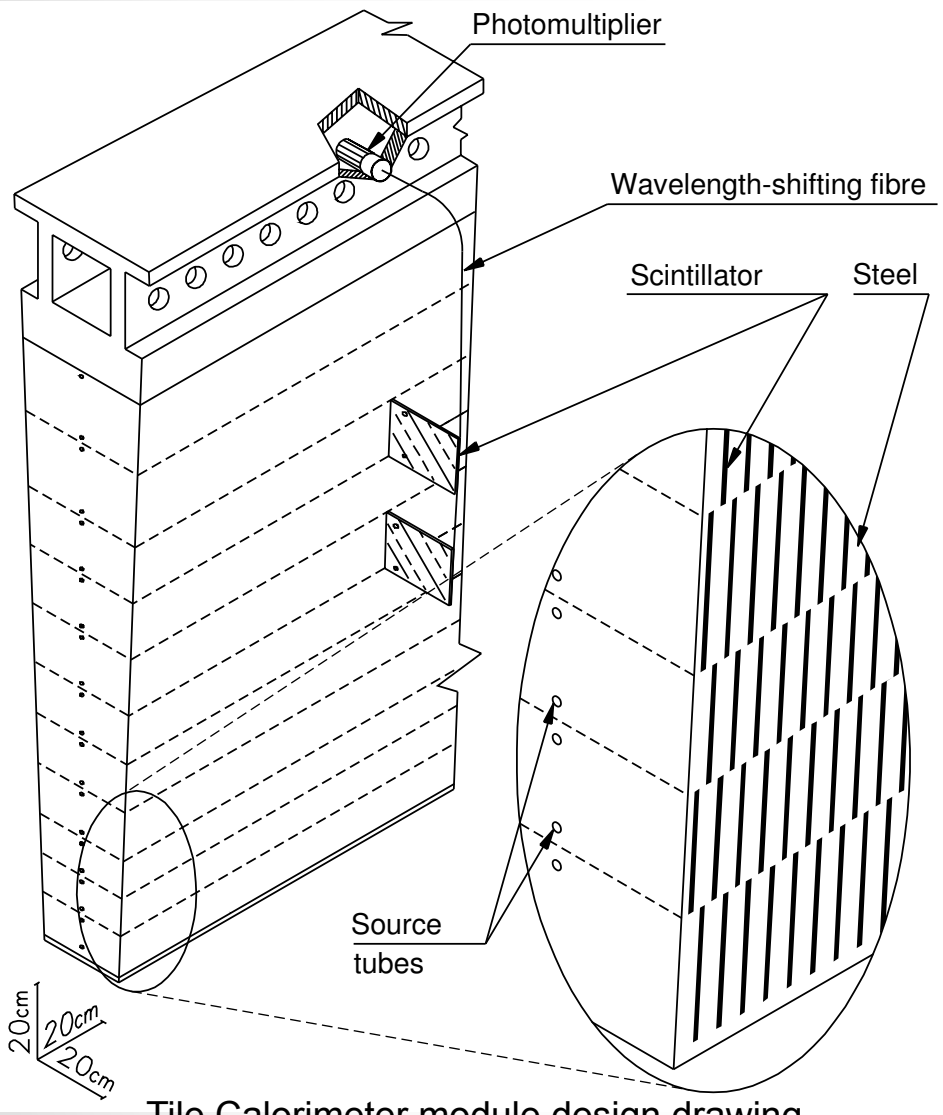


Calorimeter in the cavern



Barrel calorimeters moved to Z=0

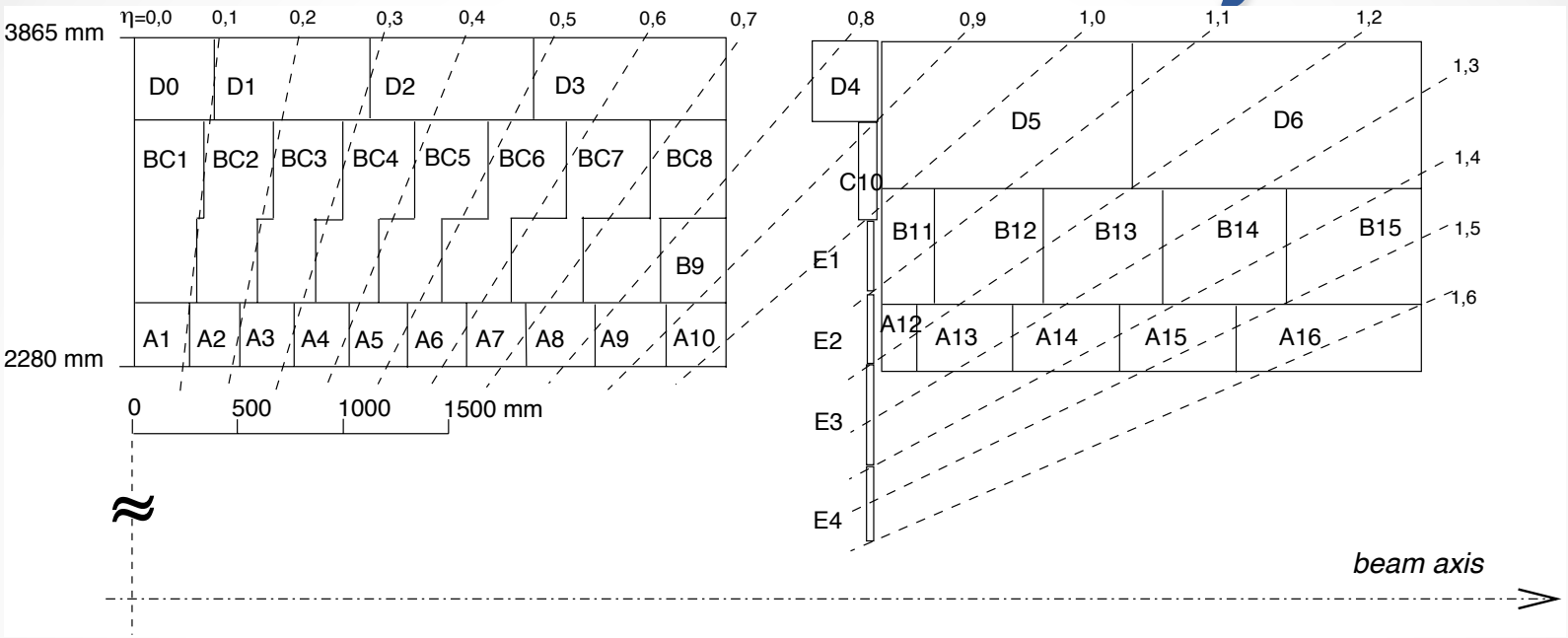
Tile Hadron Calorimeter



Tile Calorimeter module design drawing

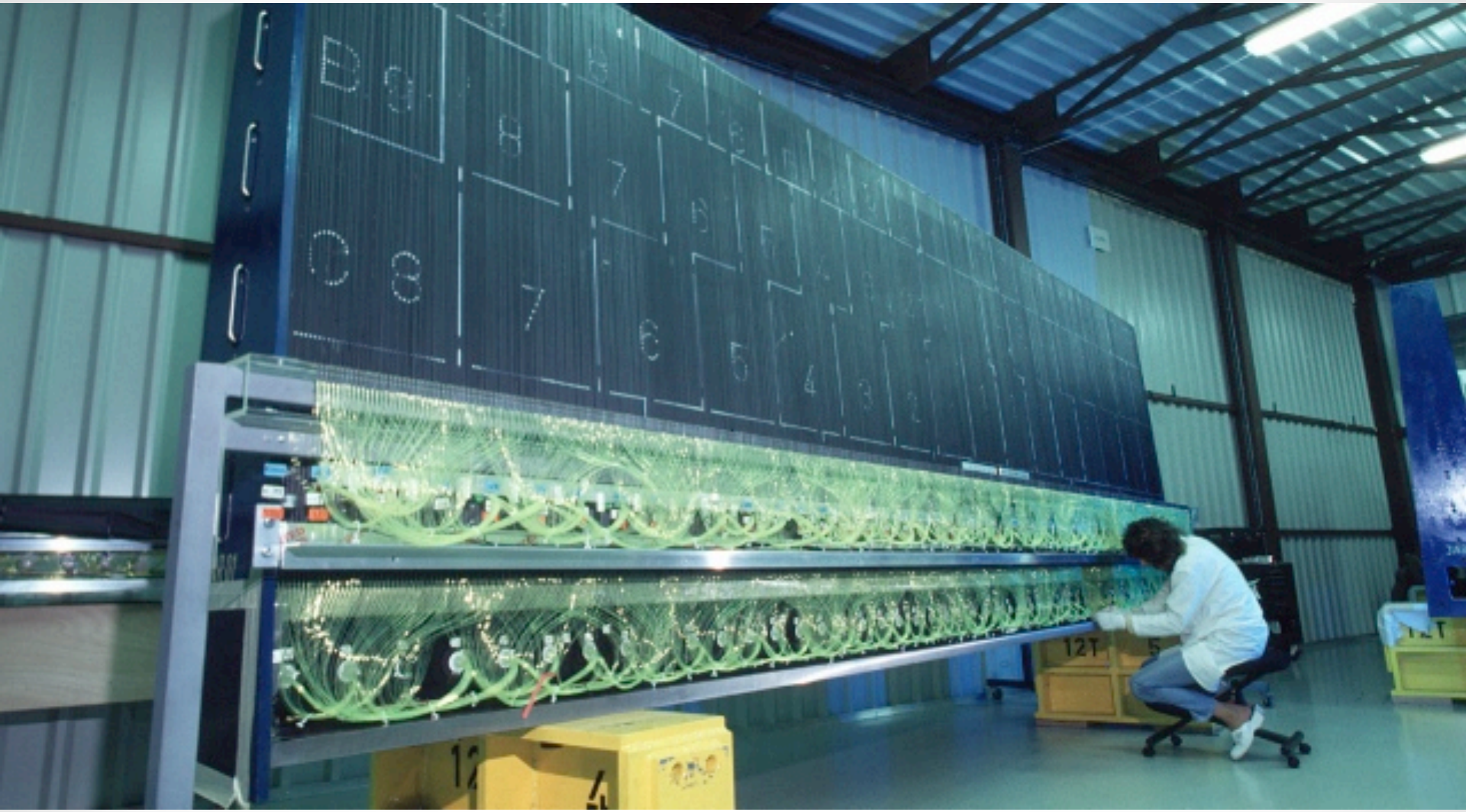
- Hadron non-compensating sampling calorimeter
  - Steel as radiator
  - Scintillating tiles as active medium
- 3 mm thick scintillating tiles (PSM, BASF polystyrene + dopants) oriented perpendicular to beam axis, wrapped in Tyvek paper
- Readout via green WLS fibres (Kuraray Y11) connected to both short edges of scintillating tiles
- Hamamatsu R7877 PMTs, located in a module's girder, collect light from the fibre bundles
- 3 cylinders: EB-A, LB, EB-C
- 64 modules in a cylinder
- One module weighs 22 tons (LB)

Calorimeter cell layout



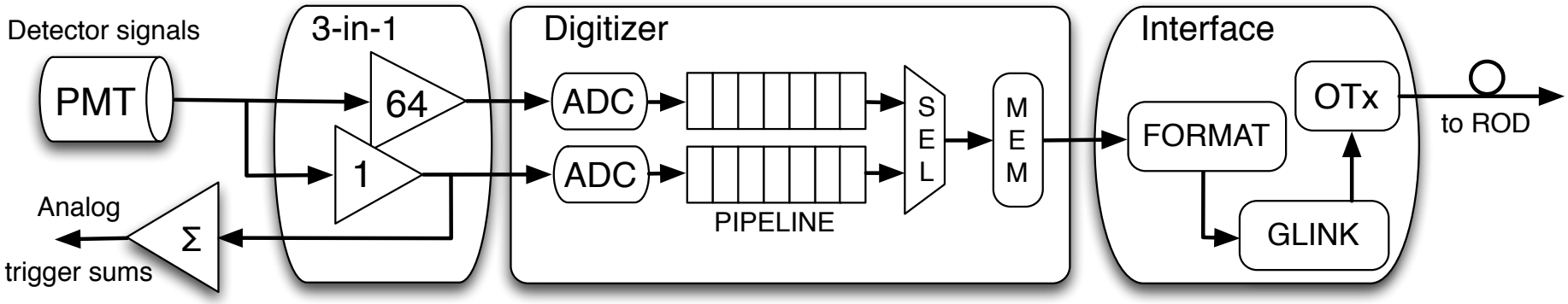
- Long barrel $|\eta|<1.0$, extended barrel $0.8<|\eta|<1.7$
- WLS fibre routing defines calorimeter cells
- 0.1x0.1 $\Delta\eta x\Delta\phi$ cell granularity (0.2x0.1 for D layer cells)
- Three longitudinal layers, total thickness of about 7λ
- Pseudo-projective towers for first level trigger
- Design resolution for jets $\Delta E/E = 50\%/\sqrt{E}+3\%$

Calorimeter module



Instrumentation of the Tile Calorimeter barrel modules

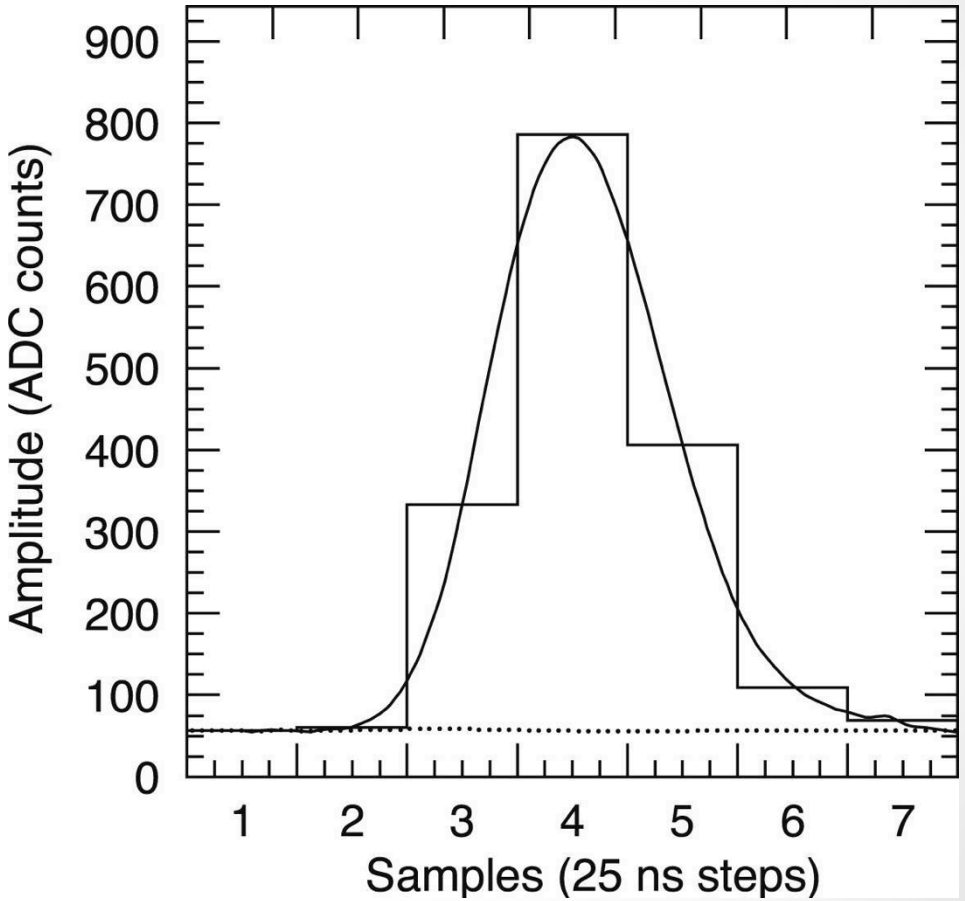
Front-end electronics



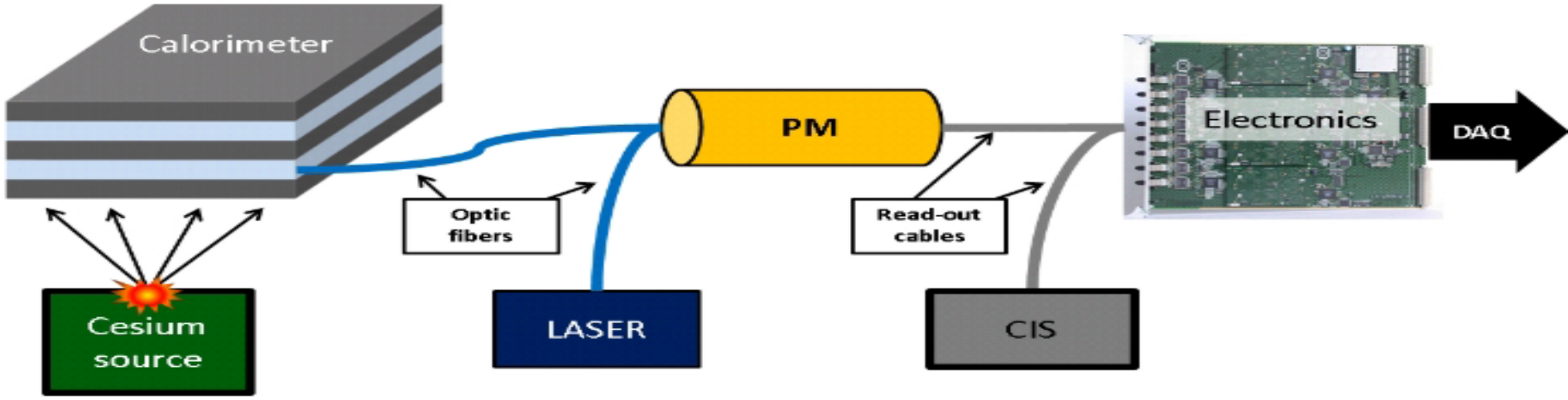
- PMTs signals are shaped and amplified with two gains (1:64)
- Analogue tower sums are provided for level one trigger
- Both gains are digitized in parallel by 40 MHz sampling 10-bit ADCs
- Digitised samples are temporary stored in pipeline memory
- Upon first level trigger decision the data of one of the gains are transferred to de-randomiser memory and then to the back-end electronics via readout fibres

Signal reconstruction

- Signal is reconstructed from 7 samples using optimal filtering
- Energy, time and quality factor are extracted from the sampled signal
- Amplitude of the signal is proportional to the energy (shaping)

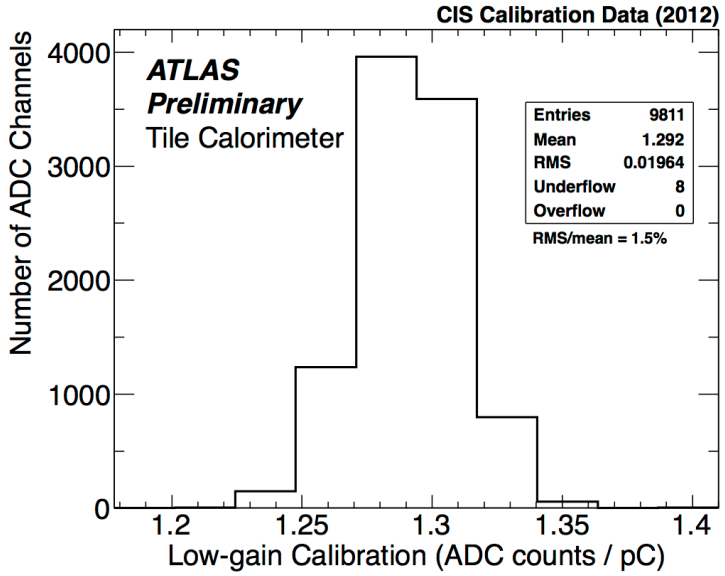


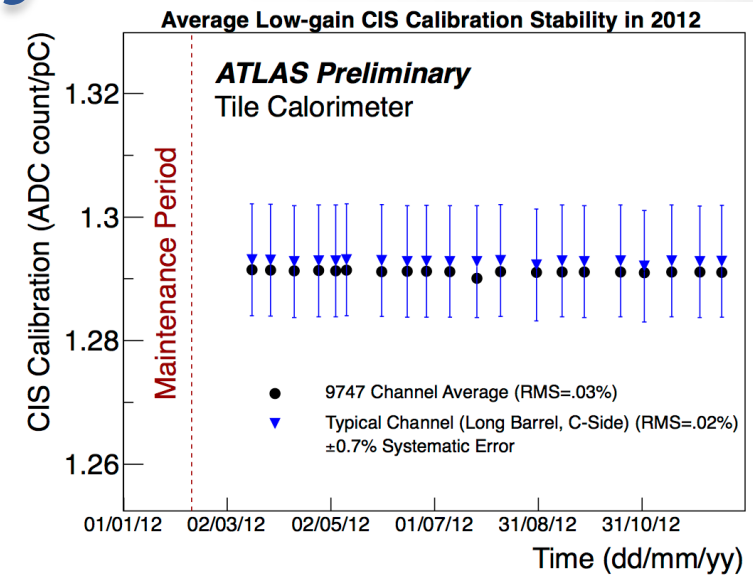
Calibration systems



- To provide correct energy and time for data reconstruction an elaborate chain of calibration systems has been conceived:
  - Charge inject system (CIS) to calibrate the response of the ADC
  - Laser calibration system to measure the performance of the PMTs
  - Cesium moving radioactive source system to calibrate the full optical path from scintillating tiles and WLS fibres down to integrated current of the PMT
  - Minimum bias monitoring system (MBM) to monitor the response of the calorimeter online
- About 11% of 192 Tile calorimeter modules were calibrated at the test beams and the EM scale was transferred to the final detector with the help of calibration systems

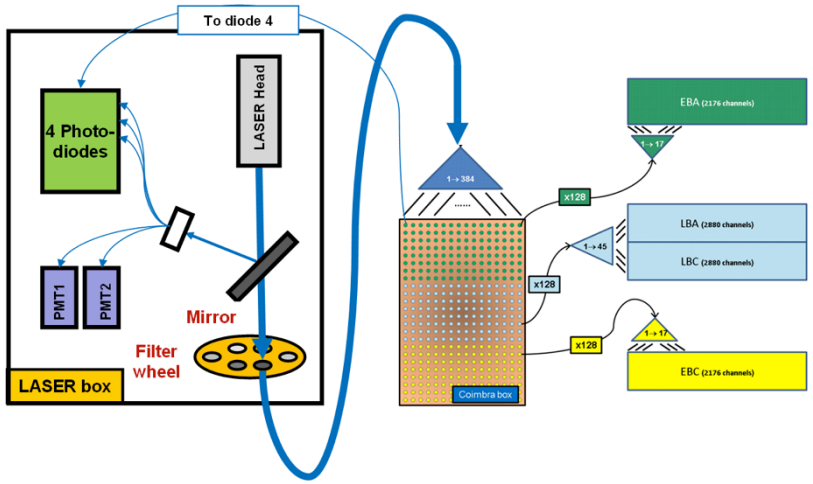
Calibration systems: CIS



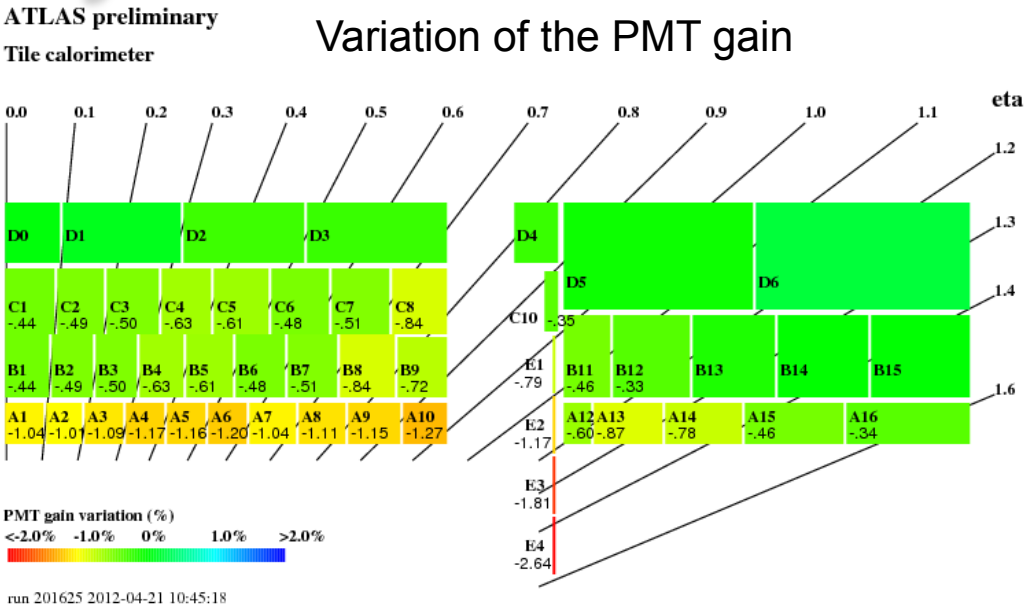


- Charge injection system (CIS) can inject a known charge into the shaper circuit. This pulse is then sampled by 40 MHz ADC like a physics signal
- Amplitude of the pulse is used to calibrate the conversion from ADC counts to pC
- The conversion factor is constant in time at the level of 0.02%
- Runs are taken twice per week for monitoring purposes
- Can be even used to simulate jets for L1 trigger

Calibration systems: Laser

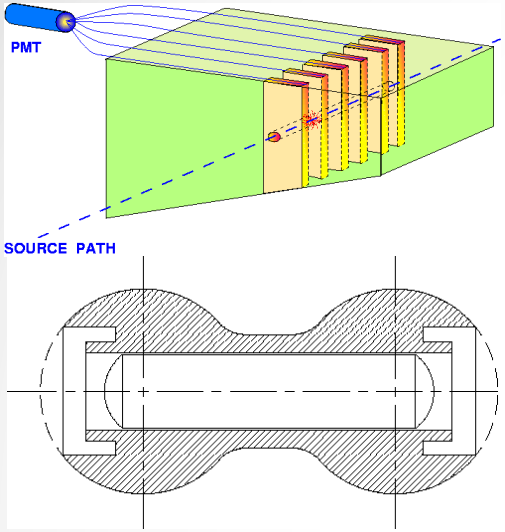


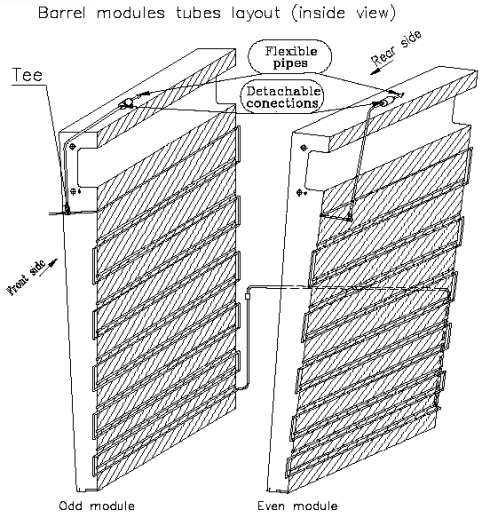
Laser calibration scheme

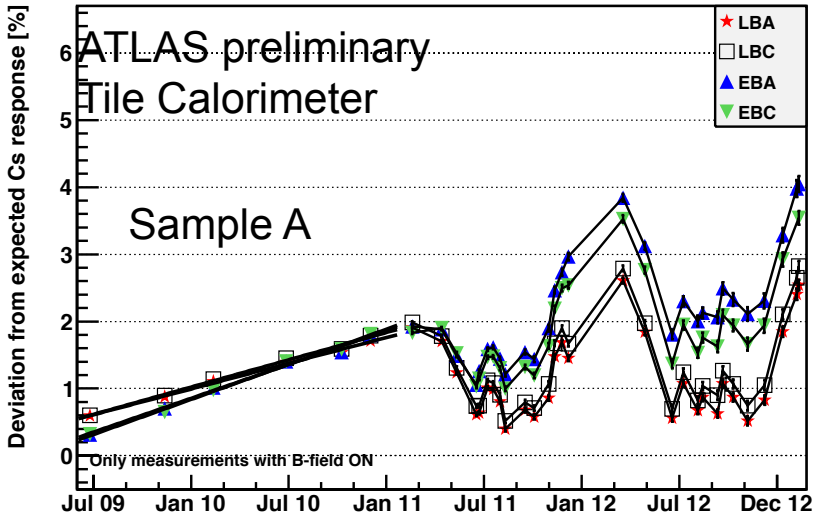


- Laser system monitors the stability and the evolution of the PMT gain by sending calibrated laser pulses (532 nm) to all PMTs simultaneously via clear fibres
- Follows the evolution of calorimeter response between Cs source scans, PMT gain drifts due with high current
- Precision better than 0.5% on the gain variation, in a time period of one month
- The largest drift is observed in A cells and gap/crack scintillators
- Also used to adjust and verify timing settings

Calibration systems: Cs

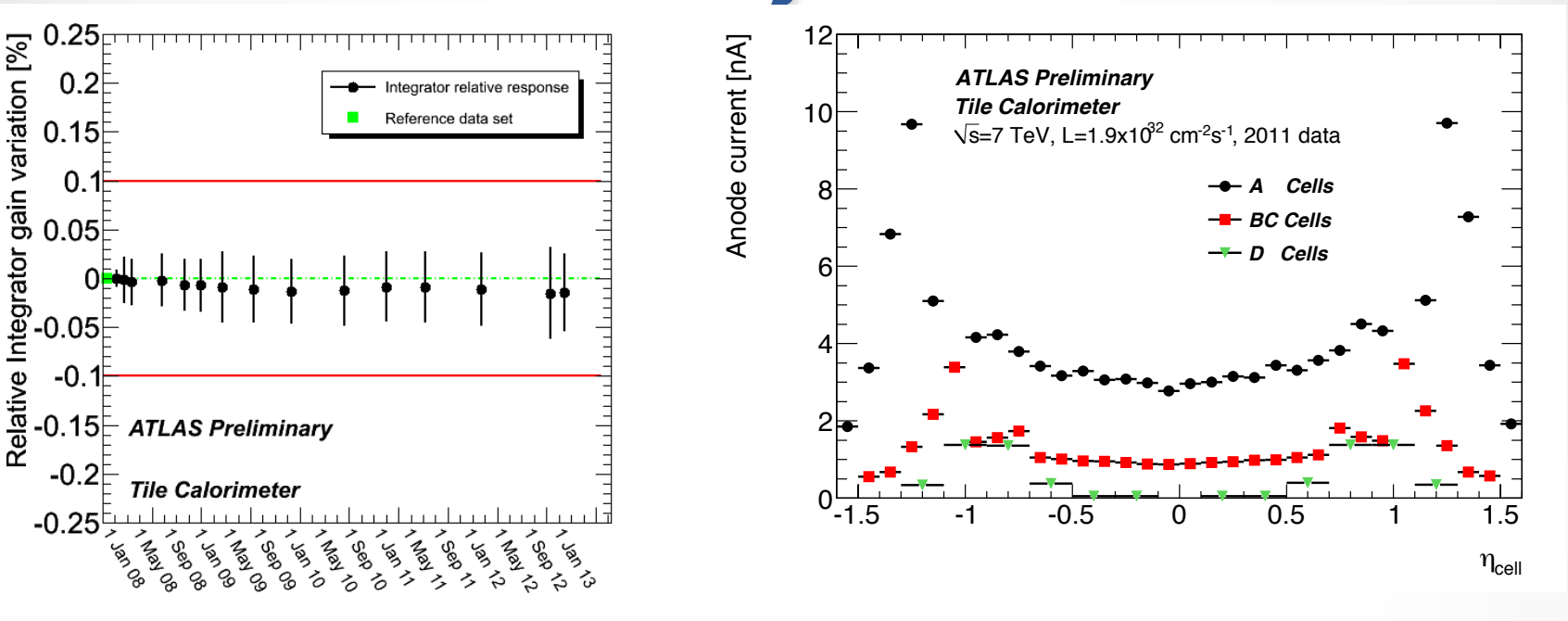






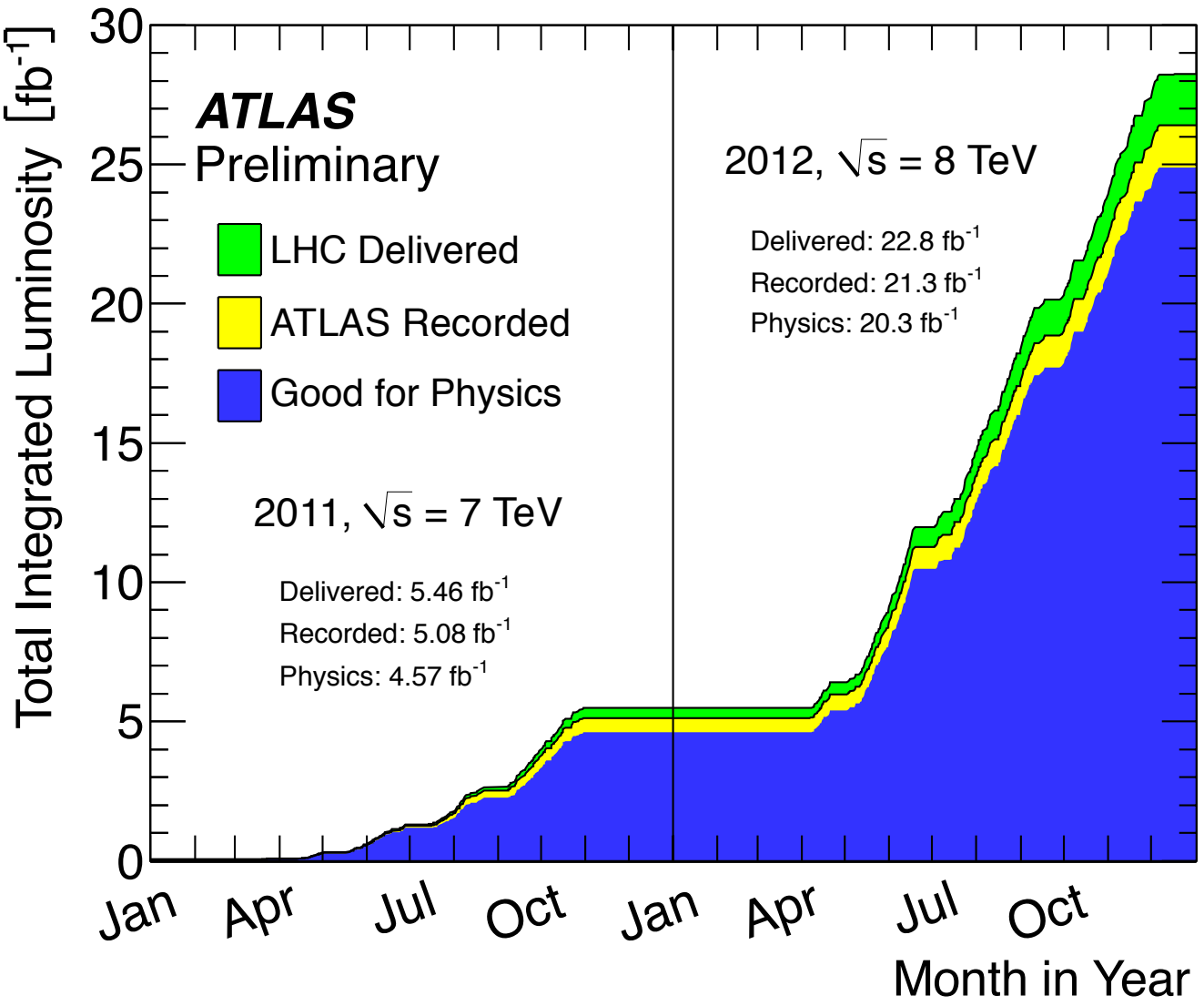
- Cs system scans all scintillating tiles with moving ^{137}Cs (662 keV) radioactive source, reading integrated currents from PMTs
- 1-2 scans per month during beam-off time
- Used to transport calibration scale from test beam measurements to running detector
- Cs scan results are used to calculate and adjust HV for PMTs to equalize cell's responses for better uniformity
- Cs scans follow the evolution of response of full optical chain from scintillating tiles to PMTs

Calibration systems: MBM

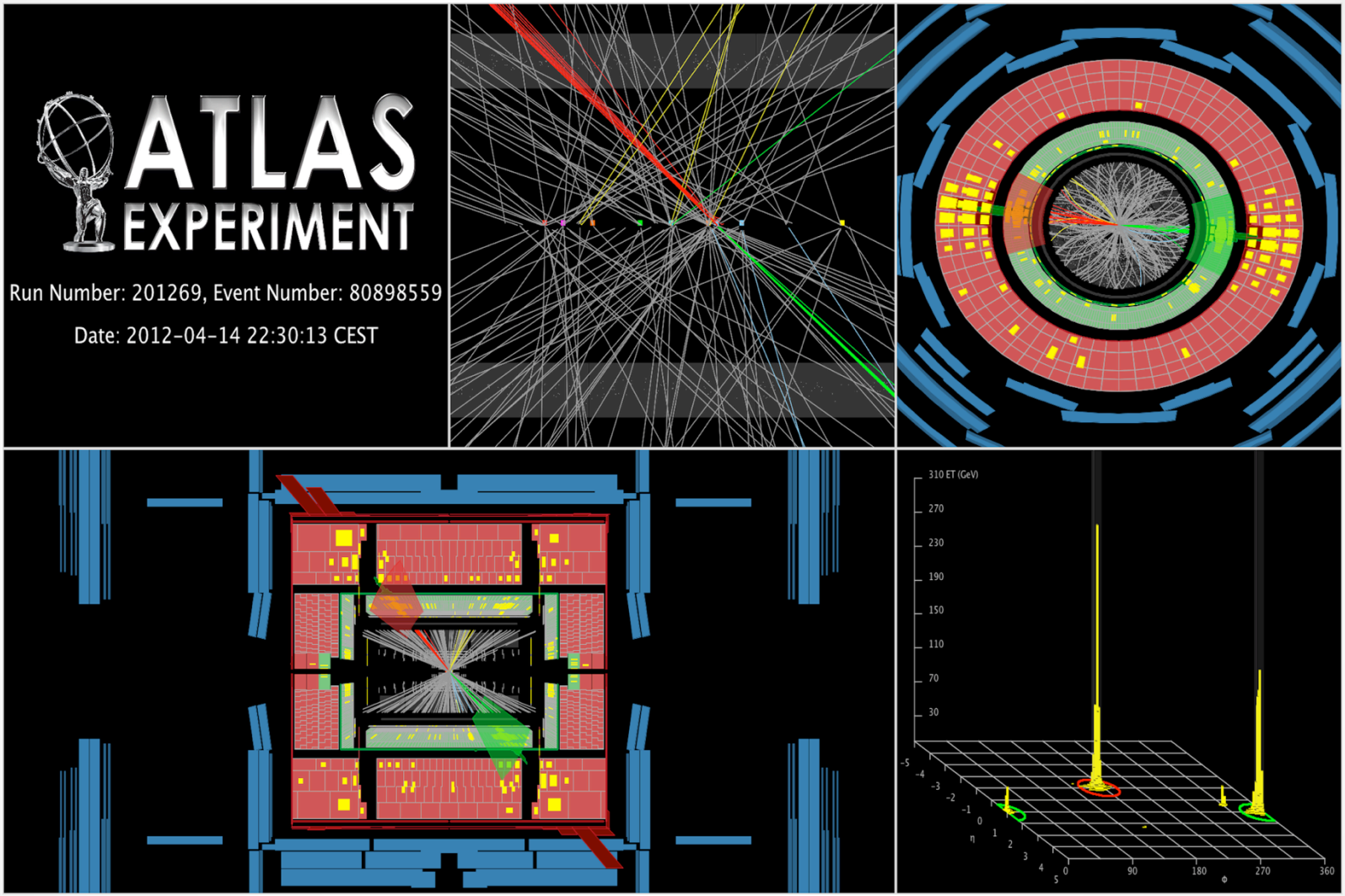


- Minimum bias monitoring system (MBM) reads integrated PMT currents of all PMTs during physics runs
- Measures luminosity and pile-up conditions
- Follows the response of the detector
- Confirms detector response variation
- Stability of each channel better than 0.05%, average stability is better than 0.01%

Run I performance

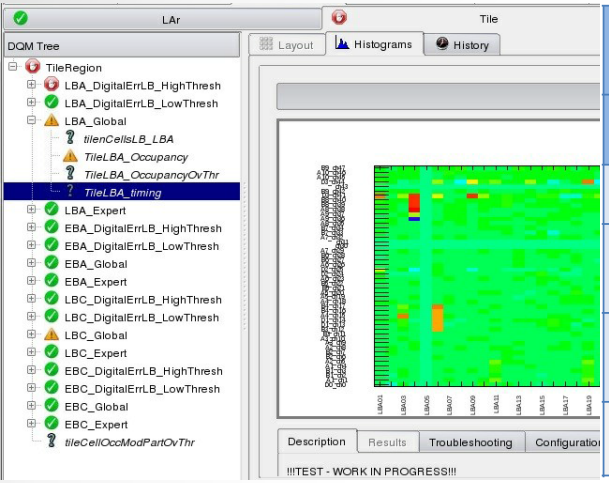


ATLAS event



Run-I event display with two central high-pT jets with an invariant mass of 4.23 TeV. The missing E_T in this event is 125 GeV

Data quality monitoring



ATLAS p-p run: April-December 2012

Inner Tracker			Calorimeters		Muon Spectrometer				Magnets	
Pixel	SCT	TRT	LAr	Tile	MDT	RPC	CSC	TGC	Solenoid	Toroid
99.9	99.1	99.8	99.1	99.6	99.6	99.8	100.	99.6	99.8	99.5

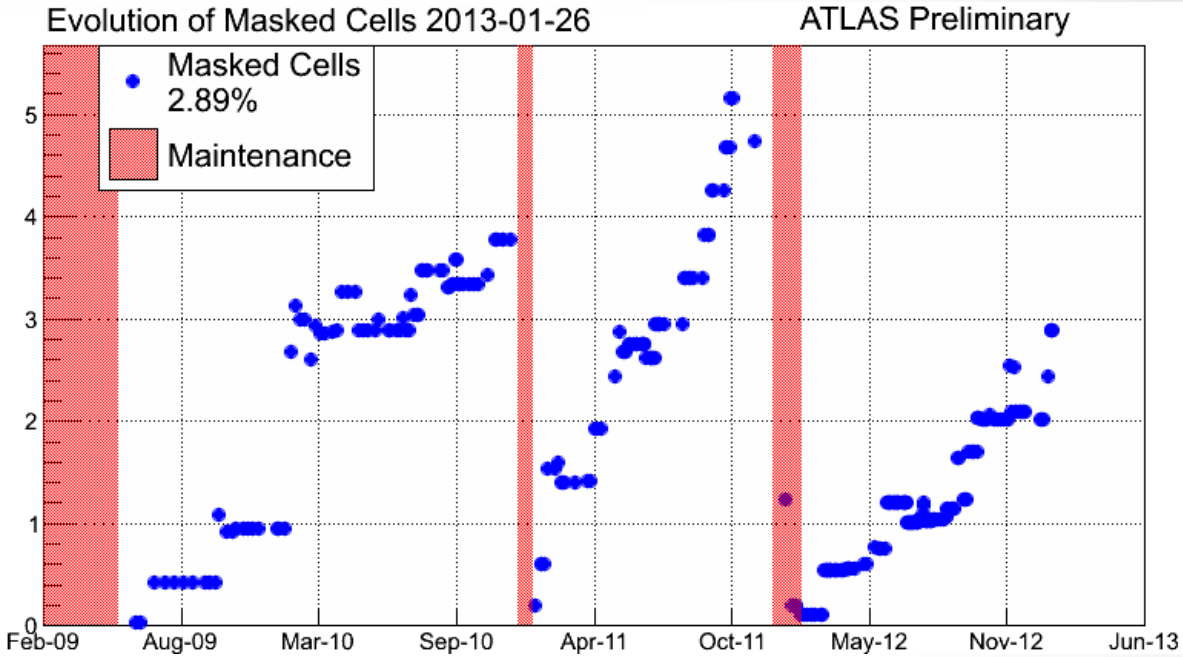
All good for physics: 95.5%

Luminosity weighted relative detector uptime and good quality data delivery during 2012 stable beams in pp collisions at $\sqrt{s}$=8 TeV between April 4th and December 6th (in %) – corresponding to 21.3 fb^{-1} of recorded data.

- Data quality monitoring framework (DQMF) monitors and collects the information of the quality of the data
- Automated quality check based on test criteria on performance histograms
- Visual control by shifters
- Thanks to all the efforts the resulting quality of the Tile Calorimeter data is 99.6%

Detector status evolution

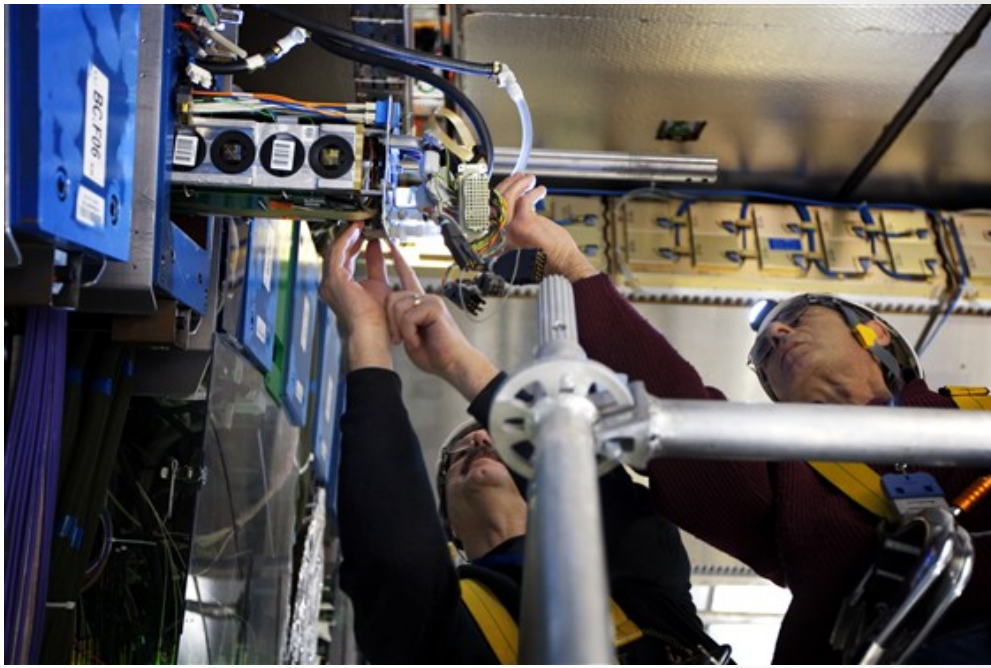
- 6 modules off (LVPS)
- 2.89% masked cells
- Masked cell energy is interpolated from the neighboring cells
- 4 modules with bad HV
- The bad HV cell's EM scale is restored with Cs and laser calibration

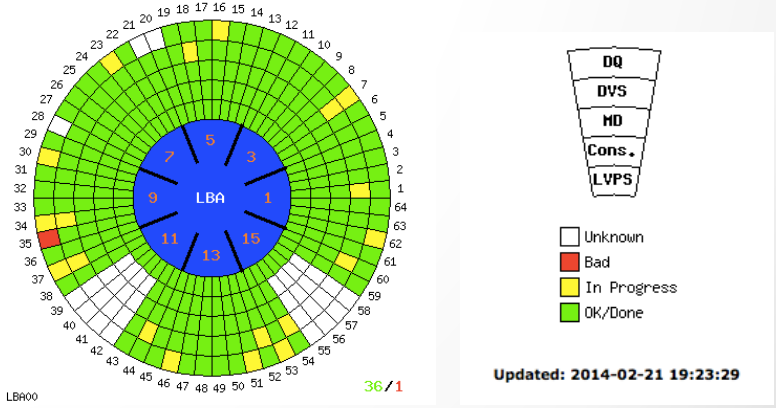


- The number of "bad" channels is increasing during data taking periods, mainly due to the failures of power supplies, taking the full module down
- Most of the broken channels are fixed during maintenance campaigns, thanks to the possibility to access front-end electronics during shutdown time
- Low voltage power supplies were replaced with upgraded ones that are more reliable and have lower noise

FE electronics maintenance

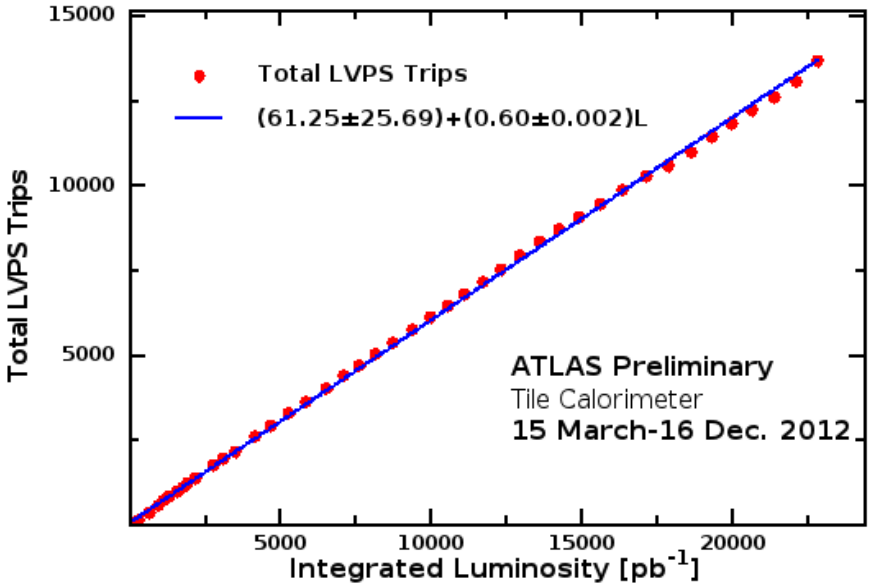
- During shutdown, when ATLAS detector is opened
- FE electronics "drawers" are extracted and bad components are replaced or fixed
- Allows to operate with minimum number of bad channels to maximize the quality of the data
- Data quality from consolidates modules is checked and the progress is tracked with web tools





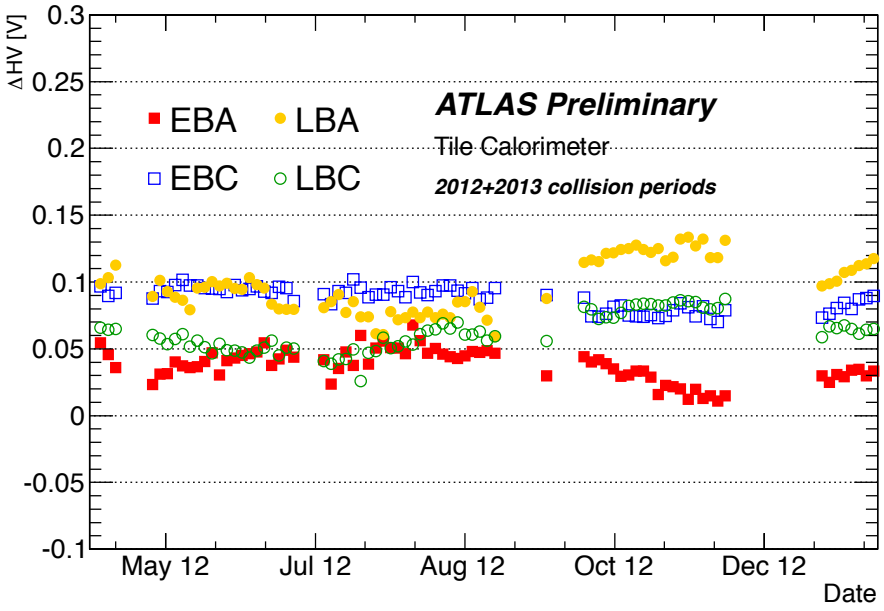
Low voltage power supplies

Finger LVPS box assembly

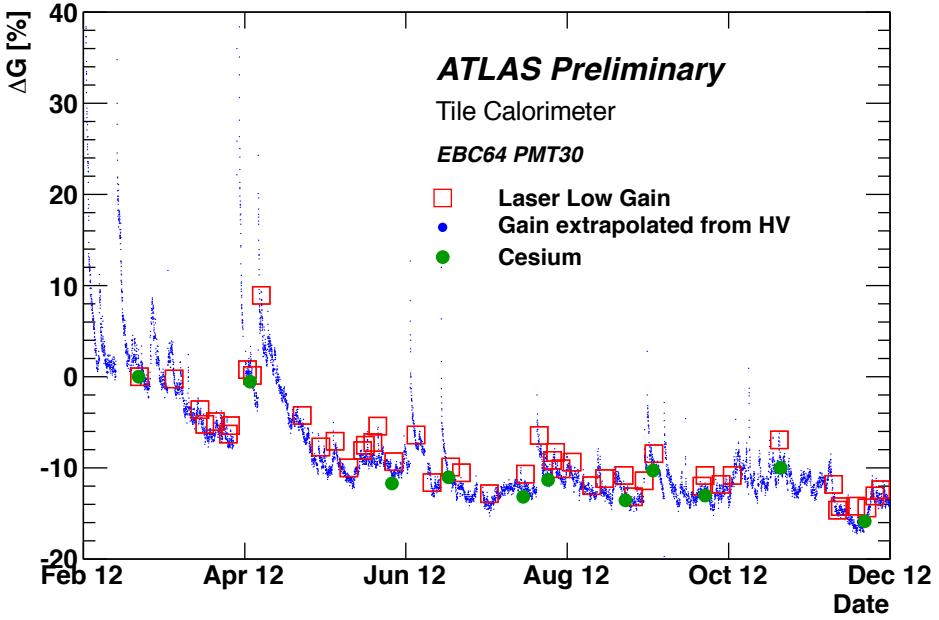


- The on-detector FE electronics power-supplies were quite sensitive and exhibit numerous trips, proportional to the integrated luminosity
- Automatic procedures to recover the tripped module were implemented in DCS and DAQ
- The power supply design was modified and proved to be more reliable and have lower noise
  - Just one trip from the sample of 40 new power supplies
  - All power supplies were replaced with the new design before Run-II

PMT gain monitoring



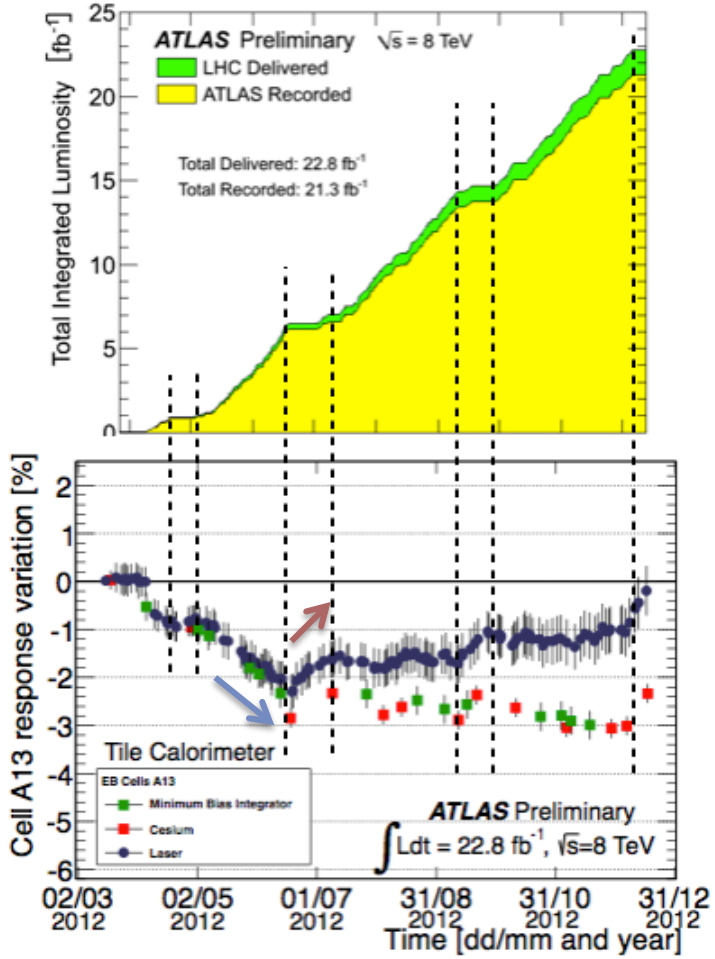
HV stability over time



Unstable channel monitoring

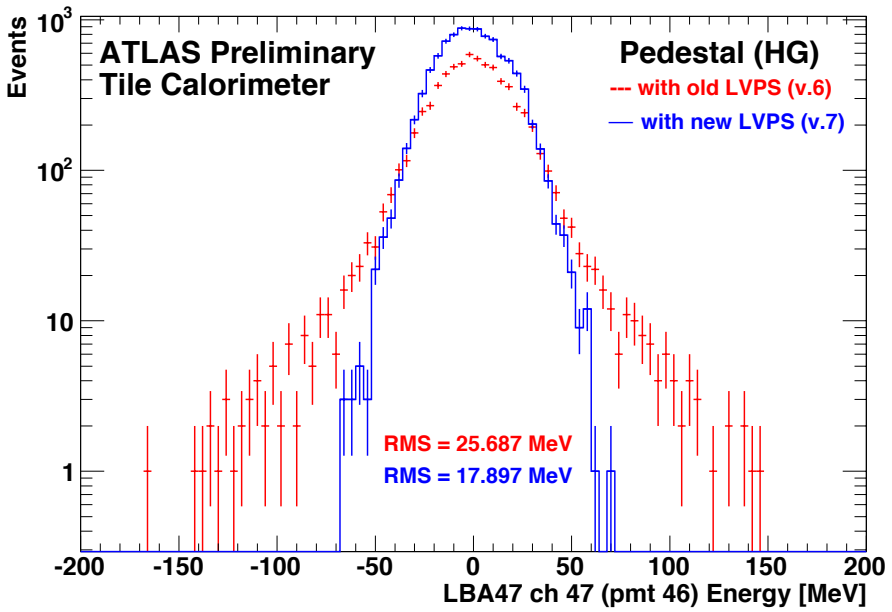
- With the gain proportional to HV (1V~1%), the stability of the HV system is crucial
- Each channel's HV is monitored
- Unstable channels are monitored and corrected with laser calibration system

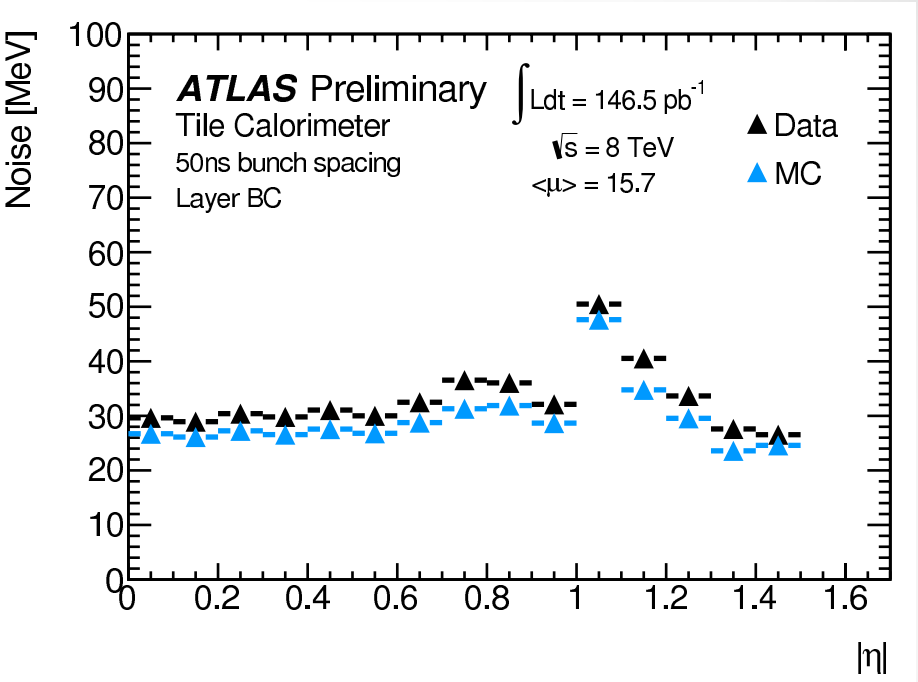
Calibration systems: combined performance



- Full set of calibration systems allows reliable and accurate calibration of the calorimeter
- Detector response drifts down with integrated luminosity and recovers back during accelerator technical stops
- Calibration systems agree with each other and follow the calorimeter response behaviour

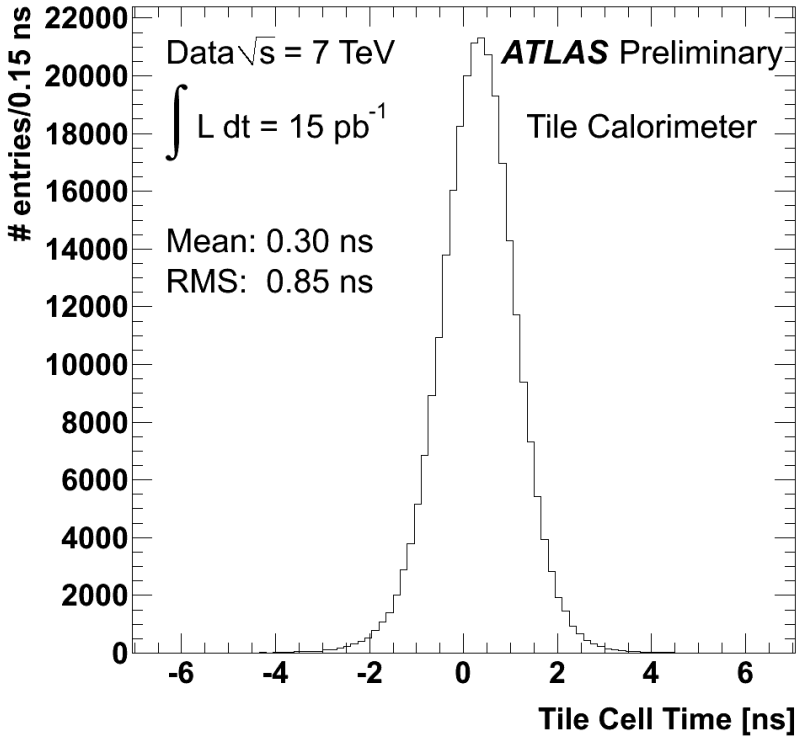
Noise

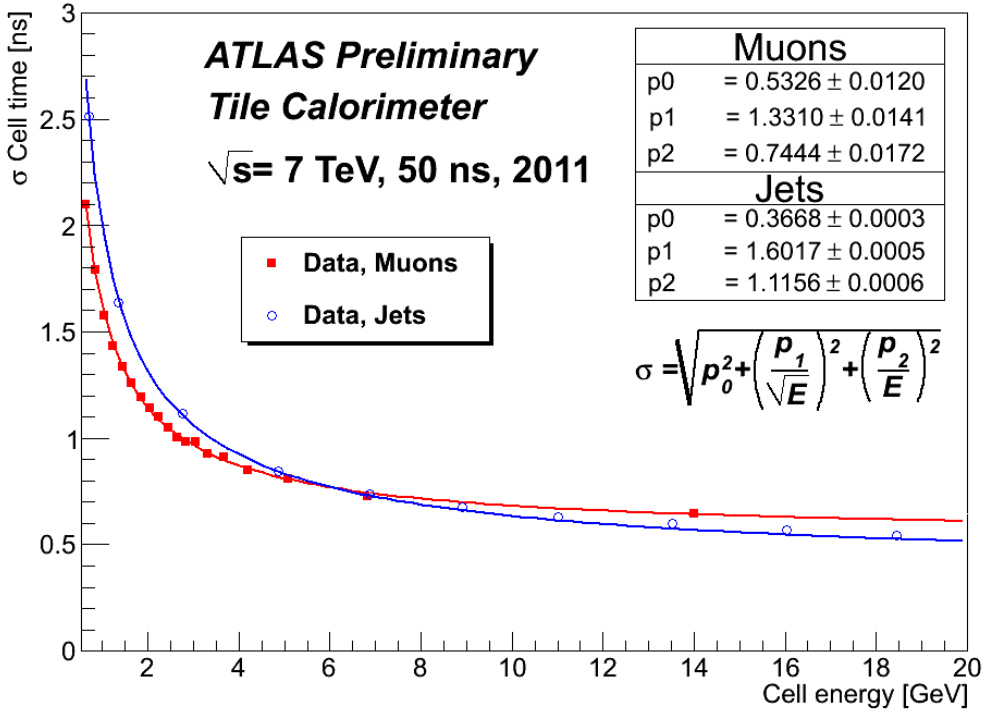




- Cell noise width was affected by old power supplies and had to be modeled with two Gaussians
- New, improved power supplies have lower noise and single-Gaussian shape
- Pile-up noise simulation is in good agreement with data

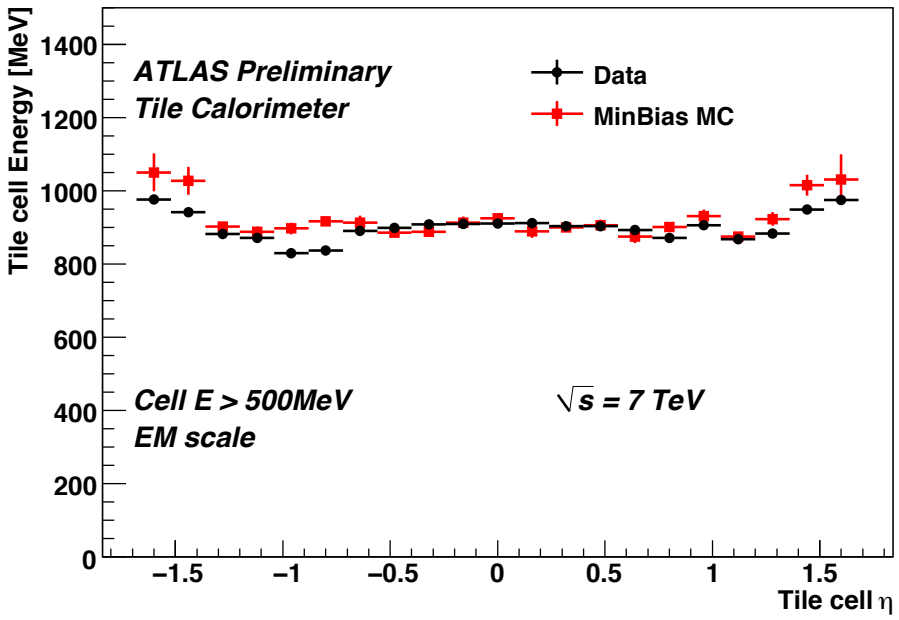
Timing

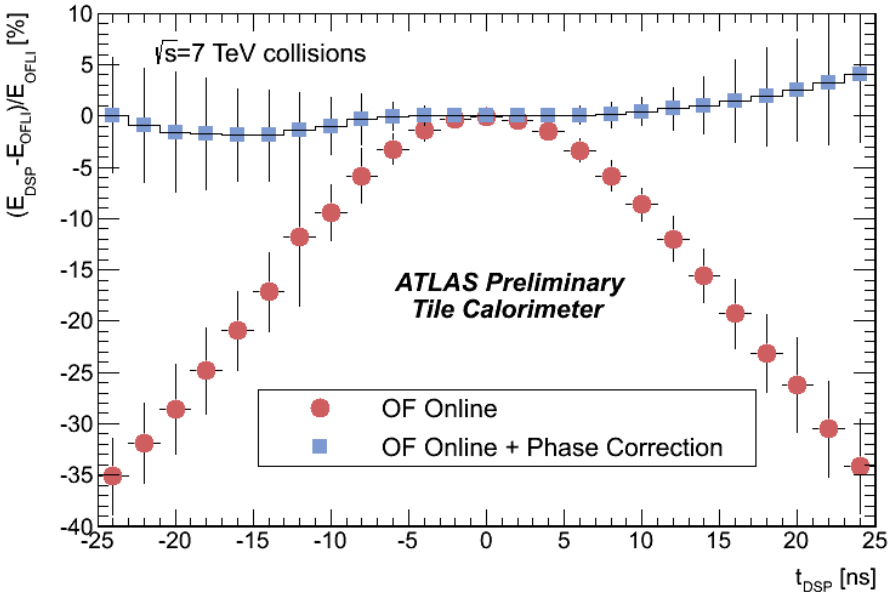




- Initial time calibration done with laser, beam splashes and scraping beam
- Good cell time performance and resolution

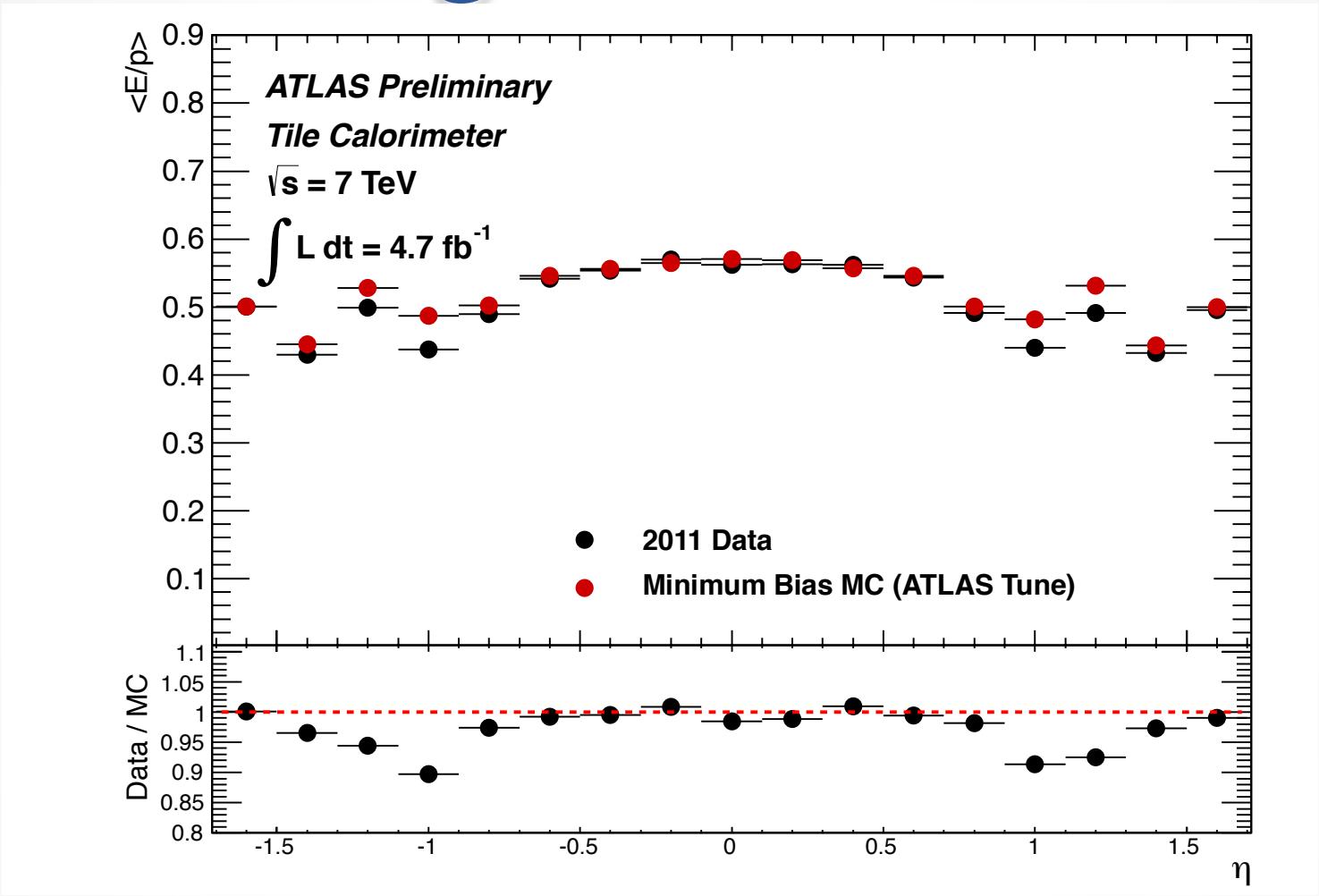
Energy reconstruction





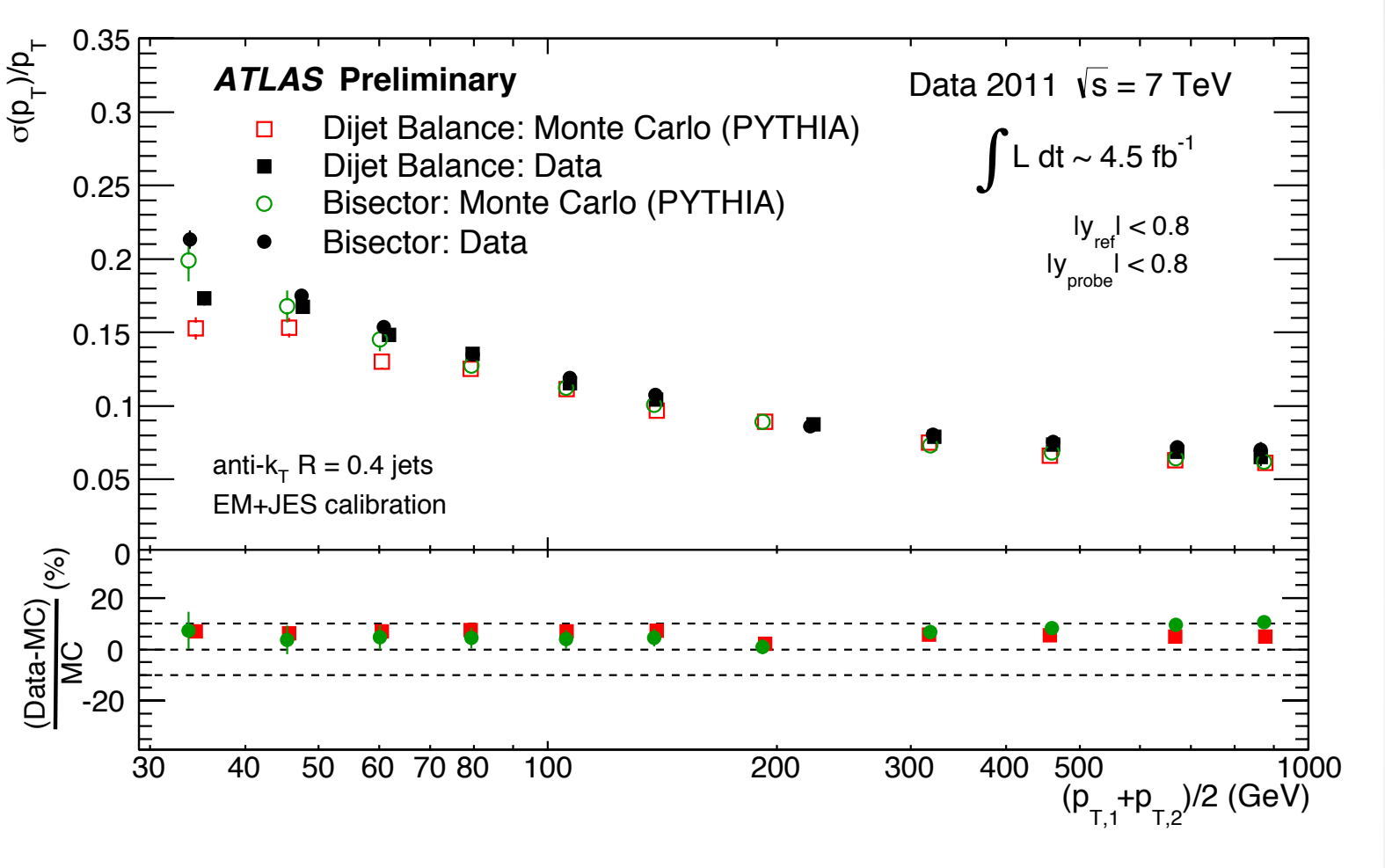
- Good agreement between data and simulation
- Energy is calculated online for high level trigger
- Good agreement between online and offline
- Energy calculation depends on the phase of the signal, can be corrected online

Single hadrons



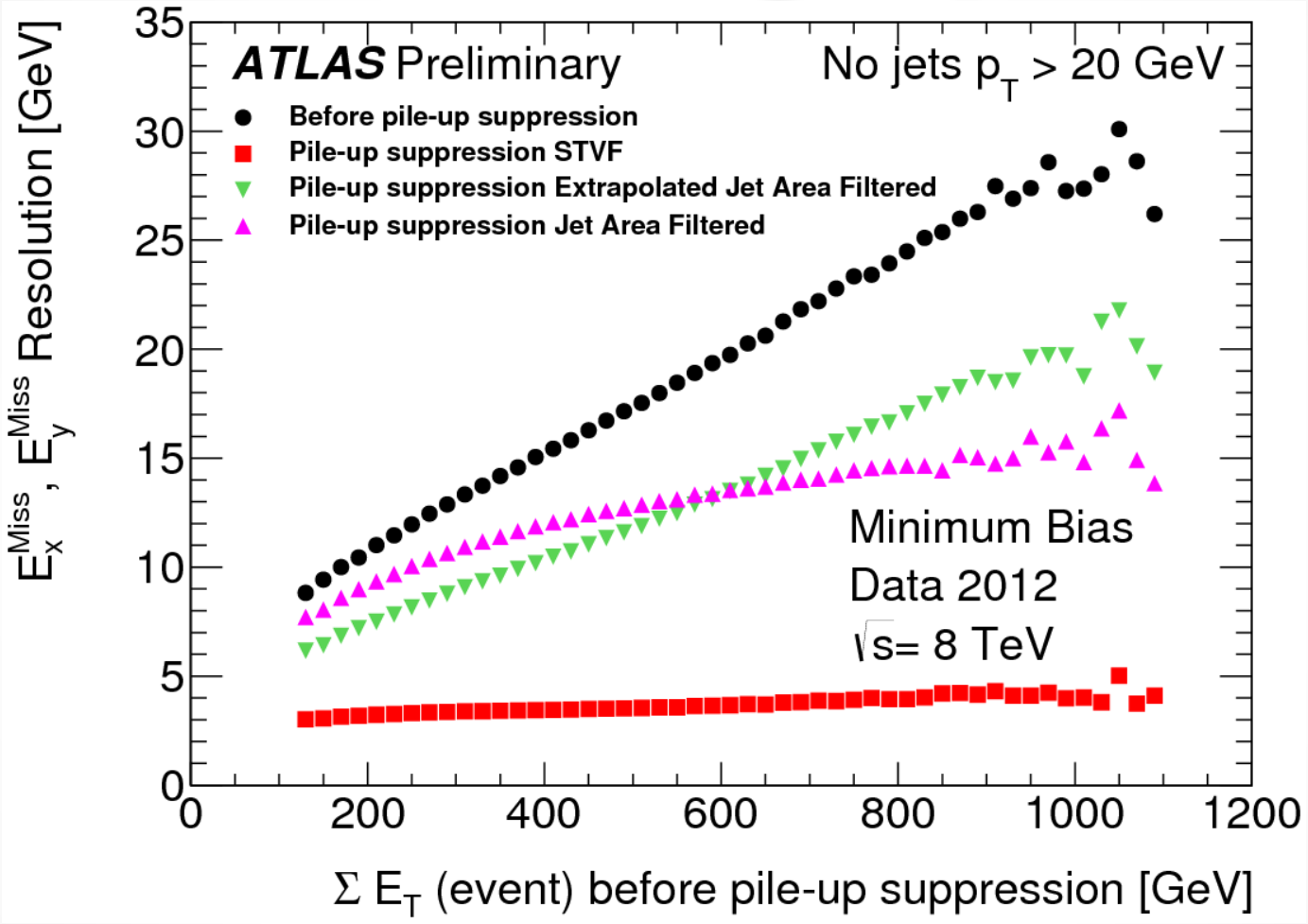
- Correct description of E/p ratio for isolated hadrons

Jets



- Jet transverse momentum resolution is under 20%

Missing E_T

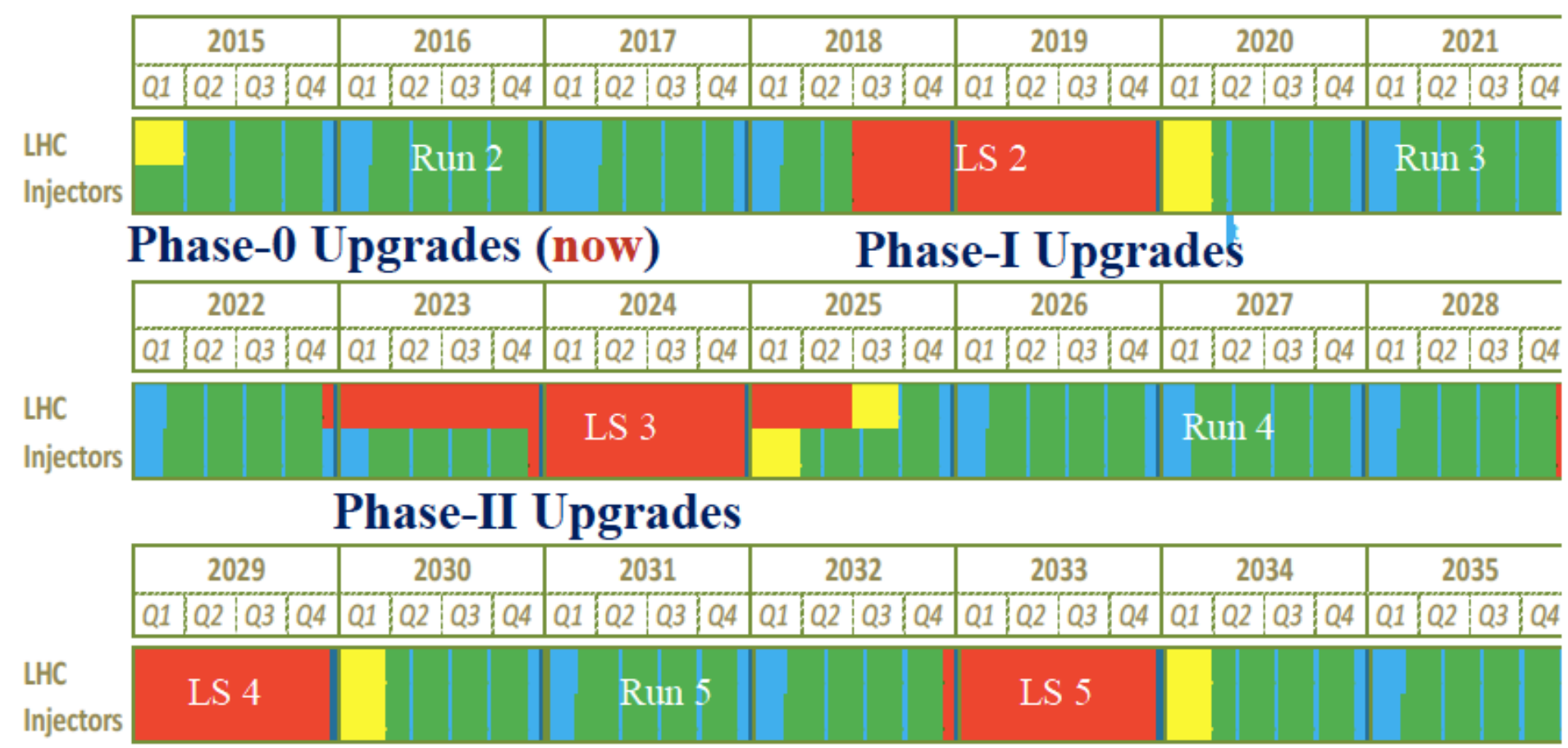


- Good resolution of missing E_T measurements
- Robust pile-up suppression algorithms

Upgrade program

- Advanced physics goals and LHC upgrade plans create new challenges for detectors
  - LHC upgrade program aims at 5-10 fold luminosity increase → more radiation → better radiation tolerance required
  - Ageing electronics → originally planned for 10 years of operation
  - Higher event rates require more efficient trigger algorithms
- A multi-phase upgrade program has been conceived: Phase-0, Phase-I and Phase-II
- The major Tile Calorimeter mechanics and optics will stay, together with associated PMTs
- Front-end and back-end electronics, calibration systems, will undergo major upgrades
  - Complete redesign for font-end and back-end electronics
  - New electronics drawer mechanics
  - Fully digital trigger with higher selectivity and finer granularity
  - Demonstrator project to discover and solve issues as early as possible

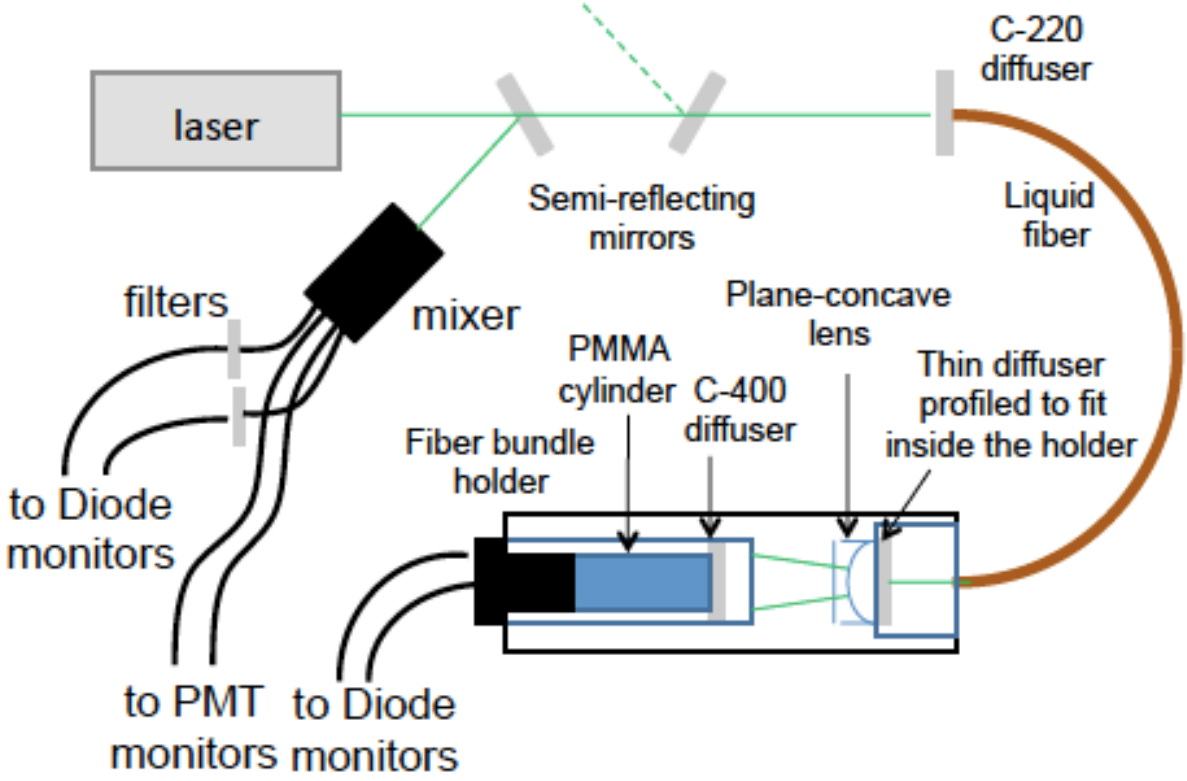
LHC and upgrade schedule

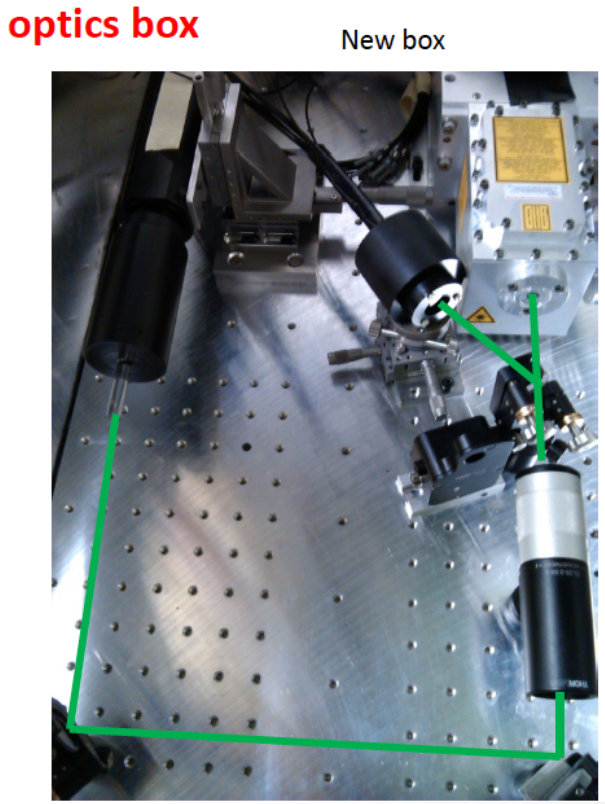


Ph0: Run-II improvements

- Before Run-II all Tile Calorimeter front end electronics drawers were extracted to fix problematic channels
- New, stable, low-noise power supplies were installed
- Upgraded laser calibration system (Laser-II) is being constructed and will be installed
- Cesium calibration system will be improved
- The outer (D) layer muon trigger will be installed to reduce fake muon rate in a specific region

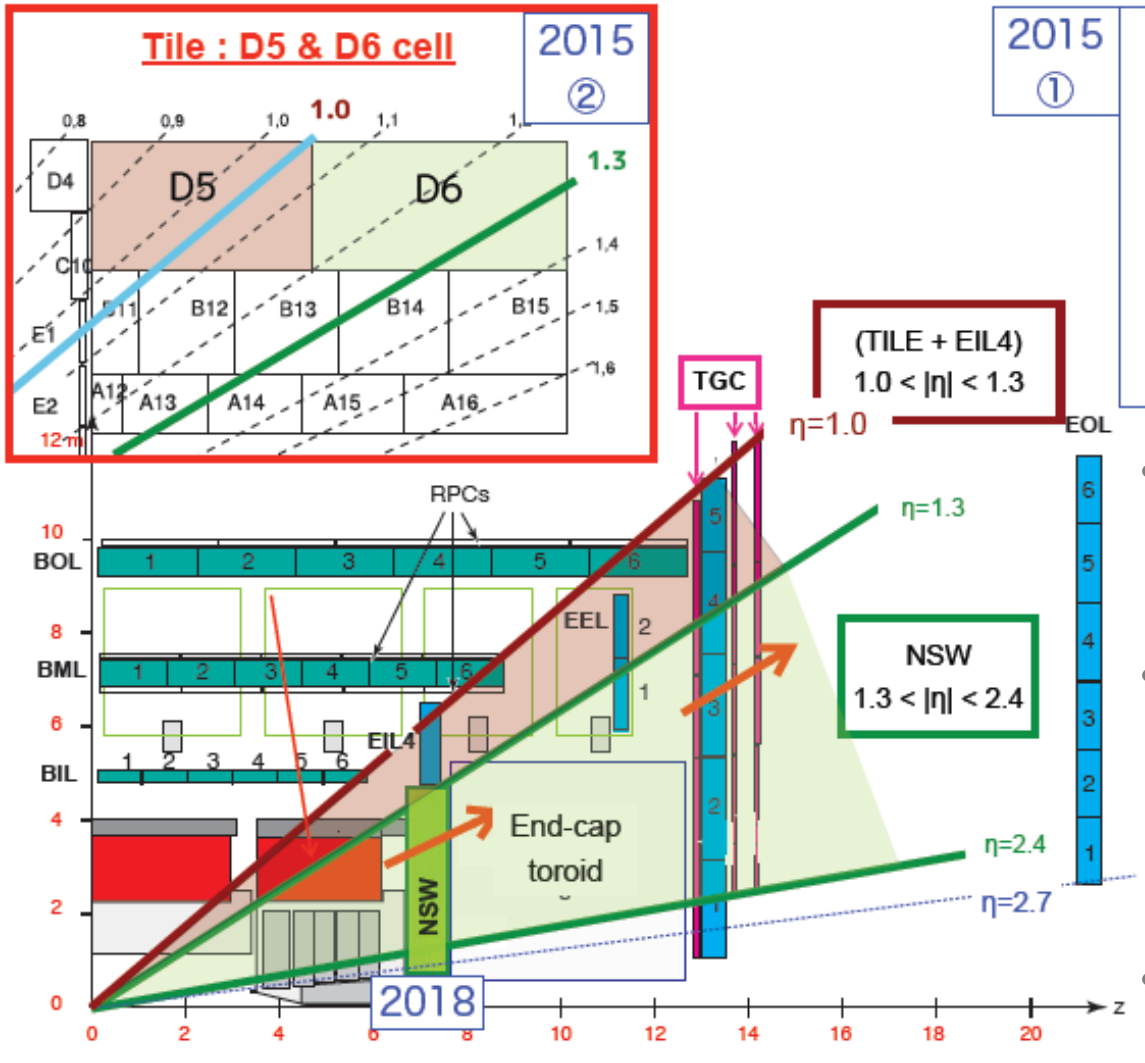
Ph0: Laser II

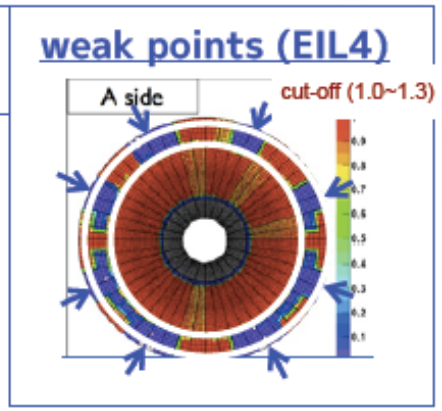




- New laser system with improved stability and precision is required to follow the evolution of the PMT response during high luminosity running
- Laser-II calibration system with new optics and electronics is being tested. Will be installed and ready for Run-II

Ph1: D-layer muon trigger



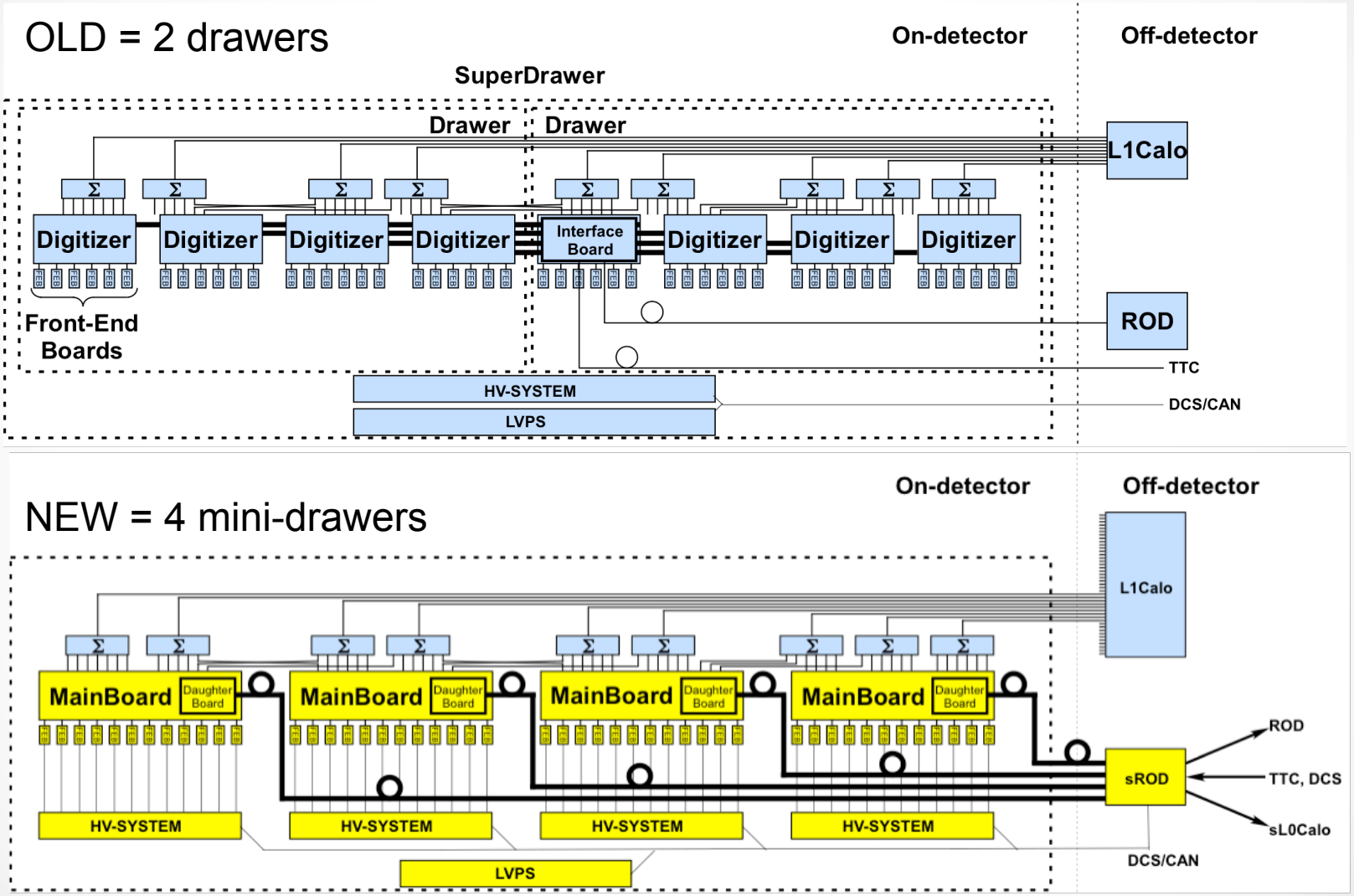


- L1 μ trigger in the End-cap region is polluted due to slow charged particles (protons)
- Region 1.0<| η |<1.3 can be cleaned up by taking coincidence with end-cap TGC muon chambers and Tile cells D5 and D6
- Tile muon trigger board (TMDB) is being developed for Run-II

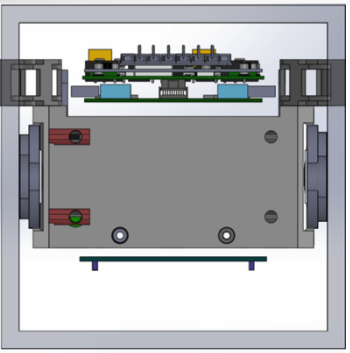
Ph2: FE electronics upgrade

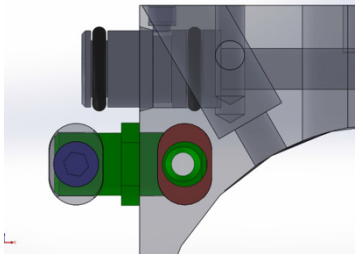
- The HL-LHC upgrade will require more performance from detector electronics
- The Tile Calorimeter will digitize shaped PMT signals and ship all samples off the detector for fast signal processing and digital triggering
- Good opportunity to explore new technologies, including high-performance FPGAs, fibre optics, improve reliability
- A demonstrator project will allow to test new ideas and technologies already in Run-II and demonstrate the feasibility of new design

FEE architecture changes



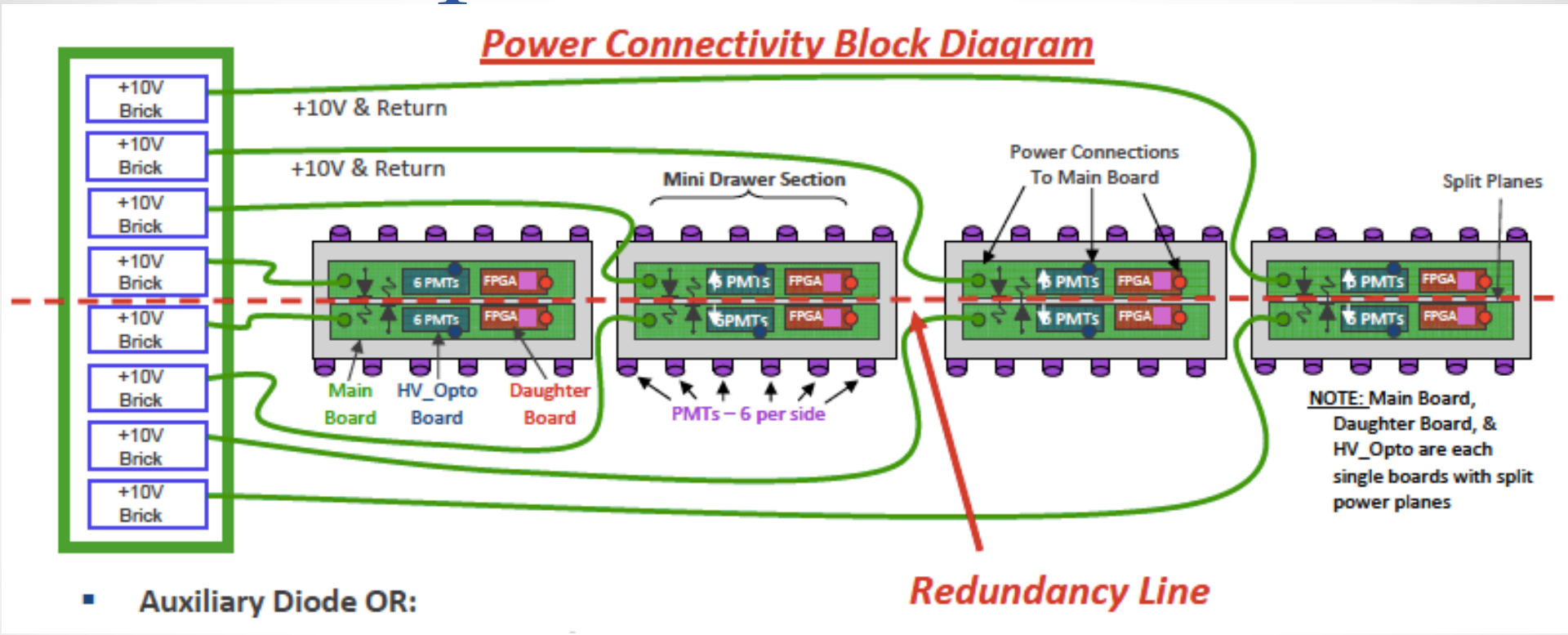
FEE new drawer mechanics





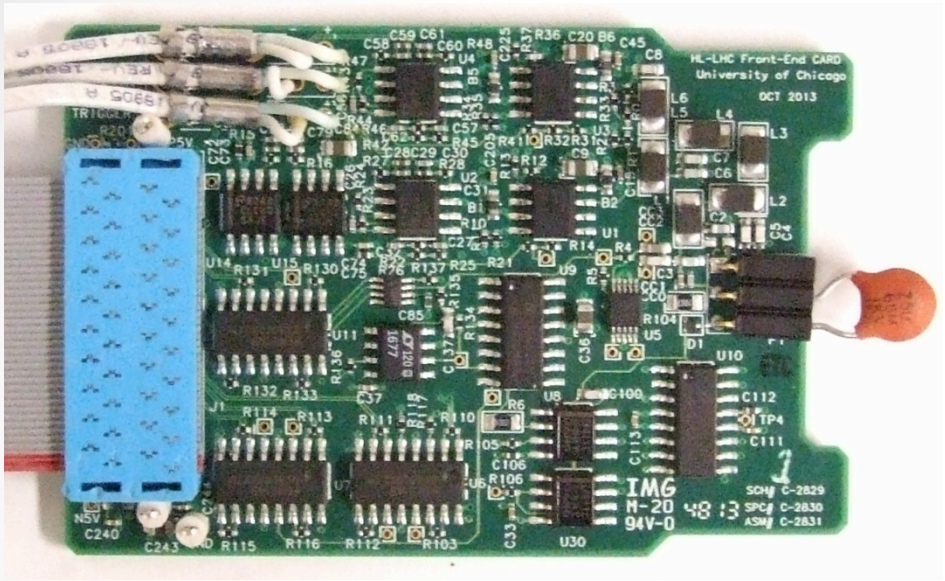
- To improve the operation, maintainability and handling a new mini-drawer design was made to replace the old super-drawer one
- New rigid inter-drawer connections and internal cooling
- New internal flexible cable trays

New power distribution



- To improve the reliability and redundancy, the electronics in the new design are made as independent as possible to reduce the number of single point failures
- Possibility to use dual power supply for redundancy

FEE upgrade options

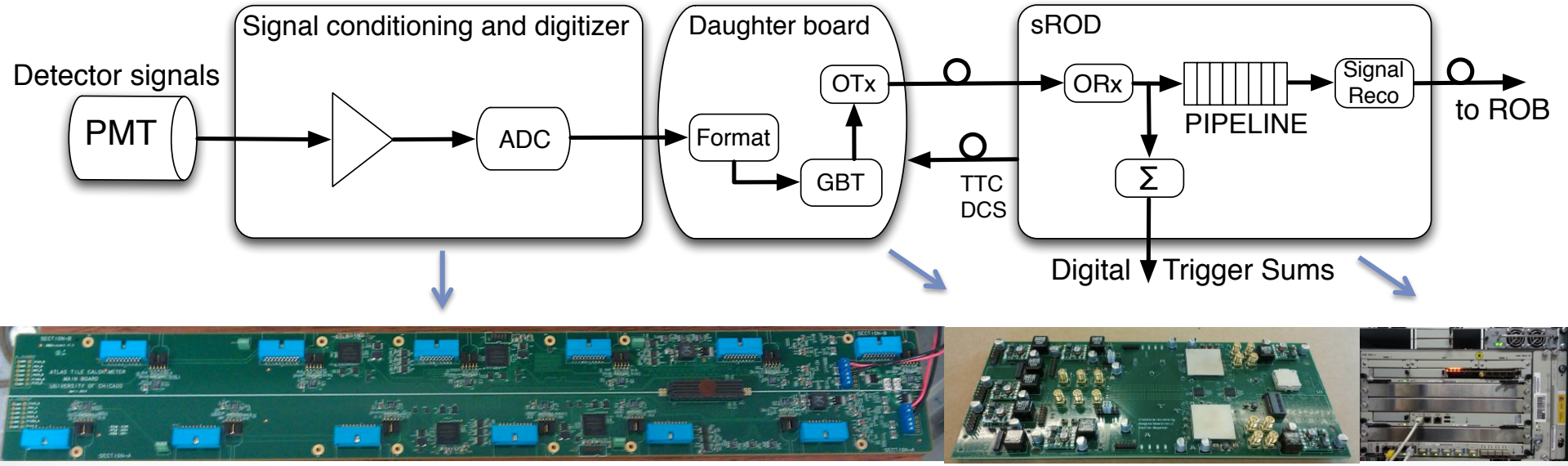


3in1 front-end board

HV distribution prototype

- Several design options are being followed for key components, up to three different technologies
  - Example: front-end card – 3in1 or ASIC or QIE
  - Example: HV system – on-detector/off-detector distribution
- The best option will be chosen based on performance results from test beams and dedicated tests

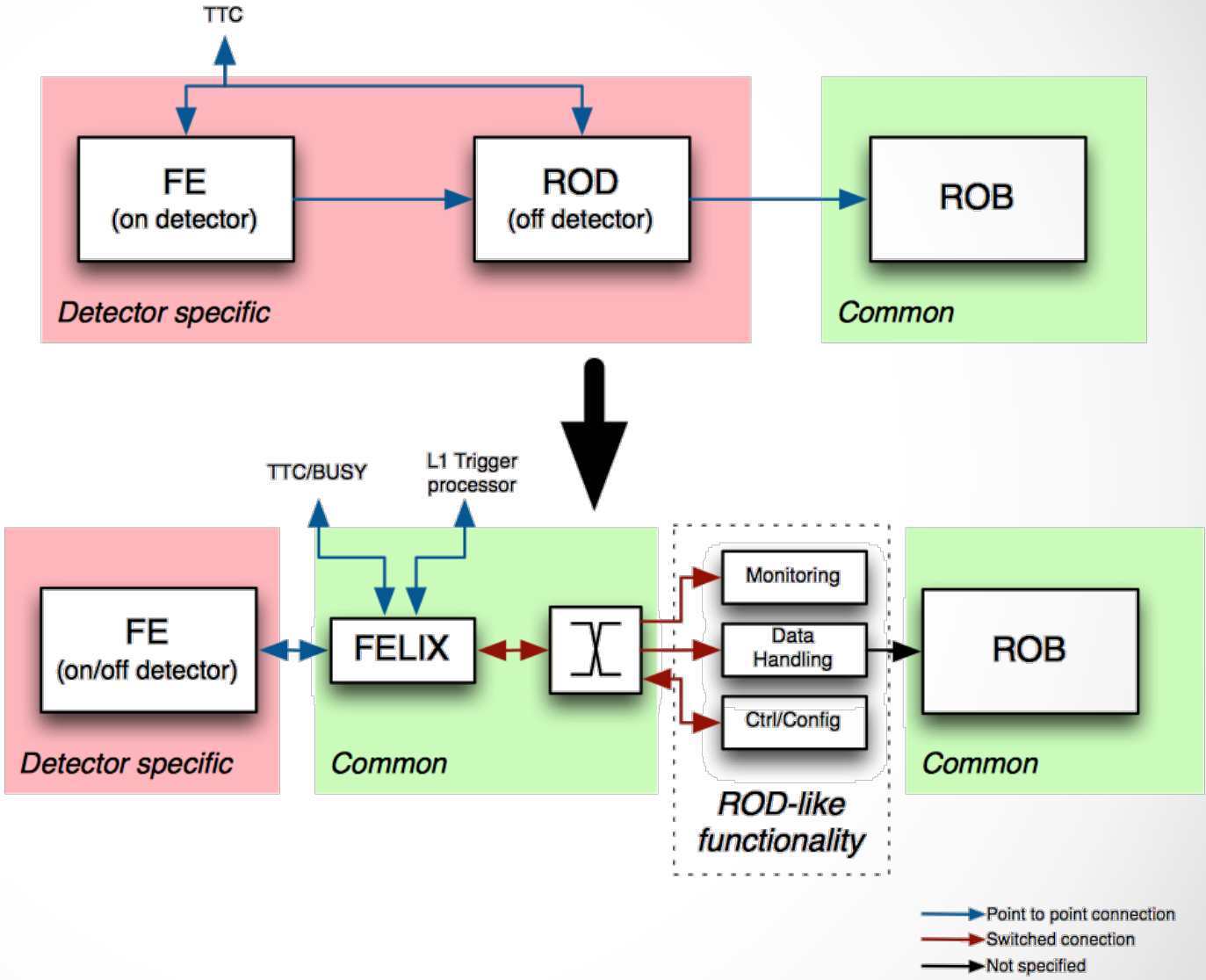
New readout electronics



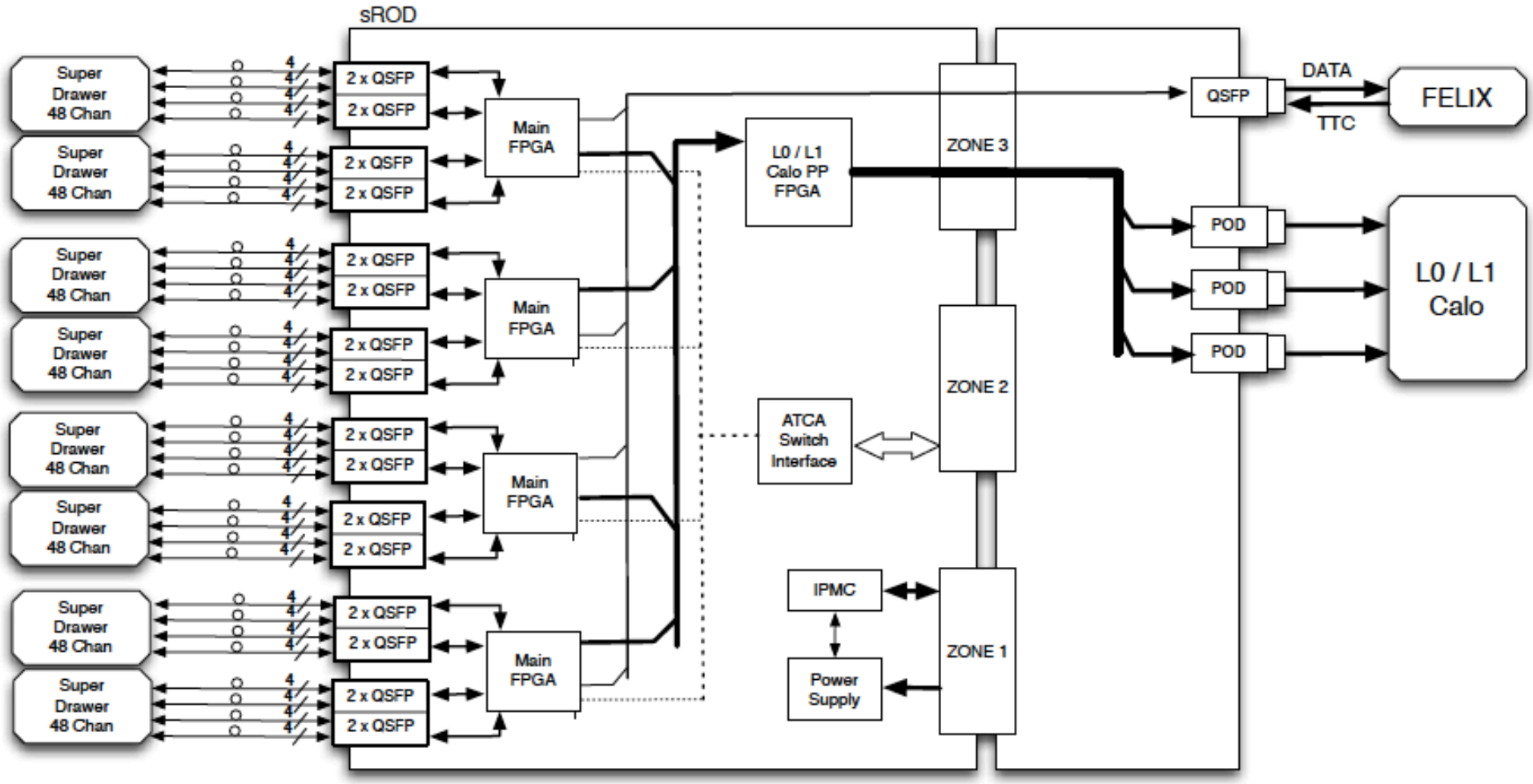
- The digitised samples will be sent outside the detector at full 40 MHz sampling speed
- The digital trigger and data buffering will happen in the back-end electronics

Proposed readout scheme

- To reduce detector specific parts use COTS switching networks
- Less P2P connections
- DCS and monitoring information routed directly to information consumers



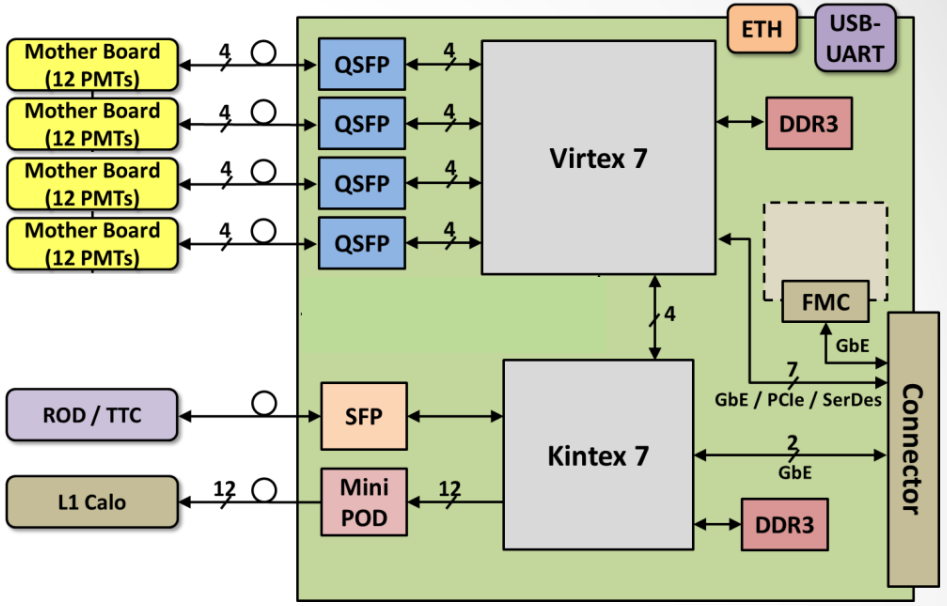
New BE electronics



- ATCA Super-ROD (sROD) board
- Processes data from 8 modules

Demonstrator

Demonstrator drawer insertion tests



sROD demonstrator board design

- In order to test and qualify new designs a "demonstrator" electronics drawer will be installed in the detector before Run-II
- To be compatible with the previous design the demonstrator will provide analogue trigger and standard data stream
- Board prototypes are being tested to be ready for insertion before the detector closure in August-2014
- Expert integration weeks proved to be essential for the project

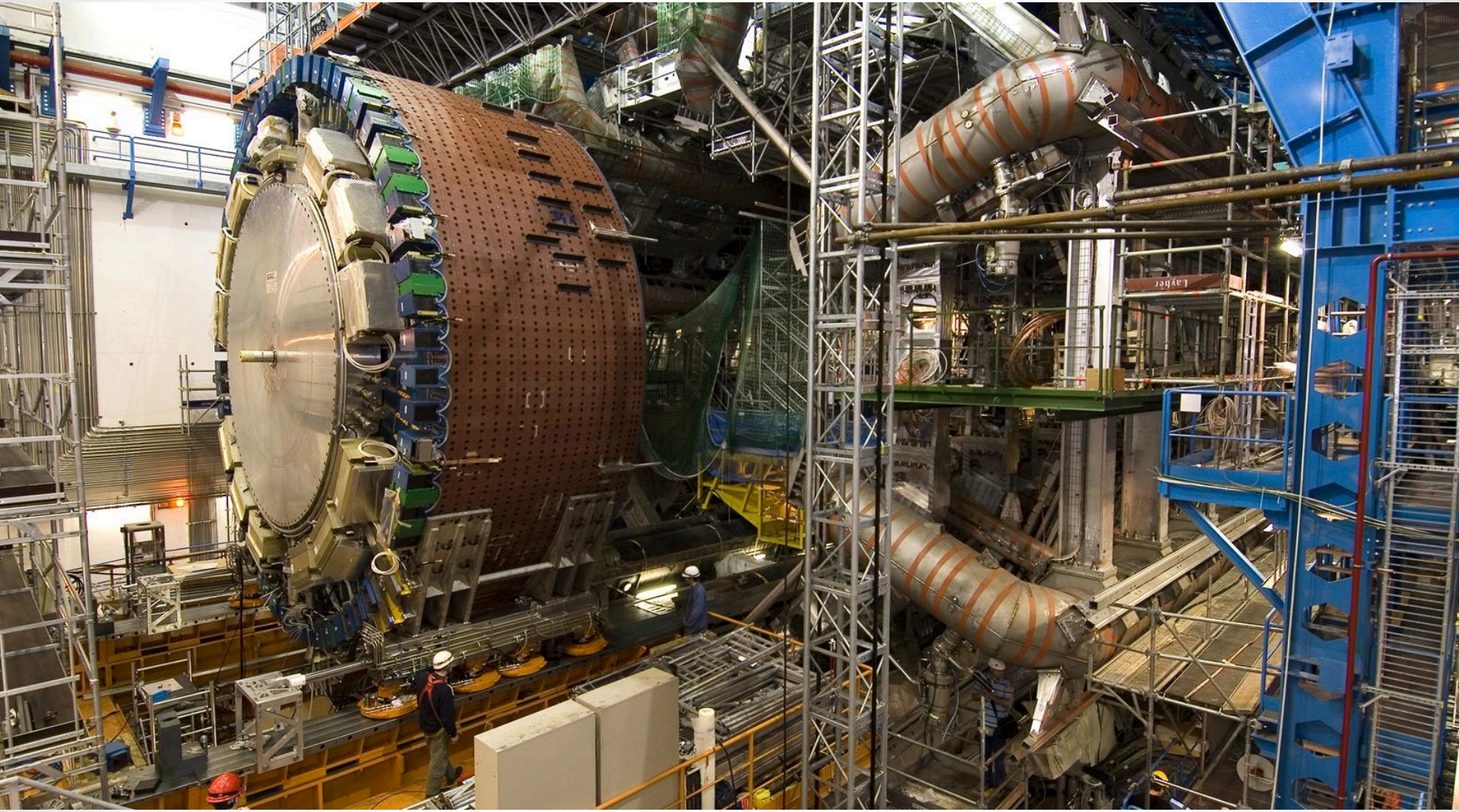
Summary

- Tile hadron calorimeter is a key detector in measuring jet energy and missing E_T energy in ATLAS experiment
- A full set of calibration systems ensures correct energy reconstruction in changing conditions
- PMT gain down-drift is well monitored, calibration systems follow the calorimeter response behavior
- Great Run-I performance with minimal data losses and high data quality
- Detector maintenance and Run-II improvements are underway
- Upgrade R&D projects for electronics replacement for HL-LHC programs are progressing, a demonstrator electronics drawer to be installed before Run-II

Thank you for your attention!

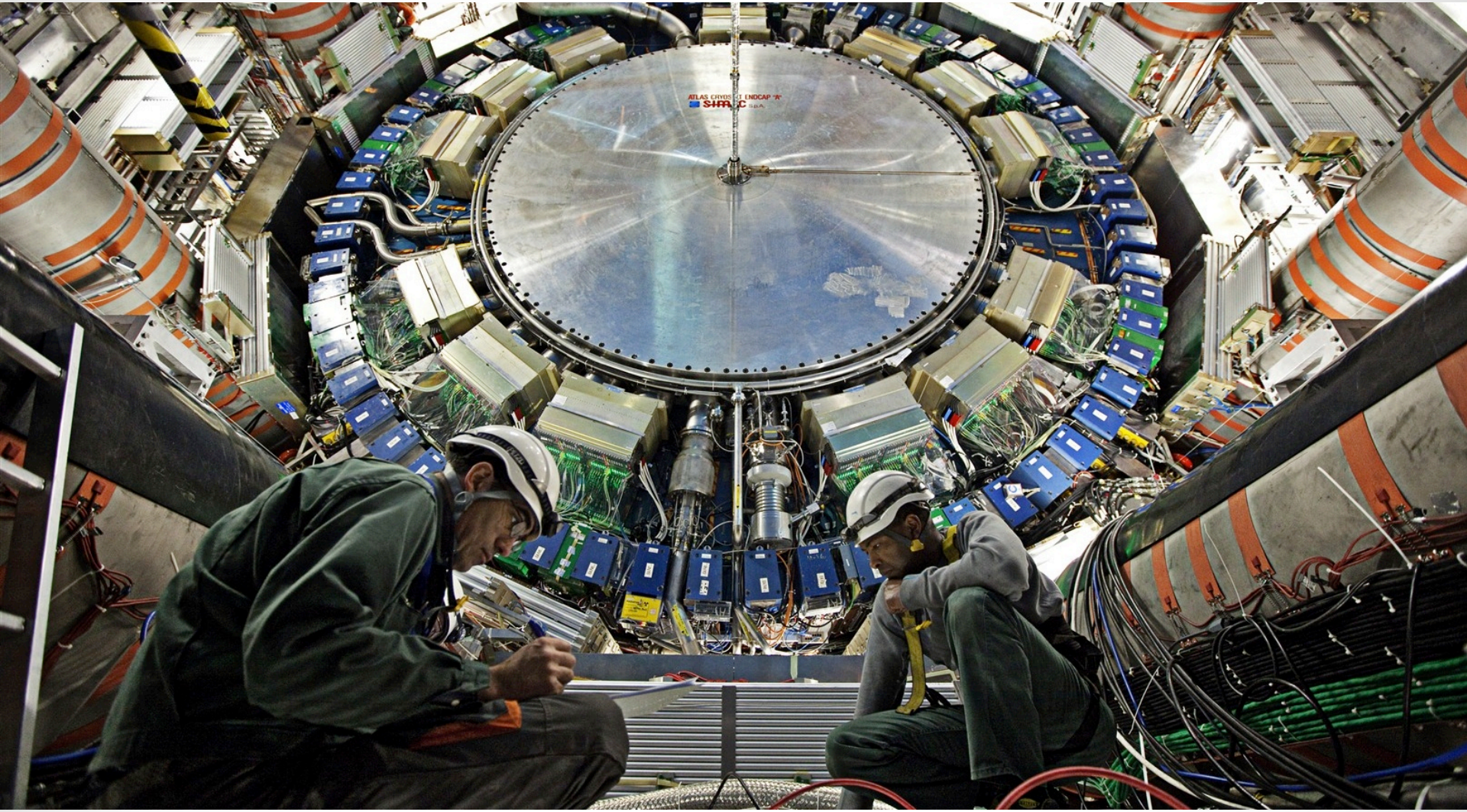
Backup slides

Calorimeter in the cavern



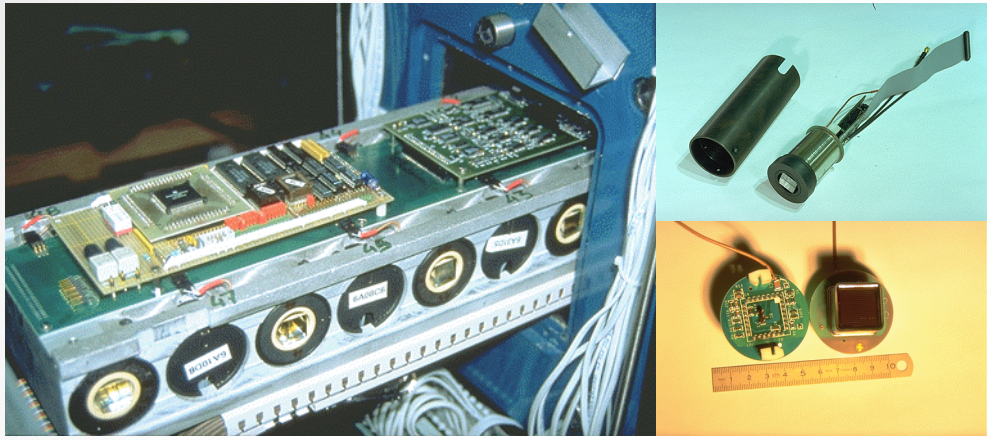
Extended Barrel calorimeters being moved to final position

Calorimeter in the cavern

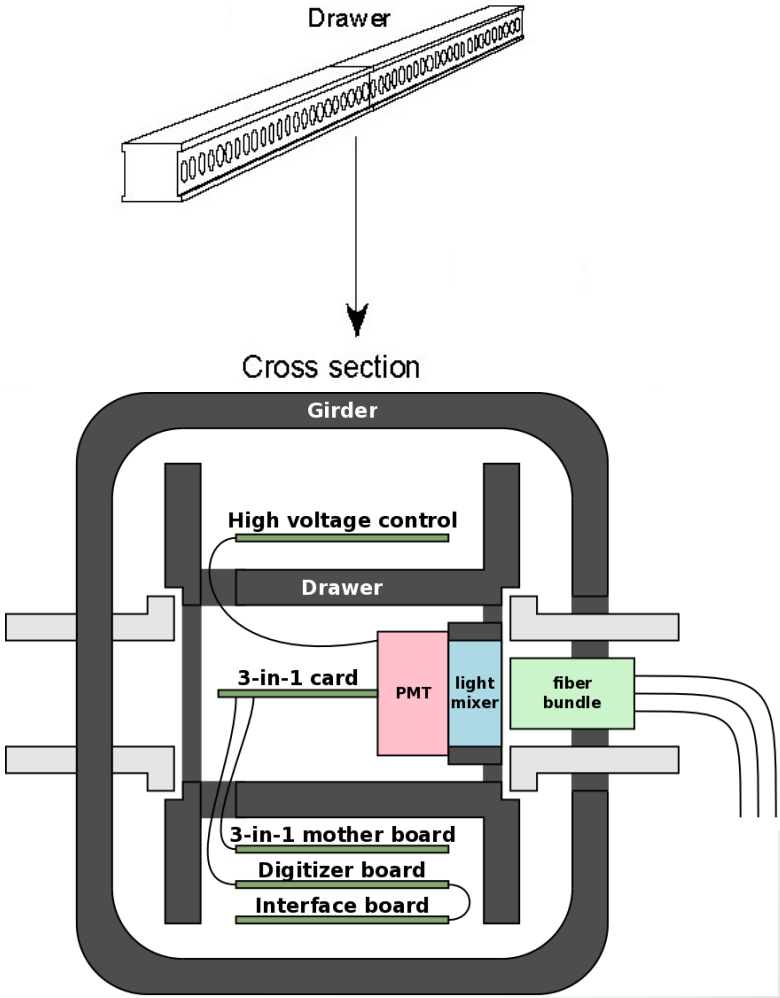


Engineers working near Extended Barrel calorimeters

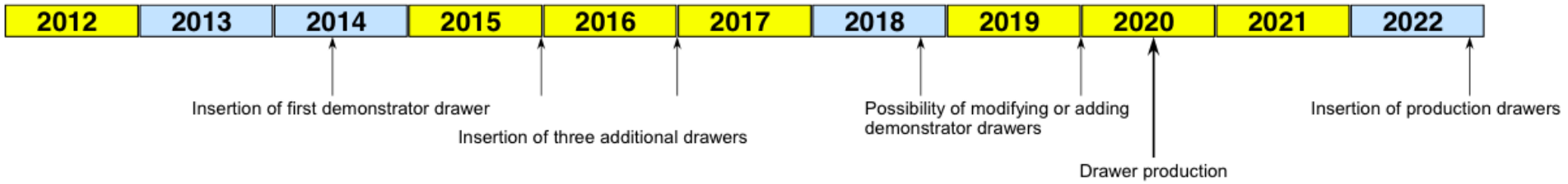
Front-end electronics drawer



- Up to 45 PMT Blocks with HV bases
- Up to 45 3-in1 cards (shaper-amplifier-integrator board)
- 4 motherboards
- 8 digitizer boards
- one optical interface board
- one TTC receiver mezzanine card
- up to 10 analog summing cards
- one integrator readout board
- HV distribution boards
- LV distribution and sense adapters

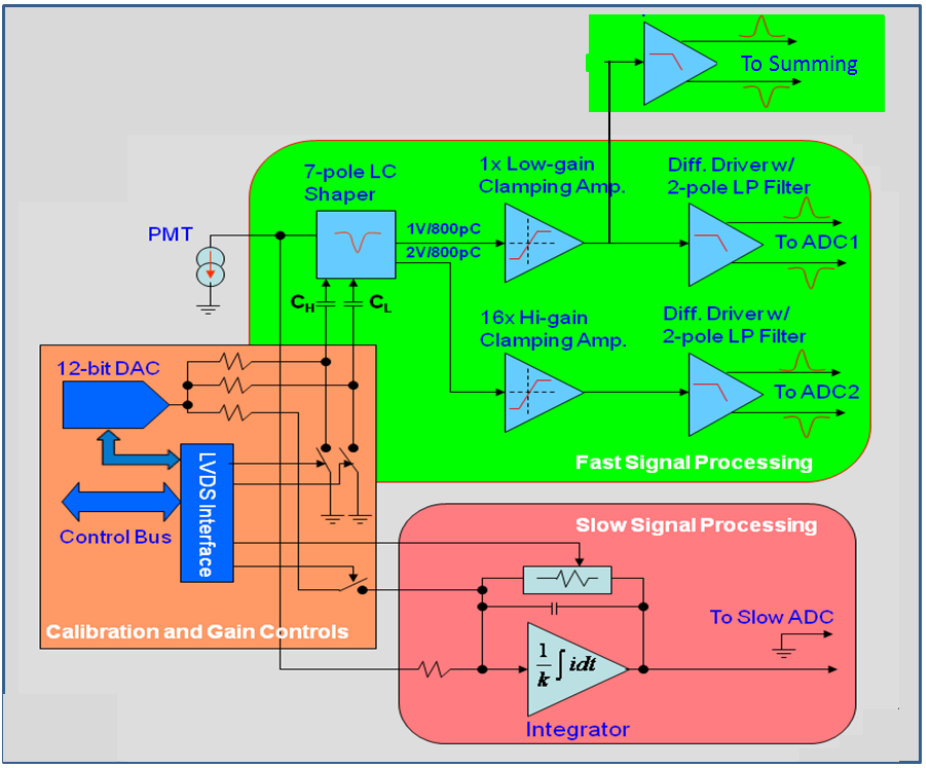


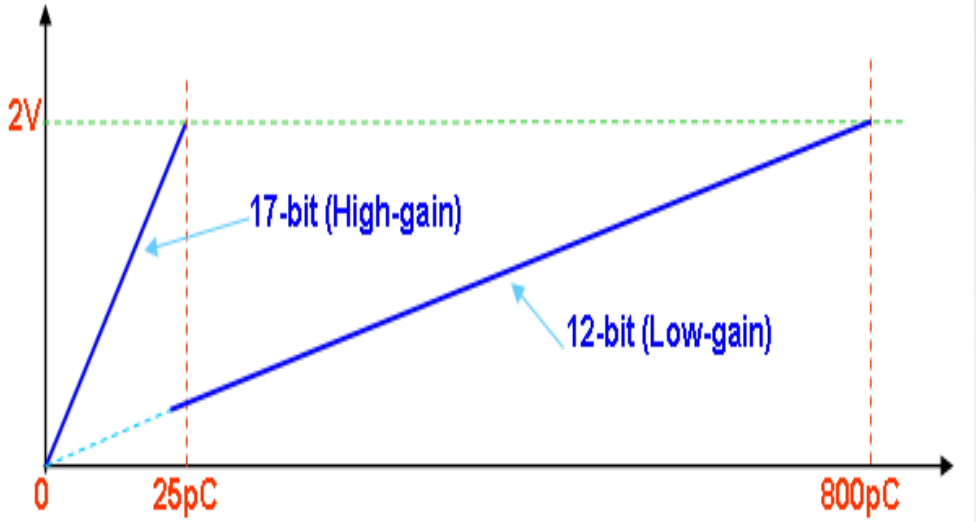
Tile upgrade timeline

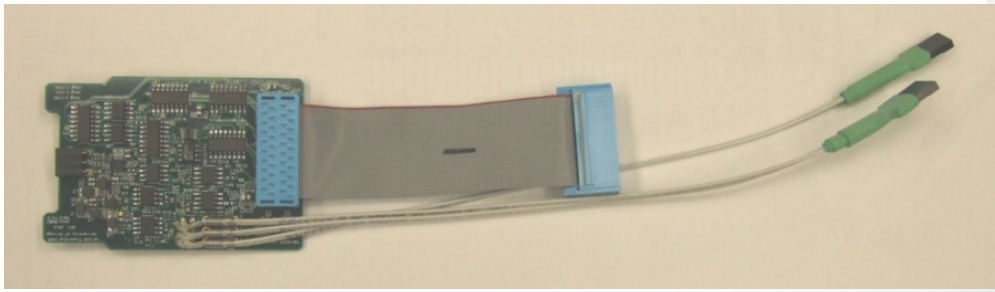


- Replace front end and back end electronics in phase 2 (except PMTs):
  - New readout architecture
  - Full data digitization at 40 MHz and transmission to off-detector system
  - Cell digital information to the L1/L0 trigger
  - Improve reliability (reduce connections, reinforce redundancy)
  - Improve LVPS system (point of load regulators)
- Install first demonstrator in Tile Cal Spring 2014
- Final front end choice based on test-beam results (2014-2016)

FEE option: new 3in1

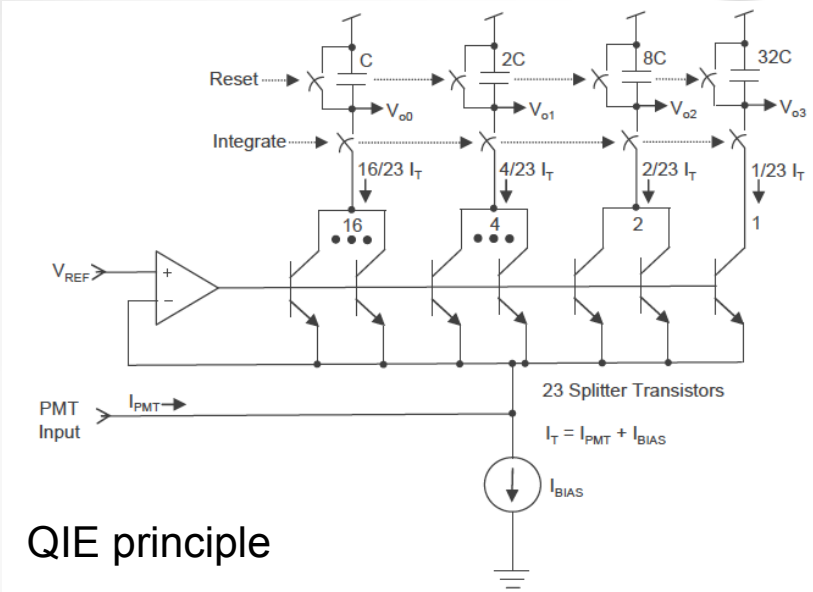




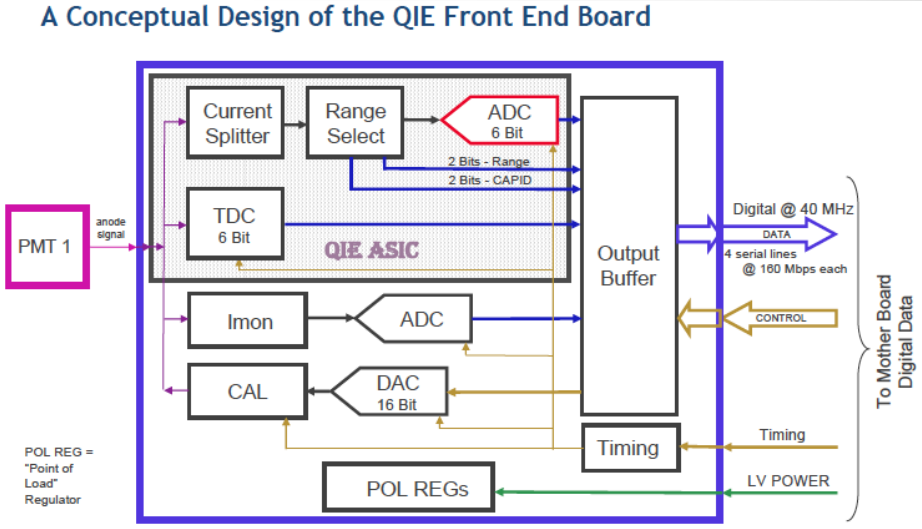


- Fast signal processing
  - 7-pole LC shaper and bi-gain clamping amplifiers with gain ratio of 32
- Slow signal processing
  - 6-gain integrator for Cs calibration and monitoring minimum bias current of proton-proton collisions
- Charge injection calibration and controls
- Retain analog trigger capability for Demonstrator

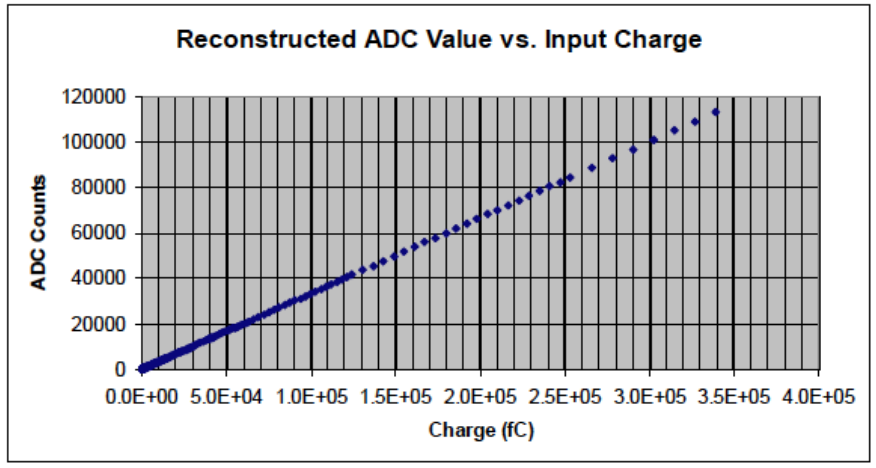
FEE option: QIE



QIE principle

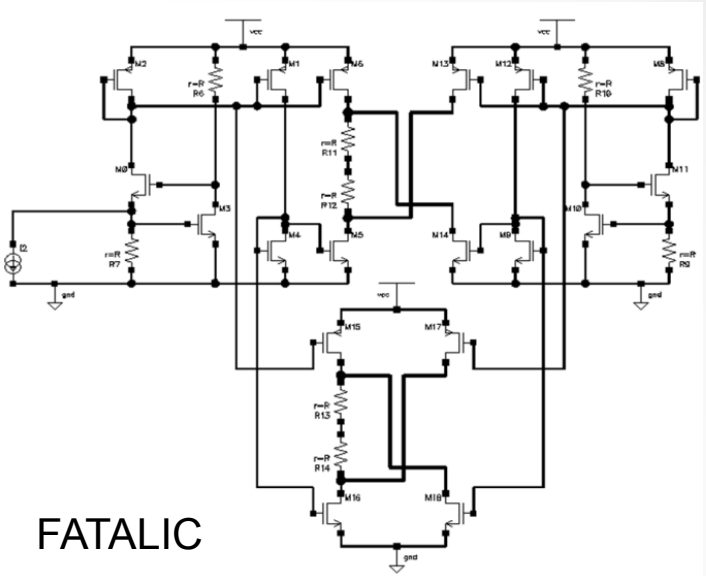


- Charge integrator
  - 4 clock cycles to acquire the data
- Data Output : 10 bits encodes a 17-bit dynamic range
  - 6-bit ADC value, 2 bits range (4 ranges), 2 bits CAPID
- Version 10.5 under evaluation
  - fully-functional, including data drivers and TDC

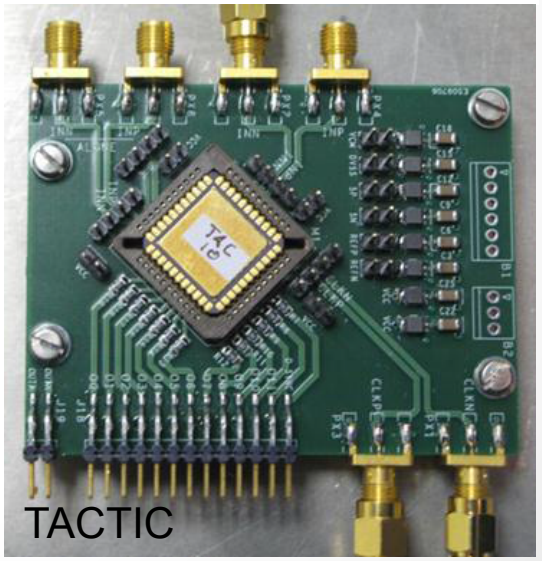


FEE option: ASIC

- Based on the FATALIC chip family + TACTIC ADC
  - Current conveyor concept
- IBM 130 nm technology. Shaping, 3 gain ranges (1, 8, 64)
- First prototypes (FATALIC 1/2) tested
- Version FATALIC 3 is being tested
- Validation of the current conveyor concept
- Digital integrator for the Cesium calibration
- TACTIC: Includes 12-bit pipeline ADC@40 MHz
  - Best resolution and speed

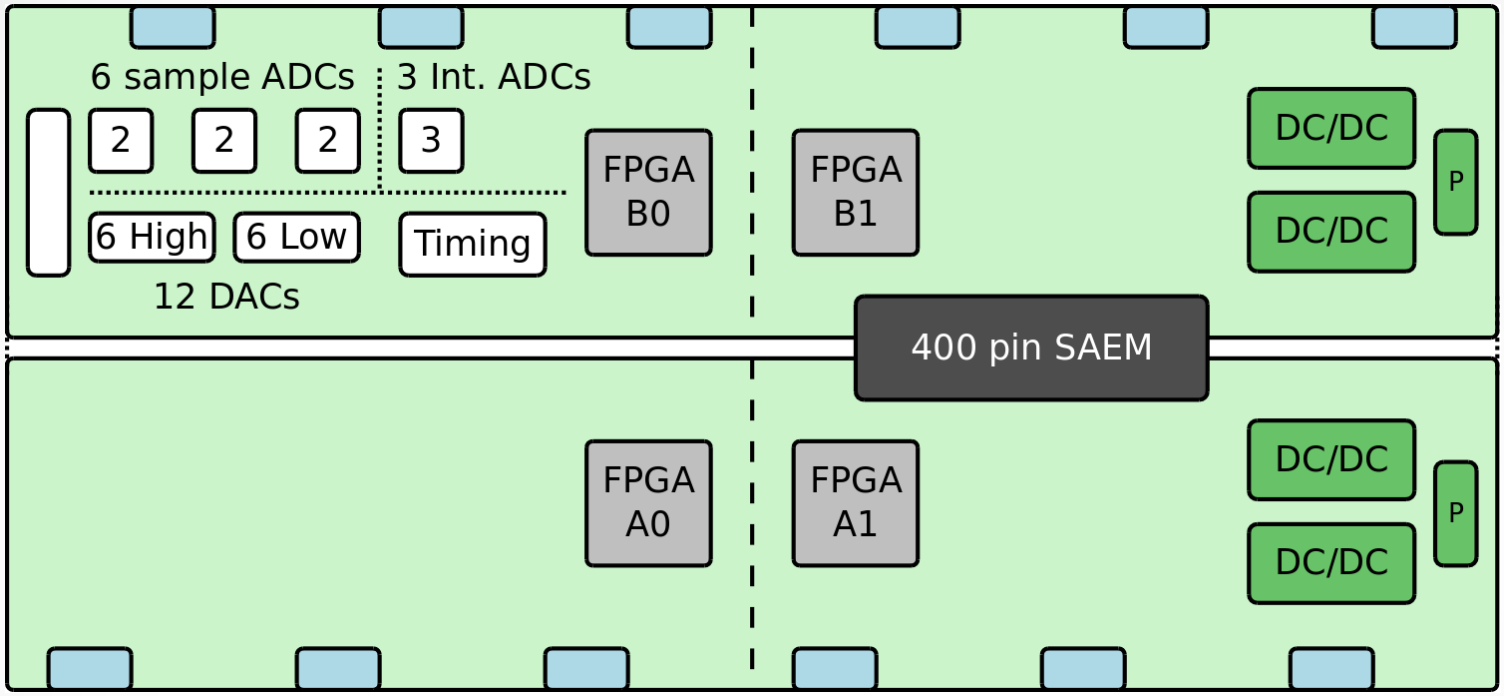


FATALIC



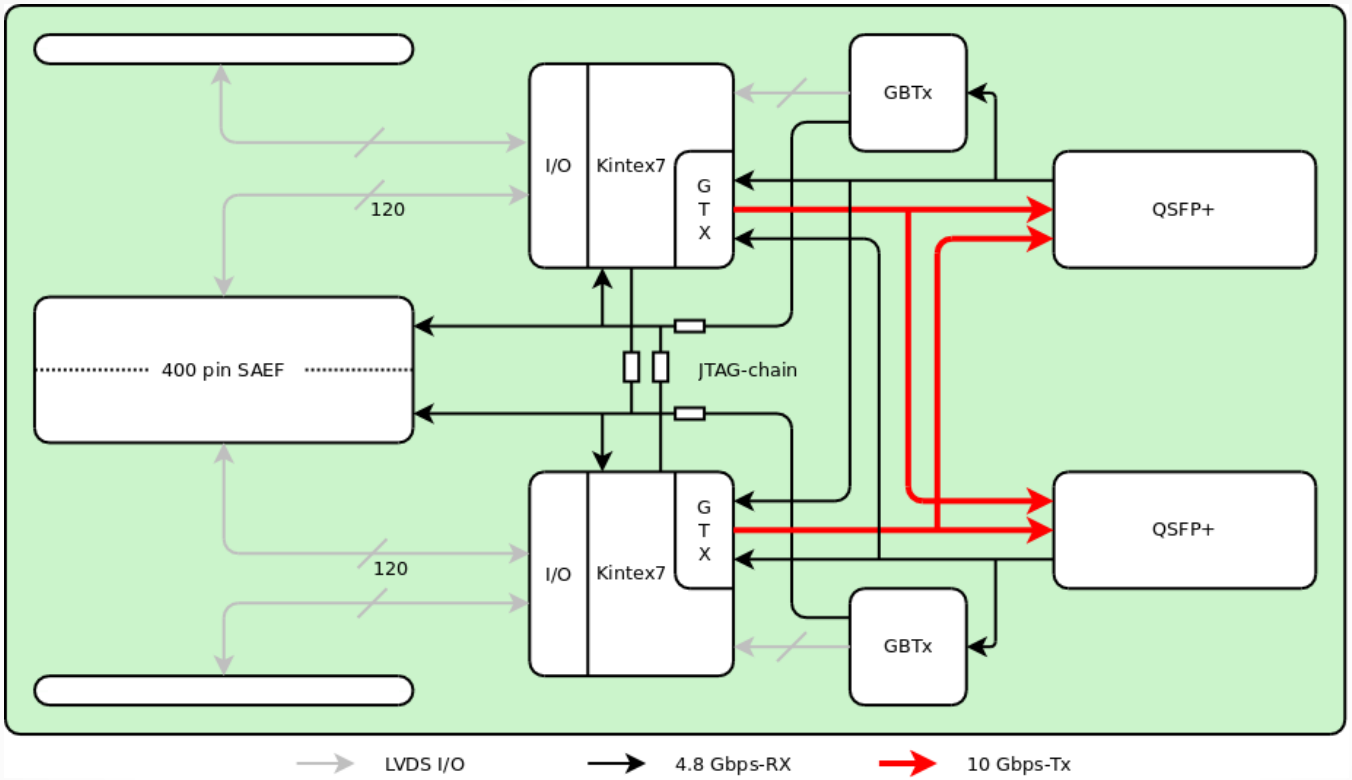
TACTIC

Mainboard



- Mainboard digitises signals from FEBs with independent discrete ADCs
  - Mainboard is split into two halves
  - Each cell will be read-out by two PMTs, one on each side of the mainboard
  - Samples are transferred serially to the daughterboard at 600 MHz
  - Commands are sent in parallel to 2 control FPGAs on each side

Daughterboard



- Daughterboard provides GBT communication with back-end electronics
  - Implementing a **redundant** system on a single PCB + triple redundant FPGA programming
  - Two Kintex 7 FPGAs and two QSFP Modulators at 40 Gb/s
  - Firmware can be also uploaded through the optical link
  - Two GBTx chips

Cs electronics upgrade

- An upgrade of the Cesium control electronics and readout chain is needed
- All good features and performance of the current system should be preserved and improved where possible
- Integration of the Cs control data flow into the new drawer electronics (via GBT-CAN/SPI link)
- First prototypes of upgraded boards have been tested
- Special test-boards with perspective components for radiation hardness tests are being designed