Super CT factory electronics and trigger concept



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Super CT factory workshop 26 - 27 May 2018

Collider important parameters

- The RF frequency is about 508 MHz.
- The period of bunch circulation is $2.557 \ \mu s$.
- The quantity of separatrices is 1300.
- The time gap between bunches is around 6 ns (filling each third separatrix).
- The mode with 8 ns gap is under discussions (filling each fourth separatrix).
- The maximum quantity of bunches in train is 390.
- The gap of 5-10% (130 separatrices) in a bunch train is necessary for suppression of the ion instability.



27.05.2018

Subdetector parameters

Detector	Channel	Channel size	Power	Trigger	Type of information
VD – GEM – Timepix	56 K 10 M	2 x 2 mm ² 150 x 150 μm ²	1 kW	Possibly	Amplitude (A), Time (T), Position (P)
DC	7.1 K	12 x 20 mm ²	2 kW	Yes	A, T, P
FARICH	1 M	4.5 x 4.5 x 50 mm ³	100 kW (21 m ²)	No	Т, Р
Calorimeter	7.5 K	$(40 - 70)^2$ mm ²	2 kW	Yes	A, T, P
Mu	4 - 44 K	\varnothing 20 mm	1 – 9 kW	Yes	Т, Р

- Analog-to-digit conversions inside the detector
- Data transfer over the optical links
- Wide using of ASIC (application-specific integrated circuit)
- Water cooling of the Front-End electronics

ATLAS LAr FEB SCA



Parameters of signals and FrontEnd electronics

Detector	Channel load	Duration of signals	Sampling rate	Bit quantity of ADC (TDC)	Time measure precision
VD	33 kHz	Rising edge 25 ns	from 20 MHz to 80 MHz	10 -12 bit ADC	1 ns
DC	50 kHz	Rising edge 100-200 ns, Falling edge – 300 ns	50 MHz (ordinary mode) 500-1000 MHz (claster mode)	10 bit ADC	1 ns
FARICH	1 MHz	5 – 10 ns	TDC	6 bits (for 8 ns) TDC	200 ps
Calorimeter	15 kHz	30 ns for clear CsI	40 – 50 MHz	18 bit ADC	1 ns
Mu	100 kHz	30 – 200 ns	TDC	11-12 bit TDC	60 ps

Rates in J/ψ at luminosity 10^{35} sm⁻²s⁻¹:

- events 260 kHz
- Bhabha 90 kHz
- cosmic 2 kHz
- Backgound several tens of kHz
- \blacktriangleright The maximum readout rate up to 400 kHz
- ➢ The event size 30 KB

The electronics block diagram



ASICs in FrontEnd electronics

Different ASICs in ATLAS LAr FEB

ASIC Type	Process	ASIC	Die Size (mm ²)	
Analog	AMS BiCMOS	Shaper	18	
	DMILL	SCA	19.8	
		SMUX	16	
	DMILL	SPAC slave	27	
Digital		CONFIG	31	
		GSEL	16	
	DSM	CLKFO	4	
		SCAC	16	

ATLAS LAr FEB



ASICs in BINP

DMXS6A



- DMXG64B is being used in fast gaseous coordinate X-ray detector DIMEX-4
- DMXS6A obtained first experimental results with Si coordinate X-ray detector DIMEX-4SI
- CTCALFE2A chip prototype for CTau calorimeter Front-end electronics - under development

CT-factory electronics and trigger

Optical data transmission lines

Detector	Channel	Data link	Trigger link
	quantity	quantity	quantity
VD – GEM	56 K	56	56
– pixel	10 M		
DC	7.1 К	48	48
FARICH	1 M	100	0
Calorimeter	7.5 К	32	32
Mu	4 - 44 K	32	32

Data links – 268 Trigger links – 168





10Gb/s SFP+ Transceiver



Size 56*14*12 mm Power 3.3 V Consumption < 1 W Price in 2010 - \$550 in 2018 - \$80

CT-factory electronics and trigger

ReadOut Processor (ROP)





- The ROP can be equipped from 2 to 8 optical inputs
- 134 ROPs are necessary for 268 optical links

BackEnd electronics location

- 134 ROPs occupy 10 VME crates
- 10 crates => 4-5 racks
- Power consumption of crate ~1 kW
- rack 2-3 kW



ATLAS BackEnd electronics



L1 Trigger



CT-factory electronics and trigger

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L1 Trigger

Requirements

- Maximal rate of L1 is 500 kHz
- Dead time < 100 ns
- Decision time (latency) $-2-3 \ \mu s$

Information

- Quantity of tracks in tracking systems
- Positions of tracks
- Energy deposition in calorimeter
- Quantity of clusters
- Position of clusters
- Muon system information

Hardware

- 168 optical links, 2-4 links per preprocessor
- => 84 42 preprocessors
- => 6-3 crates
- => 2-1 racks
- VME or ATCA

CT-factory electronics and trigger

Prototypes of electronics for FARICH

Parameter	Value	Comment
Resolution	1.19 ns	1/840 MHz sample rate
Dead time	4.76 ns	4 samples = 4/840 MHz
Maximal time interval	19504 ns	14 bit
Number of input channels	32	
Channel FIFO buffer size	256 events	
Shared memory size	4096 events	
Input signal level	LVDS	





Prototypes of electronics for CTau calorimeter

- Quantity of channels 32
- 8 channel ADC
- ADC sampling rate 50 MHz
- ADC resolution 14 bits
- Variable gain amplifiers
- Total dynamical range 17 bits
- Linearity < 0.2 %
- CTCALFE2A ASIC (under development)







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27.05.2018

Cooling of ATLAS LAr FEB





ATLAS LAr FEC structure



Cooling of ATLAS LAr BackEnd electronics





Cooling of Babar DC FrontEnd electronics









Thank you for attention





