TRB3 Platform Developments

Cahit Uğur
on behalf of the TRB3 collaboration

GSI Helmholtz Centre for Heavy Ion Research, Darmstadt – Germany

International Workshop on Antiproton Physics and Technology at FAIR
19 November 2015, Novosibirsk

Jagiellonian University in Kraków

GSI

Johannes Gutenberg Universität Mainz

Goethe Universität Frankfurt am Main

- Multi-purpose FPGA based TDC platform with 64 channels on each FPGA
- Leading edge time precision <12ps RMS on every channel
- ToT measurement on a single channel <15ps RMS
- Very stable data transfer over two 1 GbE links
- Mature DAQ and slow control protocol - TRBNET
- Existing software for eventbuilding, unpacking, calibration and analysis
- Existing FEE and AddOn boards
- Reached a (known)bug-free state

BACK TO THE BEGINNING

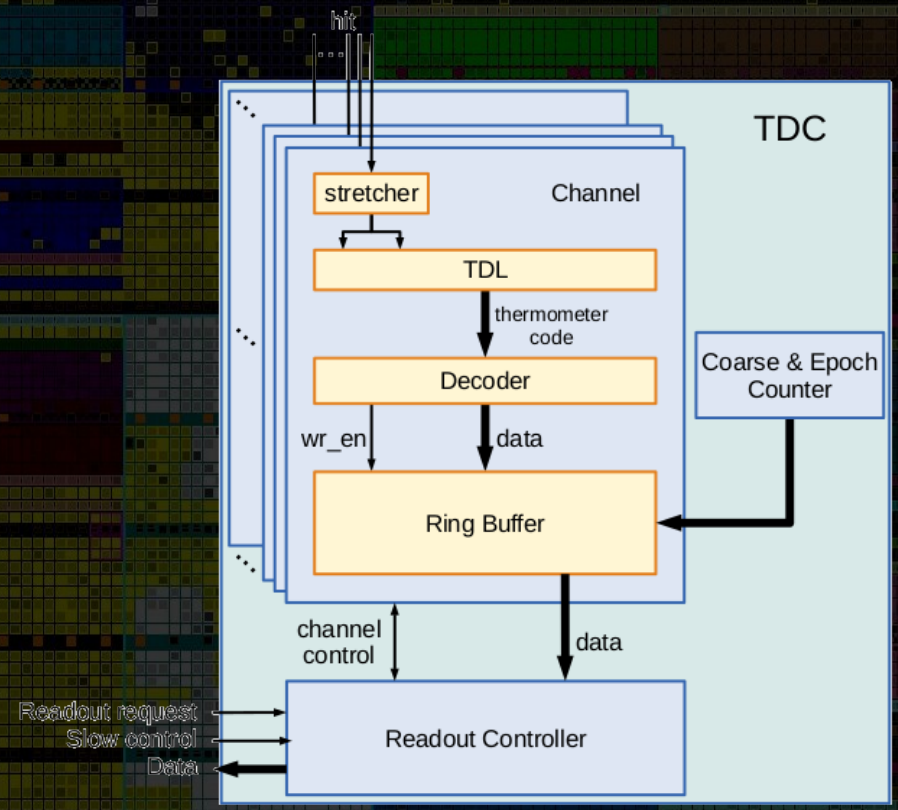
- Outline
- Concept
- TRB3 Platform: Hardware
  - Time digitisation with FPGAs
  - Amplitude digitisation with FPGAs
  - Charge digitisation with FPGAs
- TRB3 Platform: Software
- Applications

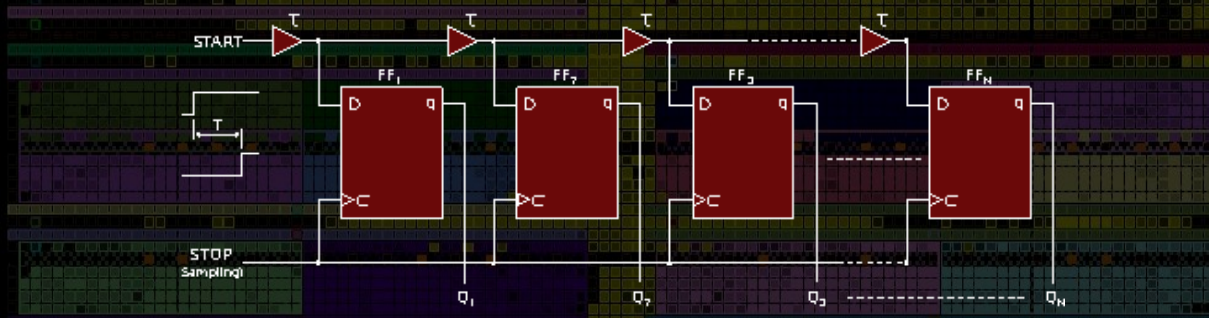
- Only commercial components
  - easily available, industrial quality in design and package
  - not producer dependent, like commodities
- Off the shelf FPGAs as FEE
  - fully configurable
  - high number of resources
- Possible to “misuse” resources
  - intrinsic delays for time measurements
  - LVDS receivers as discriminators
- Possible to alter the setup for different measurements
  - external pulser for amplitude measurements
  - signal integration for charge measurements

Tapped Delay Line
- Delay line: time → digital
- Register array: snapshot of delay line
- Common stop: 200MHz clock
- Calibration: code density test

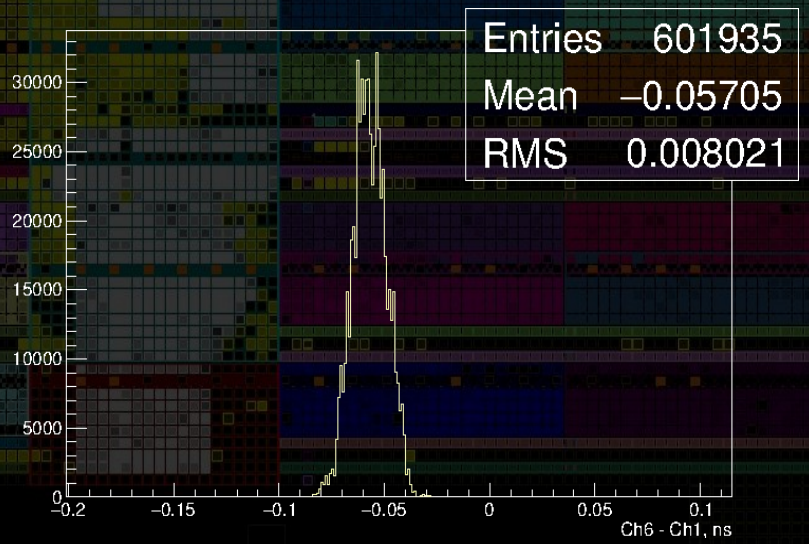
Time flag
- Coarse counter 5ns
- Epoch counter 10.24us

Stretcher short pulses & double edge
Decoder thermocode → binary
Ring buffer dynamic size

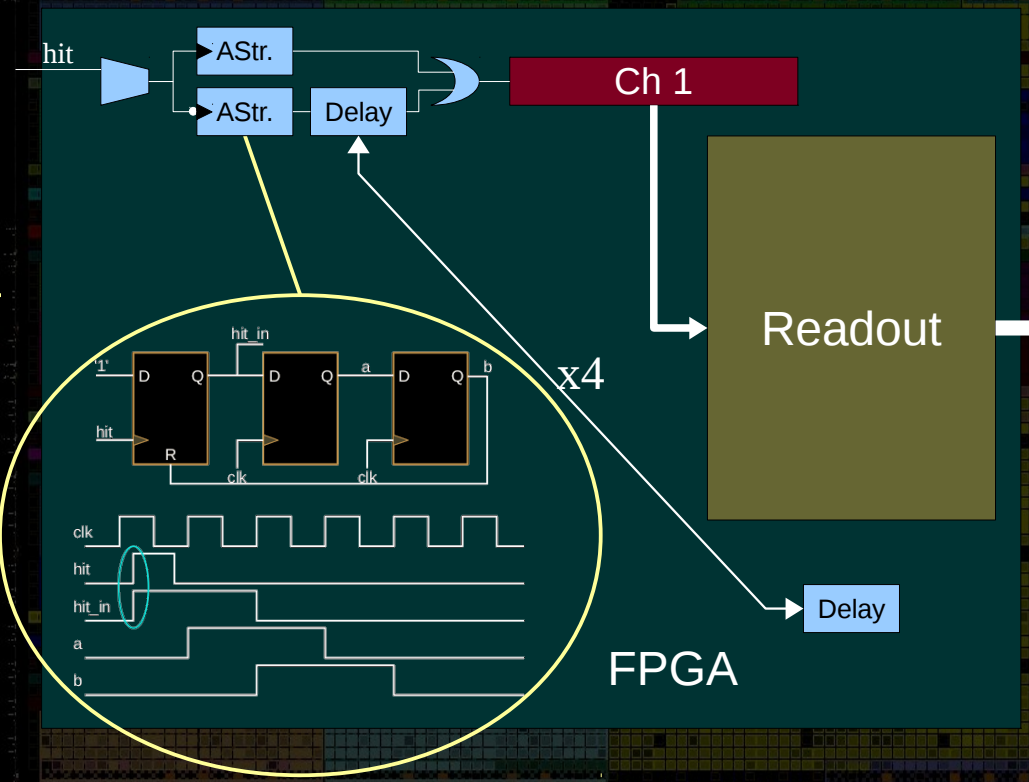




Tapped Delay Line method with common stop signal



Novel ToT Measurement



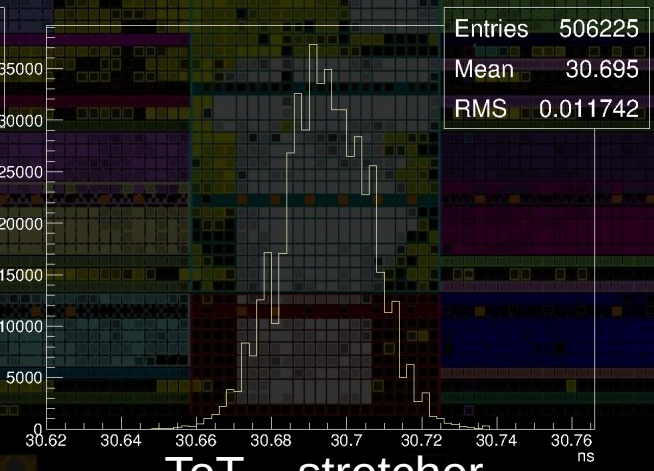
Advantages

- Double number of channels: 65ch
- %30 less data load
- High precision maintained

Disadvantages

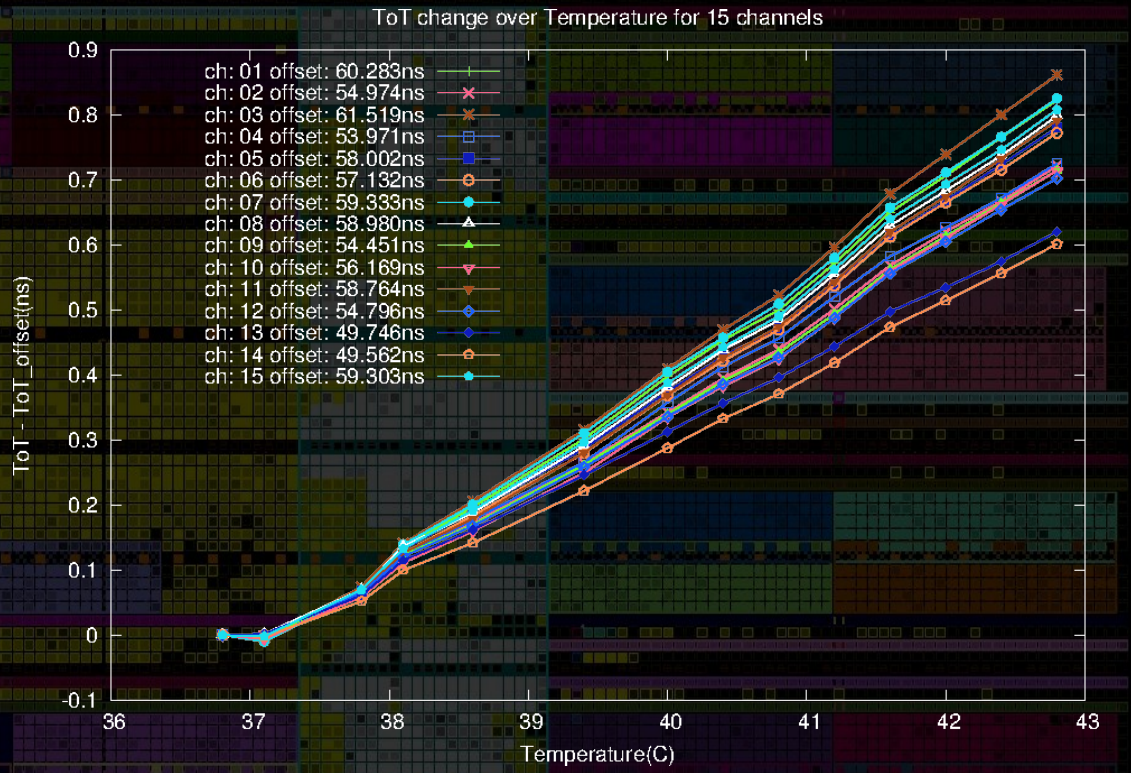
- Longer dead time ~70ns
- No multi-hit capability
- Stretcher offset

ToT – alternating channels

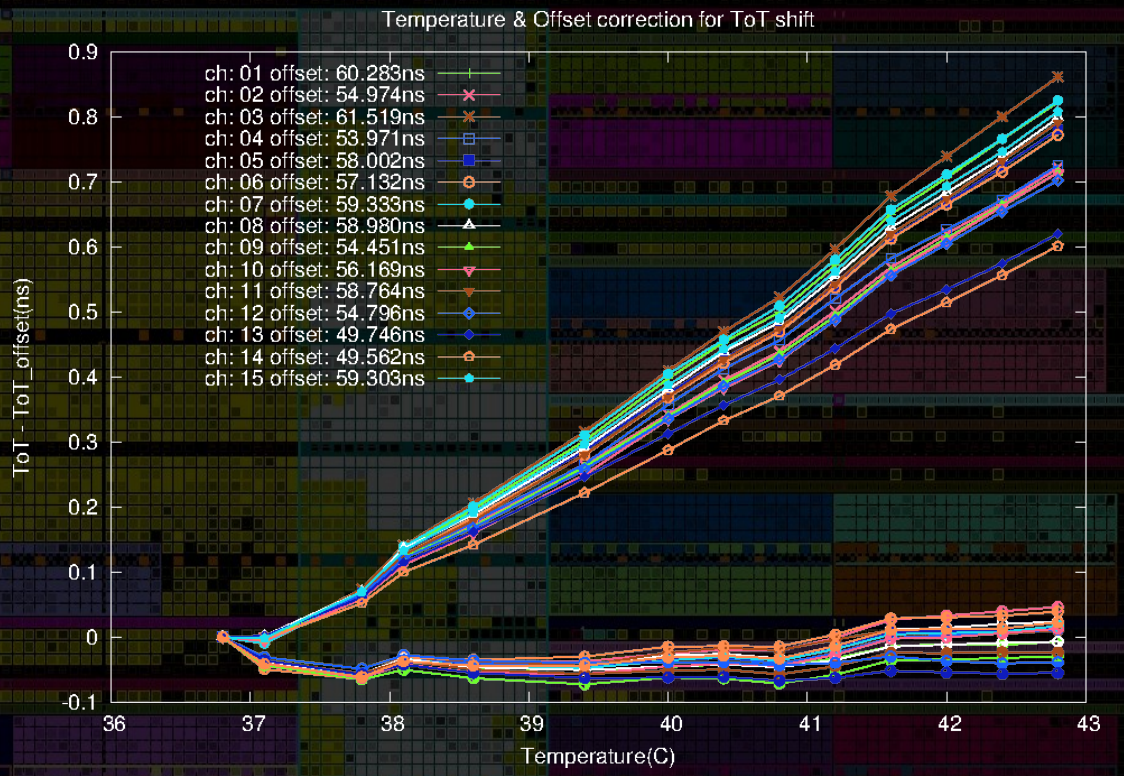


ToT – stretcher

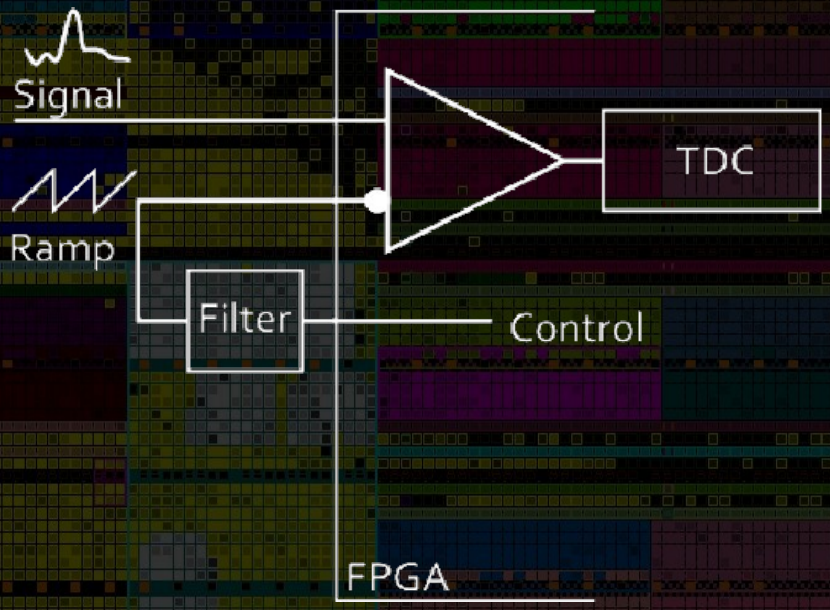
- Strong temperature dependency (0.4%/K) in ToT value due to the long signal stretching
- Different for each channel



- Strong temperature dependency (0.4%/K) in ToT value due to the long signal stretching
- Different for each channel
- Luckily can be corrected with a simple model
- $ToT' = ToT_m - k_T * \Delta T * k_O * ToT_i$
- After correction 65ps shift over 6K



- A periodic ramp signal is applied to the reference pin of an LVDS buffer
- Input signal is applied to the other input
- Measure time until reference crosses input signal
- 10bit ADC, 20MSPS needs 31ps time precision
- Advantage: many channels in one FPGA (one ramp generator), no data transfer to the FPGA, low power



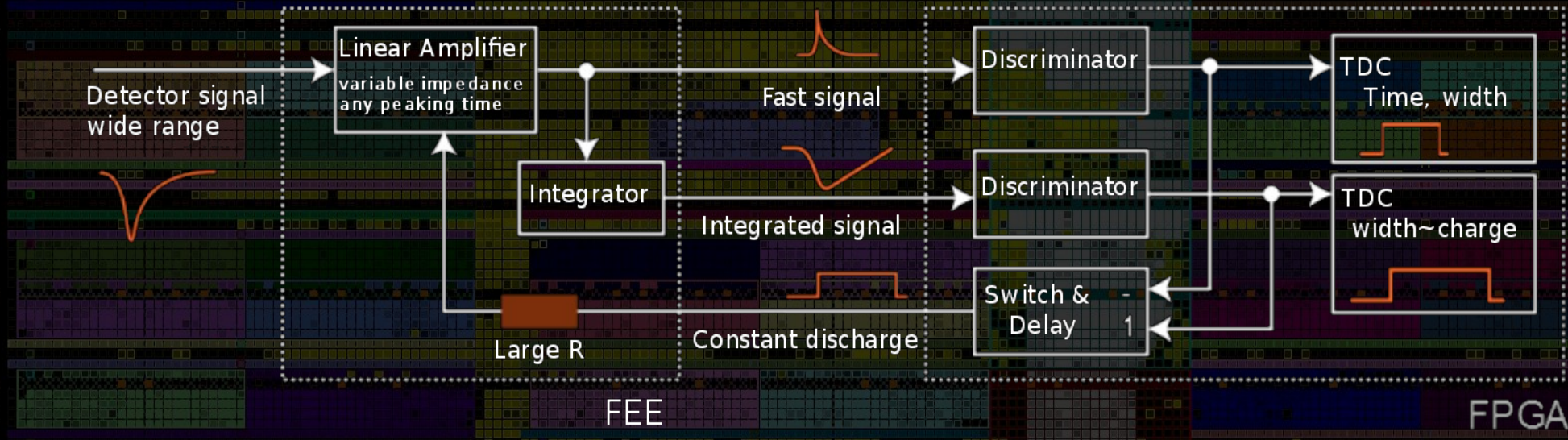
ch2 level [mV]	Mean [ps]	Jitter (RMS) [ps]
400	2551	50
800	3034	24
1200	3538	18
1600	4125	15

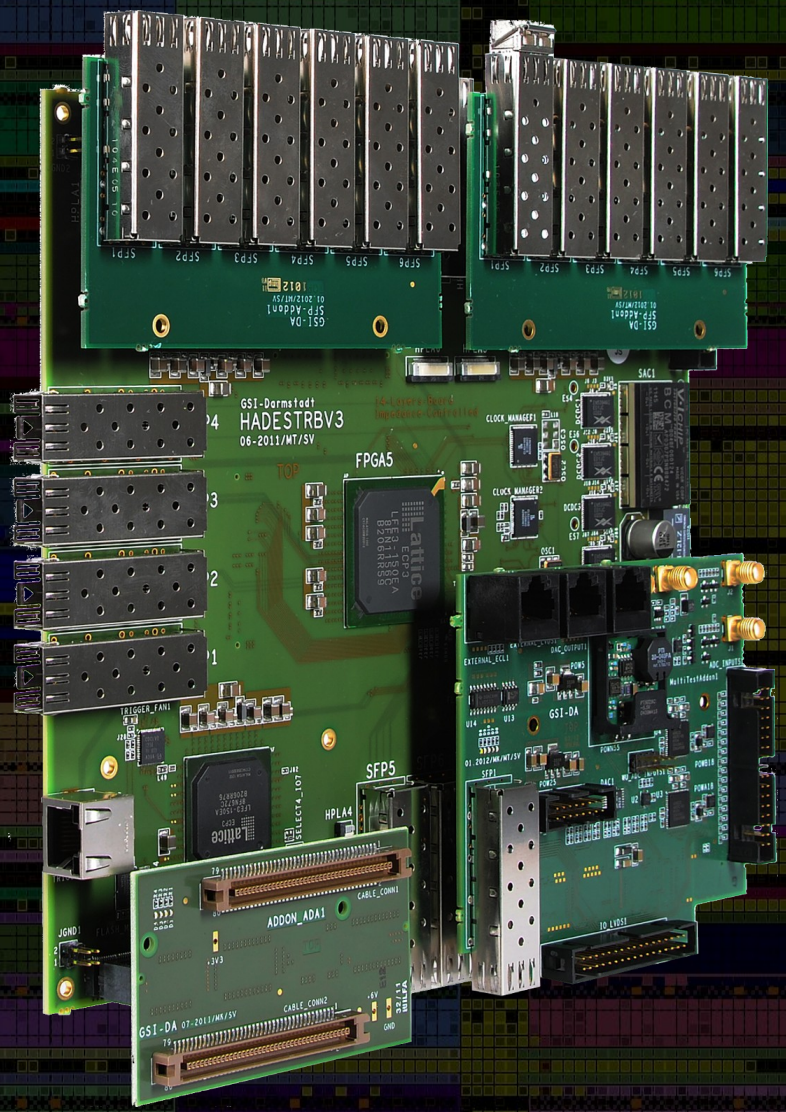
Measurements with externally generated ramp signal show that

- the ADC concept works
- the measured TDC time precision for 26ps ramps is compatible with an ADC with 10 bits precision and 20 MSPS
- An addon board with a ramp generator is being implemented for evaluation

Idea: Modified Wilkinson ADC

- The input signal is integrated with a capacitor
- The capacitor is discharged using a current source → fast crossing of zero
- Measure time necessary to reach zero

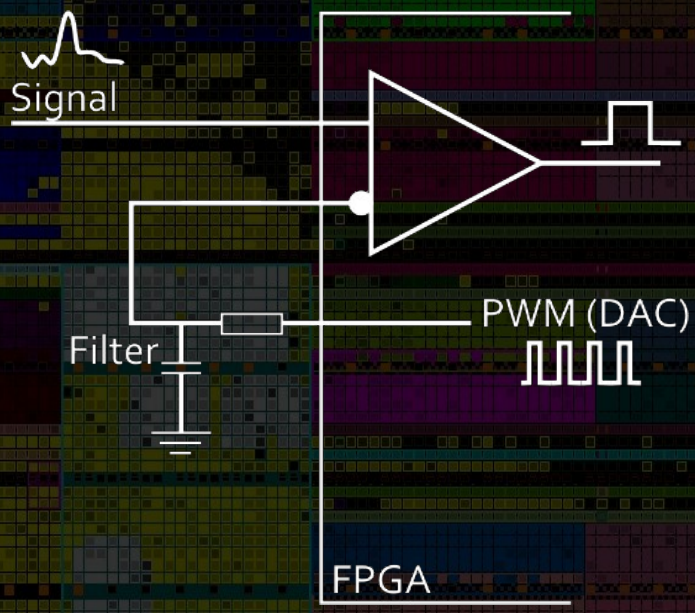


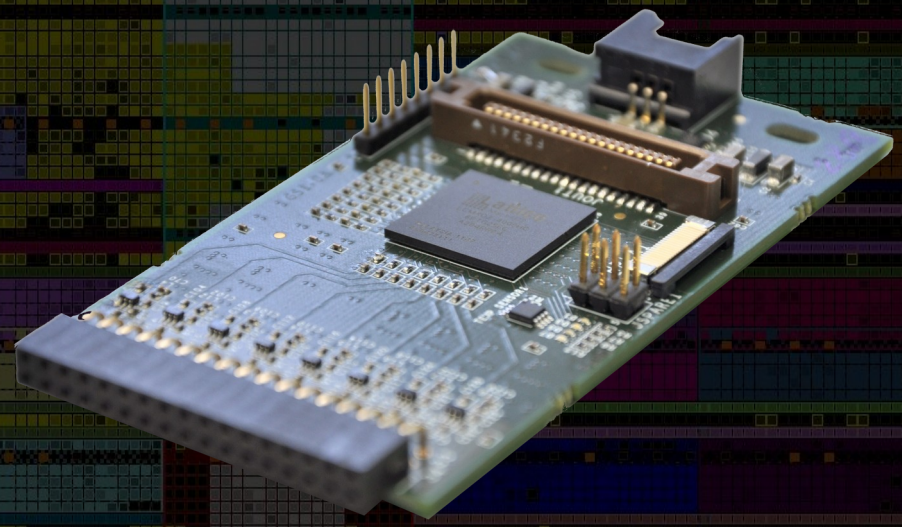


TRB3: the TRB3 collaboration
Photo by Gaby Otto, GSI Darmstadt, 06.09.2012.

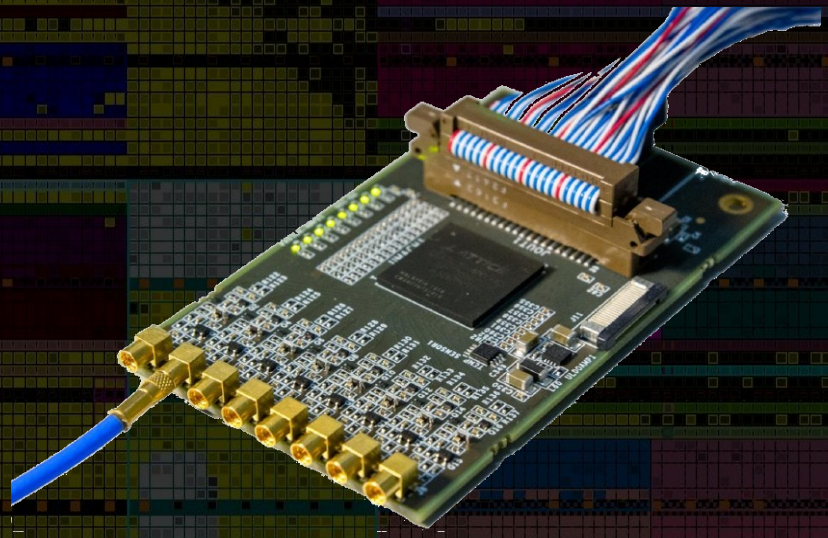
- platform for TDC measurements and data readout
- developed firmwares and software
- 4 peripheral FPGAs with 256 TDC channels
- central FPGA as CTS & GbE controller
- flexible with many addons
- 8-12 ps leading edge time precision
- 10-15ps ToT time precision
- 40 MHz max. hit rate (burst)
- 140MB/s data readout via 2 GbE links

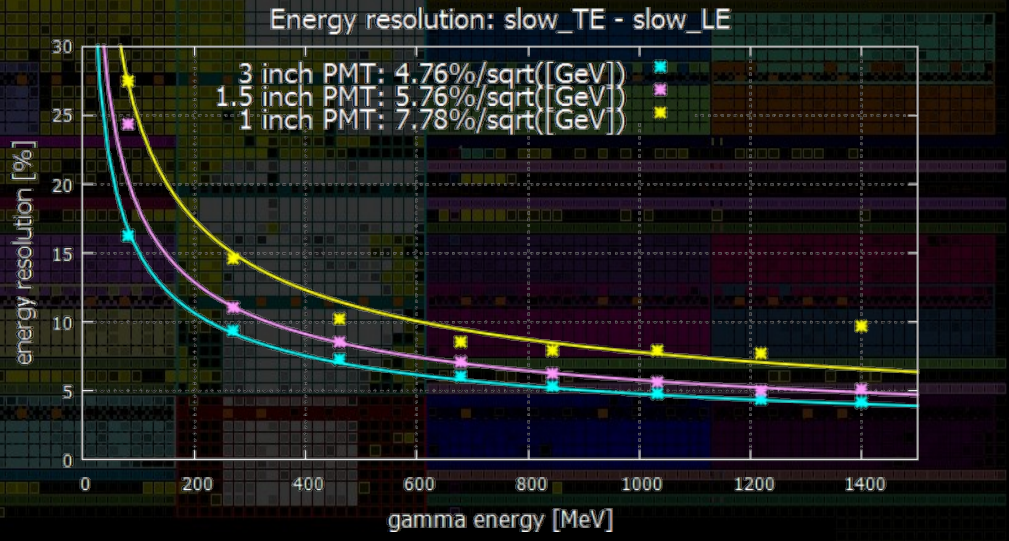
- FEE for leading edge and ToT measurement
- Pre-amplification, discrimination, threshold setting, ToT encoding in the pulse width
- Placed directly at the detector, no cable, only digital signals are sent out
- Pulser test: ~23 ps
- Single photoelectron laser test with MCP: ~70ps
- Tested in many Barrel DIRC test beam times



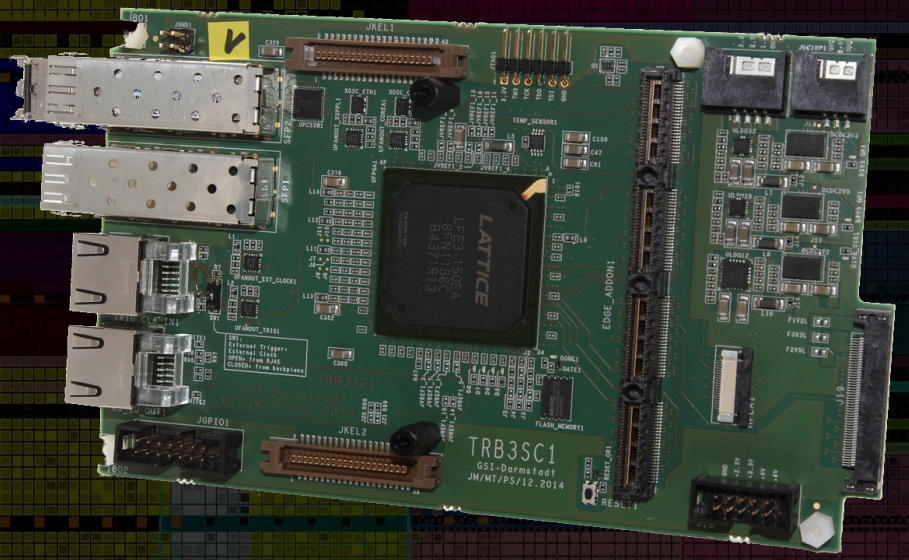


- FEE for charge measurement
- Signal is integrated, charge is encoded in pulse width
- Tested in lab with pulser and in gamma beam in Mainz (MAMI)
- Charge precision in lab: 0.5% (no walk correction)
- Charge precision: as low as 5% (no walk correction)
- Further investigations are ongoing

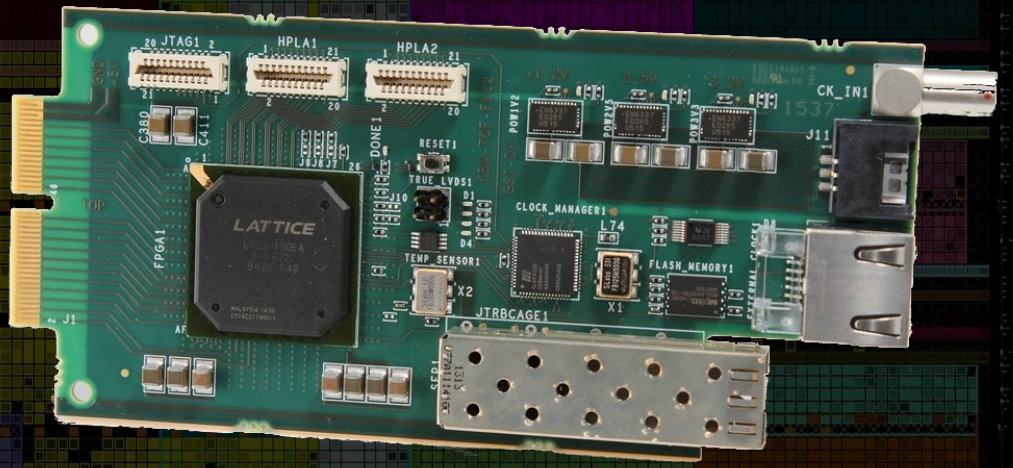




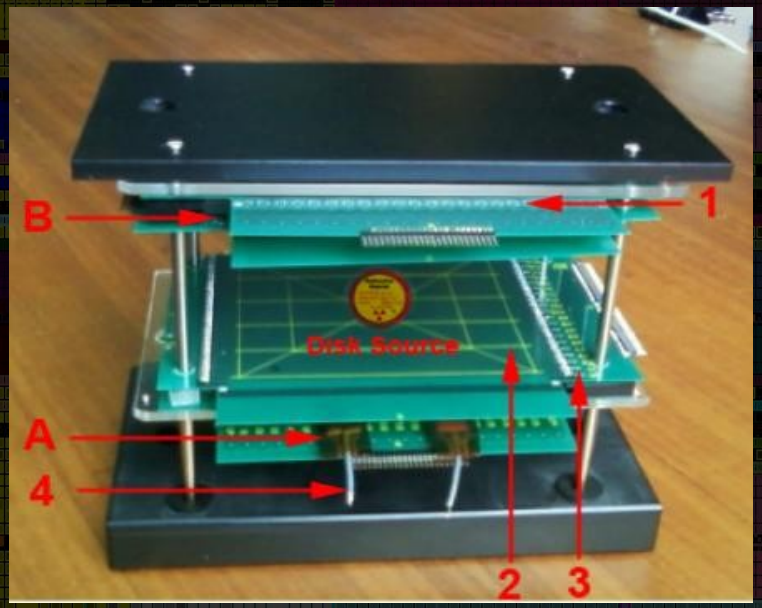
- Optimised power supply: low-noise DC-DC converters or pure linear regulation
- Additional I/O: 40 differential I/O lines in addition to any AddOn board
- Adaptable read-out band-width: 1 GbE link per crate (9 boards) or up to two GbE links for each board
- Stand-alone operation or mounting in crate (3U, 180mm deep) possible
- Additional fast Serdes connection: AddOns can use up to 8 Serdes links in addition to 4 connections via backplane and 2 SFPs
- Flexible clocking: Internal oscillator, external via backplane, external via cable
- Compatible to all existing AddOns



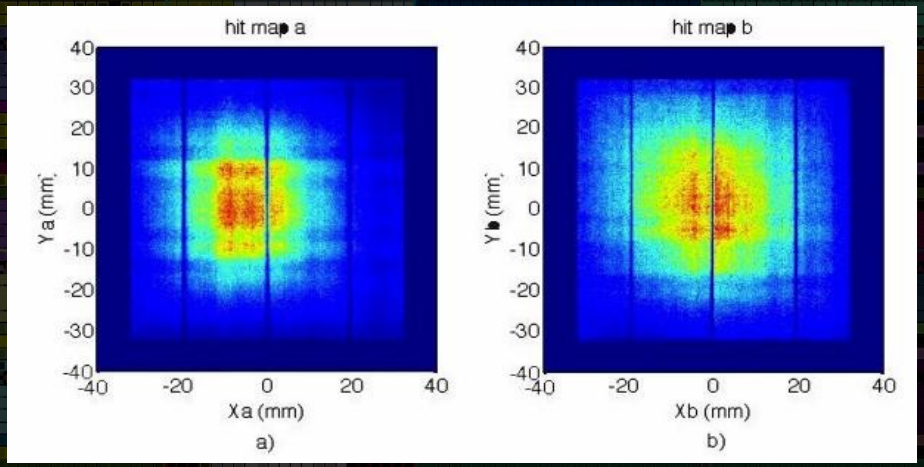
- A quarter of a TRB3 in a small form factor
- 32 differential I/O lines
- 64 TDC channels for ToT measurements
- 1 GbE link for read-out
- External or internal clock
- Fully compatible with the TRB3 system
- Very good time resolution <12ps RMS
- Tested in many CBM-TOF test beam times – also next week @CERN



- Positron Emission Tomography (PET) for molecular imaging
- Approach is RPC (Resistive Plate Chambers) based
- Simulations suggest factor 8 better performance over the best commercial tomography [1][2]
- Animal PET Prototype demonstrated 0.4 mm image resolution with TRB2 [3]
- Prototype for high resolution animal PET scanner and low sensitivity (for cost reasons) whole body human scanner is under development



A-detector a; B-detector b; I-X strips; 2-Y strips; 3-signal division network; 4-high voltage connections. [3]

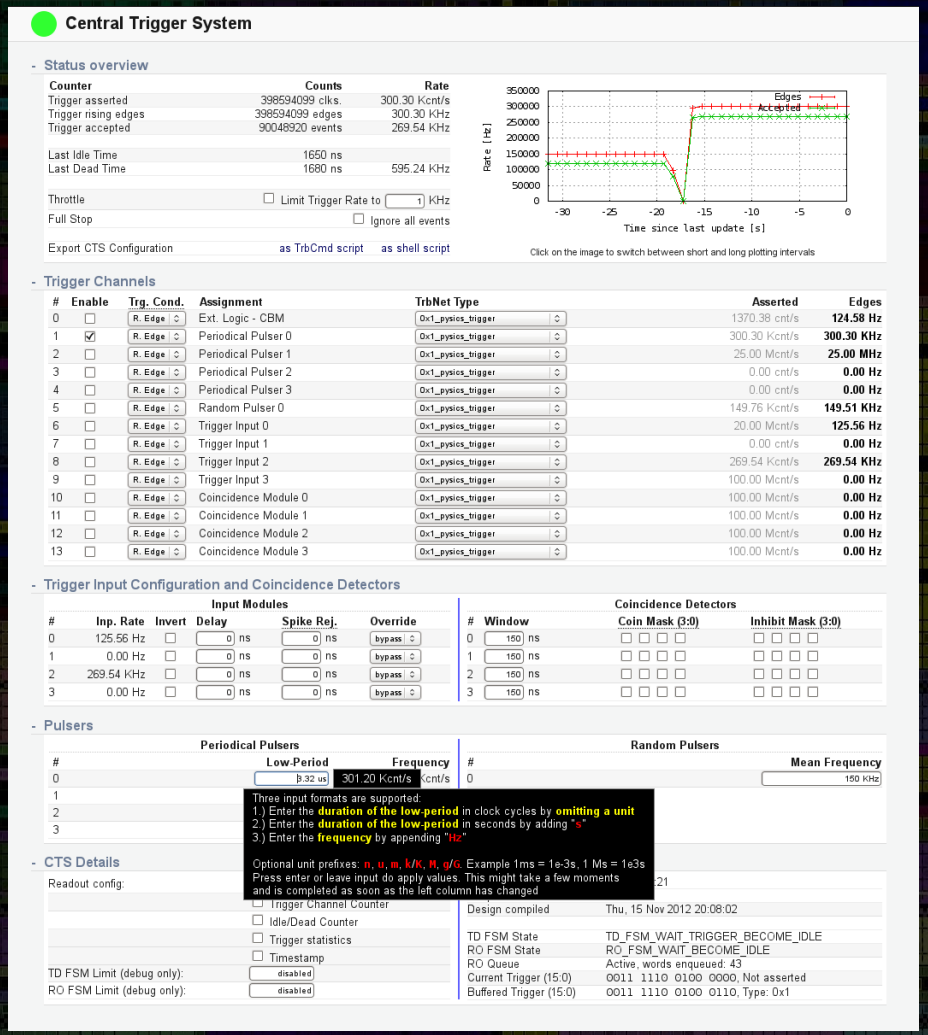


Hit map in a) detector a, and in b) detector b. The shadowed vertical lines correspond to the 0.35 mm spacers used to define the gap width. [3]

[1] A. Blanco et al., Nucl. Instr. and Meth. A602 (2009) 780;

[2] M. Couceiro et al., 2012 IEEE Nucl. Sci. Symp. Conf. Record (2012) 2651;

[3] P. Martins et al., 2012 IEEE Nucl. Sci. Symp. Conf. Record (2012) 3760



Central Trigger System

- Status overview

Counter	Counts	Rate
Trigger asserted	398594099 clks.	300.30 Kcnt/s
Trigger rising edges	398594099 edges	300.30 KHz
Trigger accepted	90048920 events	269.54 KHz
Last Idle Time	1650 ns	
Last Dead Time	1680 ns	595.24 KHz

Throttle: Limit Trigger Rate to 1 KHz
Full Stop: Ignore all events
Export CTS Configuration: as TrbCmd script | as shell script

Click on the image to switch between short and long plotting intervals

- Trigger Channels

#	Enable	Trg. Cond.	Assignment	TrbNet Type	Asserted	Edges
0	☐	R. Edge	Ext. Logic - CBM	0x1_pysics_trigger	1370.38 cnt/s	124.58 Hz
1	☑	R. Edge	Periodical Pulser 0	0x1_pysics_trigger	300.30 Kcnt/s	300.30 KHz
2	☐	R. Edge	Periodical Pulser 1	0x1_pysics_trigger	25.00 Mcnt/s	25.00 MHz
3	☐	R. Edge	Periodical Pulser 2	0x1_pysics_trigger	0.00 cnt/s	0.00 Hz
4	☐	R. Edge	Periodical Pulser 3	0x1_pysics_trigger	0.00 cnt/s	0.00 Hz
5	☐	R. Edge	Random Pulser 0	0x1_pysics_trigger	149.76 Kcnt/s	149.51 KHz
6	☐	R. Edge	Trigger Input 0	0x1_pysics_trigger	20.00 Mcnt/s	125.56 Hz
7	☐	R. Edge	Trigger Input 1	0x1_pysics_trigger	0.00 cnt/s	0.00 Hz
8	☐	R. Edge	Trigger Input 2	0x1_pysics_trigger	269.54 Kcnt/s	269.54 KHz
9	☐	R. Edge	Trigger Input 3	0x1_pysics_trigger	100.00 Mcnt/s	0.00 Hz
10	☐	R. Edge	Coincidence Module 0	0x1_pysics_trigger	100.00 Mcnt/s	0.00 Hz
11	☐	R. Edge	Coincidence Module 1	0x1_pysics_trigger	100.00 Mcnt/s	0.00 Hz
12	☐	R. Edge	Coincidence Module 2	0x1_pysics_trigger	100.00 Mcnt/s	0.00 Hz
13	☐	R. Edge	Coincidence Module 3	0x1_pysics_trigger	100.00 Mcnt/s	0.00 Hz

- Trigger Input Configuration and Coincidence Detectors

Input Modules

#	Inp. Rate	Invert	Delay	Spike Rej.	Override
0	125.56 Hz	☐	0 ns	0 ns	bypass
1	0.00 Hz	☐	0 ns	0 ns	bypass
2	269.54 KHz	☐	0 ns	0 ns	bypass
3	0.00 Hz	☐	0 ns	0 ns	bypass

Coincidence Detectors

#	Window	Coin Mask (3:0)	Inhibit Mask (3:0)
0	150 ns	☐☐☐☐	☐☐☐☐
1	150 ns	☐☐☐☐	☐☐☐☐
2	150 ns	☐☐☐☐	☐☐☐☐
3	150 ns	☐☐☐☐	☐☐☐☐

- Pulsers

Periodical Pulsers

#	Low-Period	Frequency
0	3.32 us	301.20 Kcnt/s
1		
2		
3		

Random Pulsers

#	Mean Frequency
0	150 KHz

Three input formats are supported:
1.) Enter the **duration of the low-period** in clock cycles by **omitting a unit**
2.) Enter the **duration of the low-period** in seconds by adding "**s**"
3.) Enter the **frequency** by appending "**Hz**"

Optional unit prefixes: **n**, **u**, **m**, **k/K**, **M**, **g/G**. Example 1ms = 1e-3s, 1 Ms = 1e3s
Press enter or leave input do apply values. This might take a few moments and is completed as soon as the left column has changed

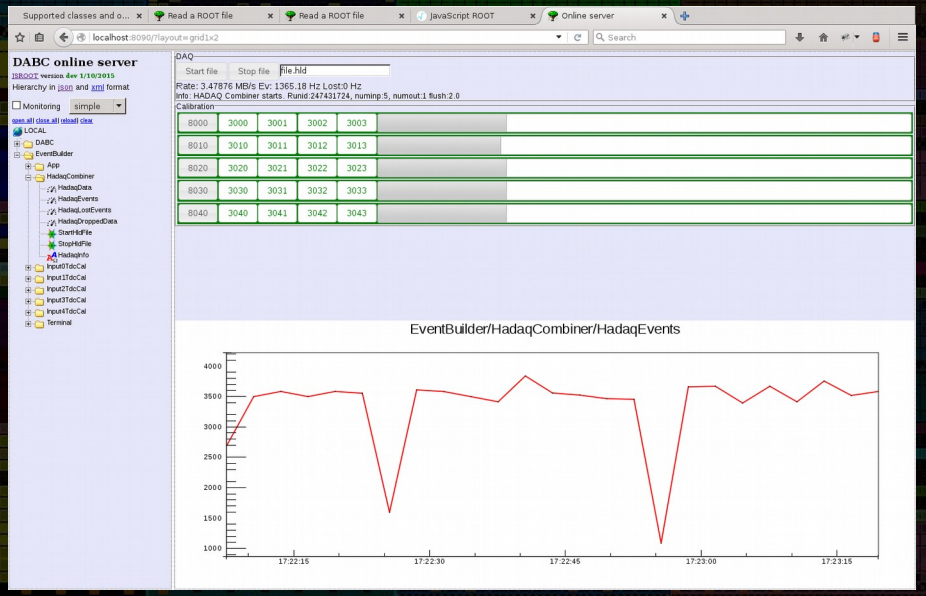
- CTS Details

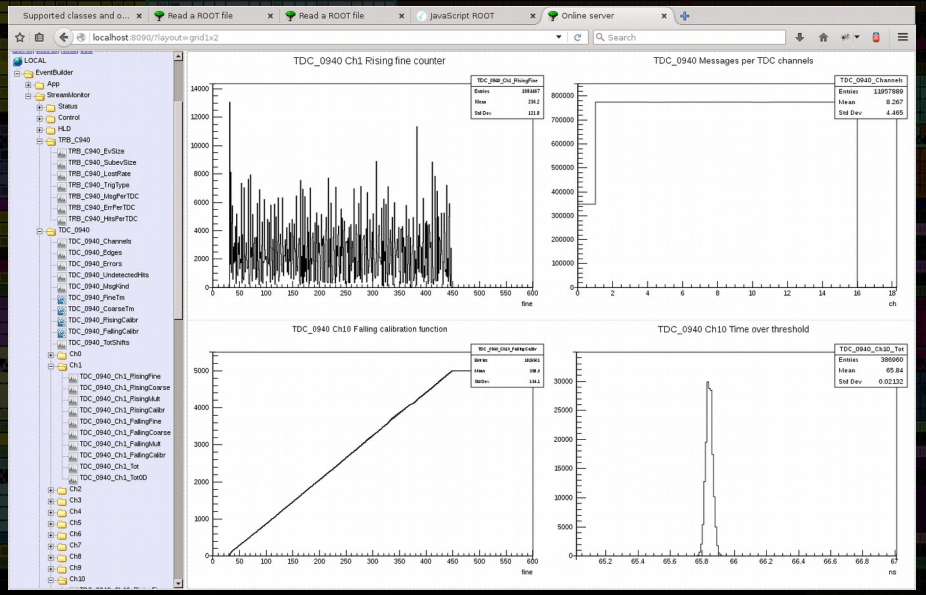
Readout config:
Trigger Channel Counter
Idle/Dead Counter
Trigger statistics
Timestamp
TD FSM Limit (debug only): disabled
RO FSM Limit (debug only): disabled

Design compiled	Thu, 15 Nov 2012 20:08:02
TD FSM State	TD_FSM_WAIT_TRIGGER_BECOME_IDLE
RO FSM State	RO_FSM_WAIT_BECOME_IDLE
RO Queue	Active, words enqueued: 43
Current Trigger (15:0)	0011 1110 0100 0000, Not asserted
Buffered Trigger (15:0)	0011 1110 0100 0110, Type: 0x1

- Extendible and modular structure
- Master and slave mode operation
- Free running operation
- Up to 16 independent trigger modules
- 4 channel TDC for trigger time
- 8 general purpose trigger inputs
- Coincidence detection
- Periodic & Random pulser
- On-board and off-board trigger distribution
- Trigger generation from TDC channel inputs
- Tested successfully during the CBM and PANDA test beams with slave and master modes

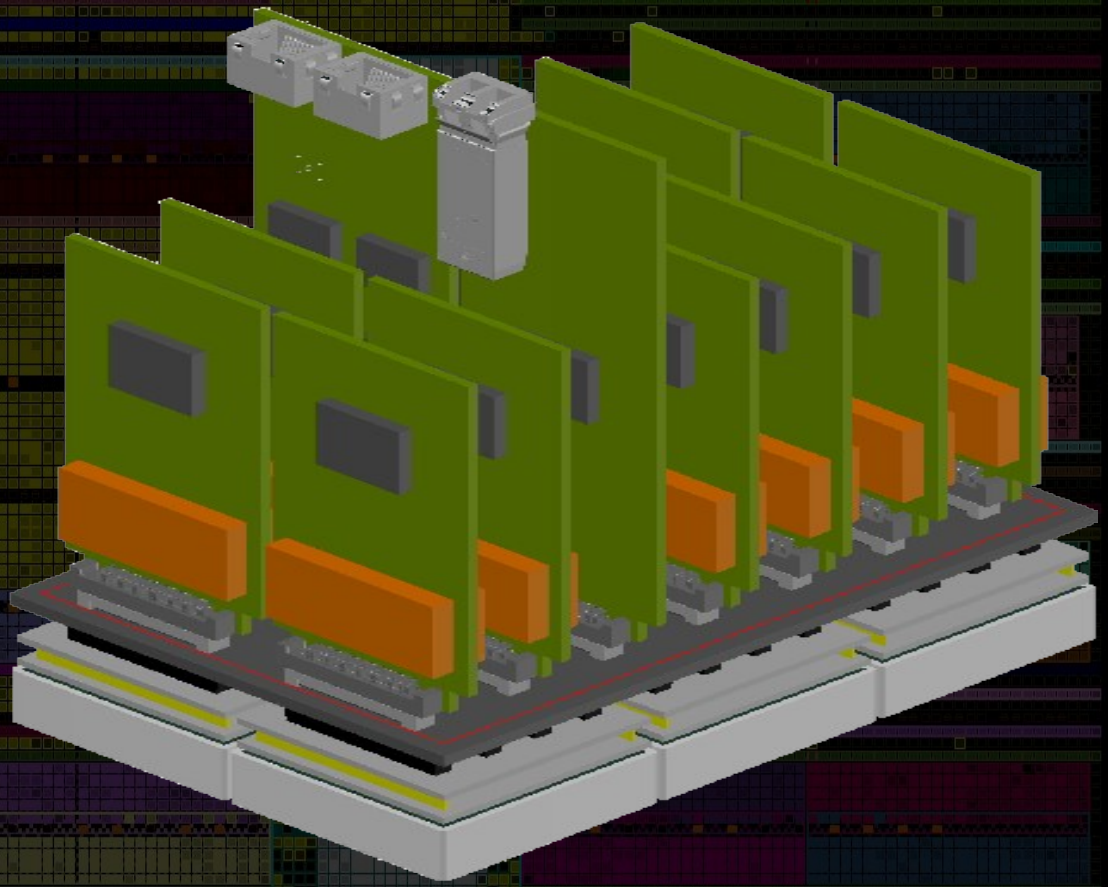
- Well tested and debugged full software package – eventbuilder, unpacker and analysis software
- DABC as eventbuilder
  - Eventbuilding rate: 500MB/s
  - Event sorting, on the spot calibration, online server for data analysis
  - Delivery of raw data and calibrated data as hld or root data
- Stream framework as analysis software
  - Written in C++
  - For histograms root is used
  - Can be integrated in DABC
  - Monitoring with a browser or Go4
  - Automatic offset correction for ToT measurements
  - Automatic temperature correction (being tested...)





NEW GENERATION : DIRICH

- New FEE concept for MA-PMT readout
- HADES + CBM RICH cooperation
- 32 channels, amplification, discrimination, TDC and DAQ
- No cables for analogue parts
- One backplane for 12 modules
- One backplane for signal, data, trigger, clock and power distribution
- Of course not risk free!



TRB3 COMMUNITY

Developers

Cahit Uğur	TDC
Jan Michel	TrbNet & DAQ
Grzegorz Korcyl	GbE
Manuel Penshuck	CTS
Michael Traxler	Organisation & Hardware
Ludwig Meier	Slow Control Software
Jörn Adamczewski-Musch	DAQ & Analysis
Sergey Linev	DAQ & Analysis
Matthias Hoek	Unpacking & Analysis

Active Users

Marek Pałka Jochen Frühauf
Adrian Rost Andreas Neiser

PANDA DIRC Groups in Mainz & GSI

Detector Groups

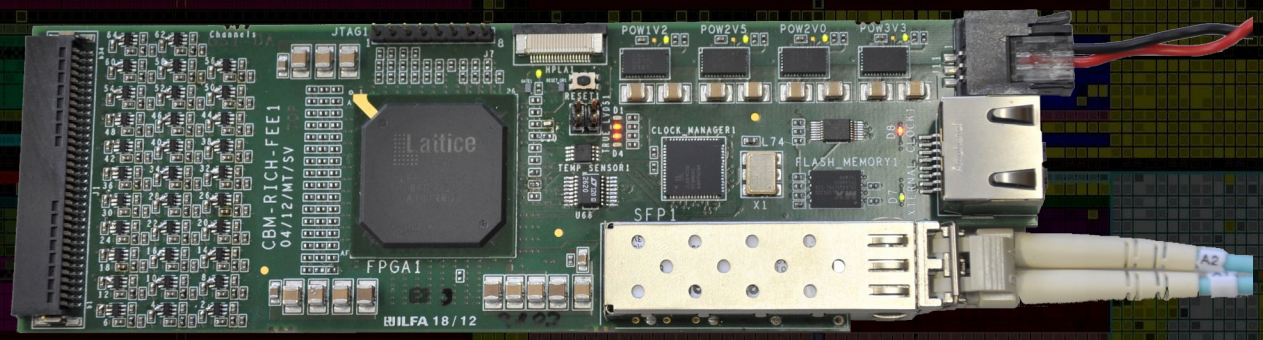
PANDA Barrel DIRC PANDA Disk DIRC
PANDA ToF CBM Forward Calorimeter
CBM – RICH CBM – ToF
HADES MDC FEE HADES Calorimeter
Mainz A2 Collaboration Mainz Neutron Detector

Coimbra PET Scanner
and many more to come...

TIME TO COME BACK

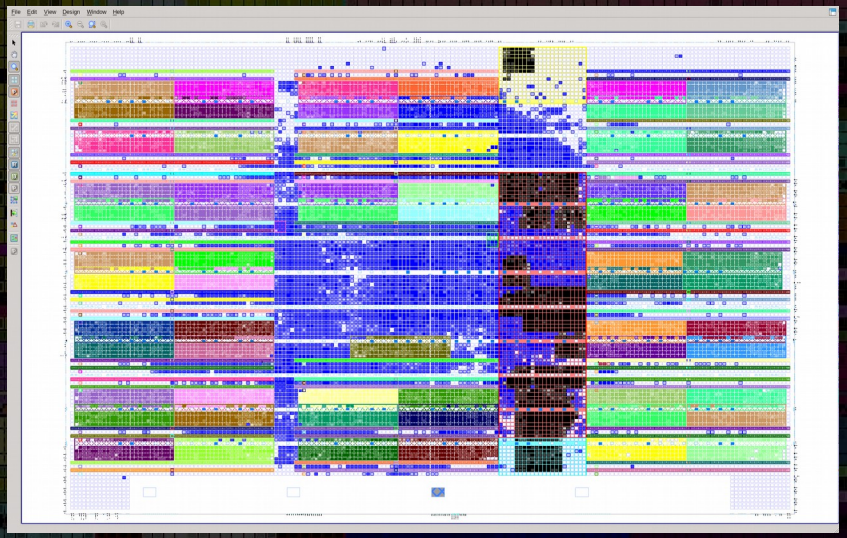

BACKUP
SLIDES

FEE & 65 Channel TDC

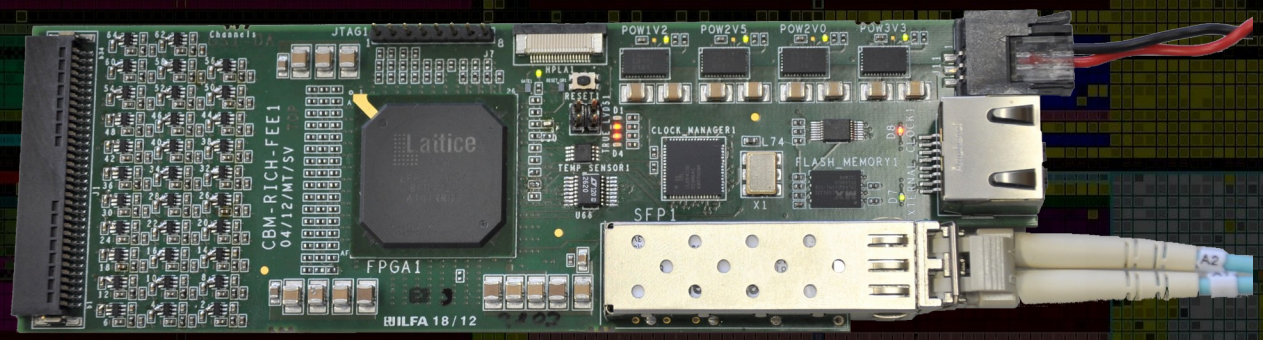


- 64 signals from detector
- Amplification
- Thresholds
- Input signal discrimination
- Time measurement
- Data readout

- Trigger signal is digitised for reference time (65th channel)
- Data readout through 2GBit/s optical link
- 5x16 cm to be plugged on the back of an MCP-PMT
- Very high density for FEE & 65 channel TDC + DAQ + Power
- Tested during the CBM October 2012 test beam
- The Sync message is processed at the internal TRB3-CTS and distributed to 4 FEEs
- Half detector readout with CBMRICH-FEE, other half with nXYTER



FEE & 65 Channel TDC



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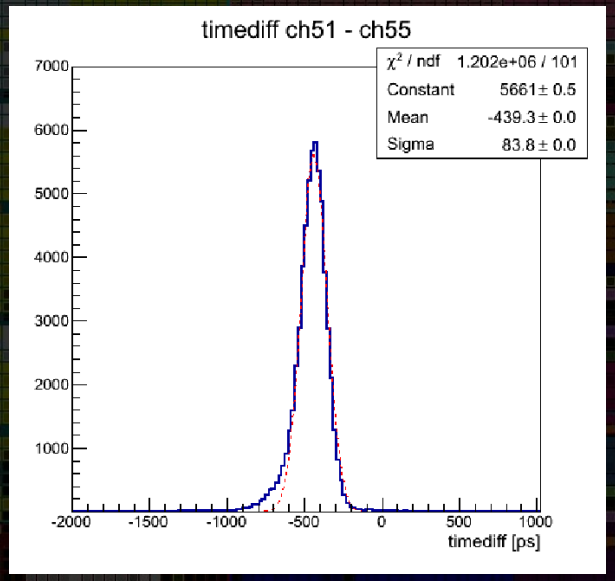
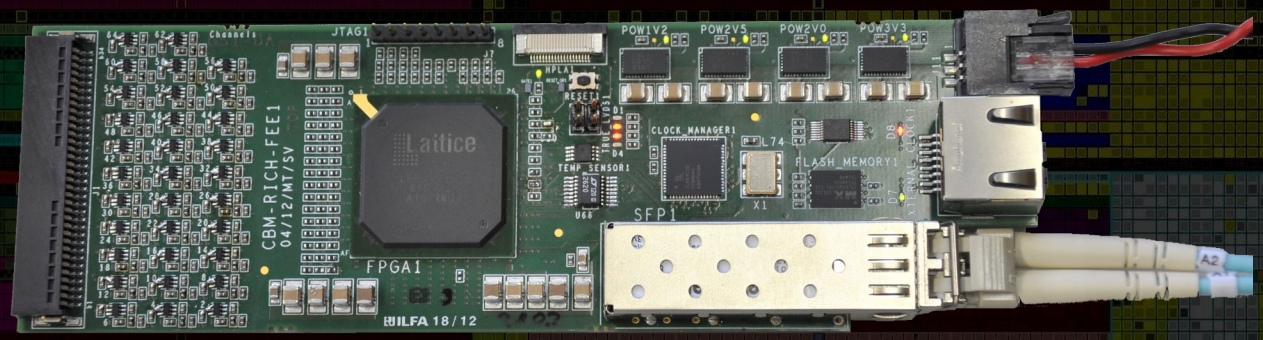


FEE & 65 Channel TDC



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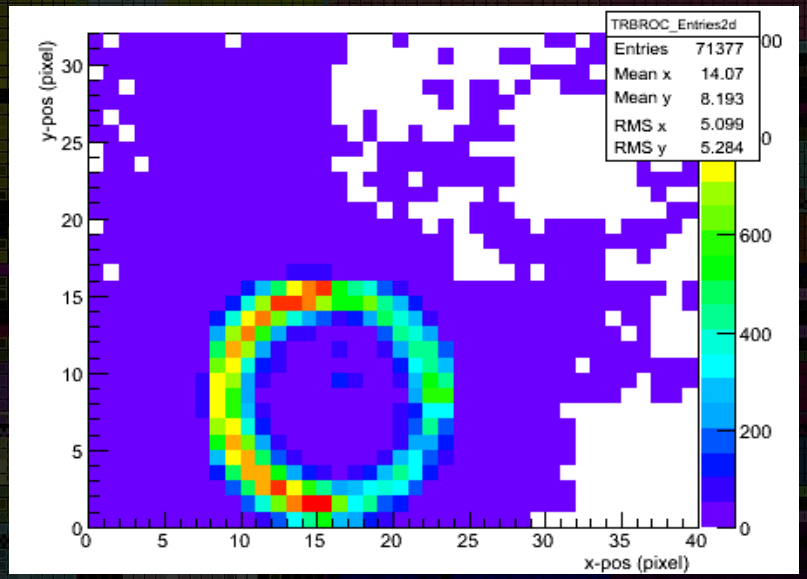
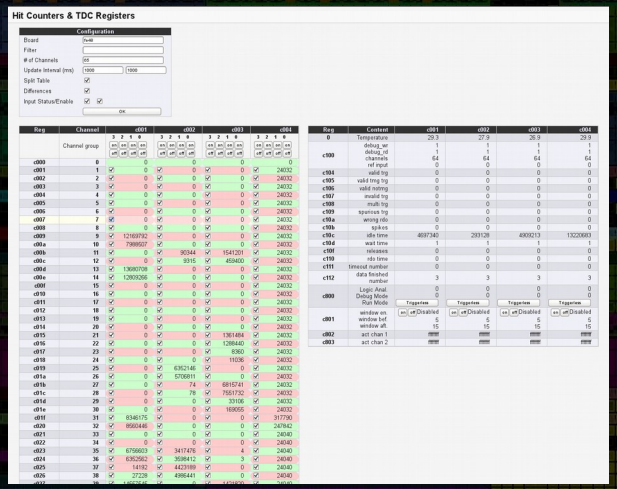
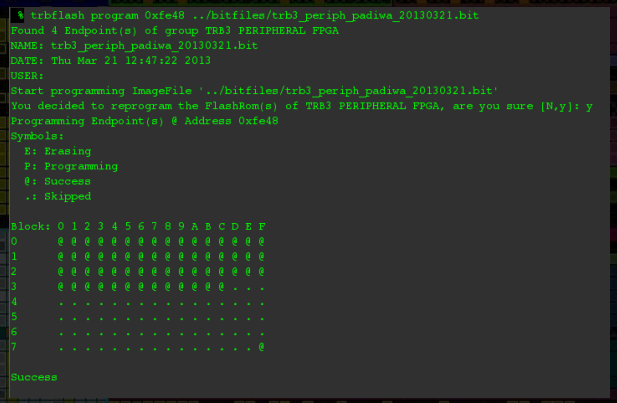


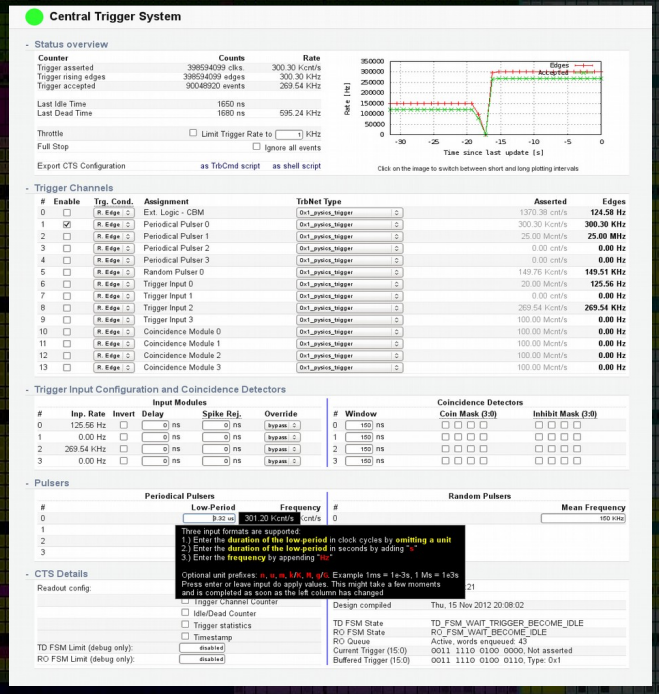
TRB3 Platform: Software



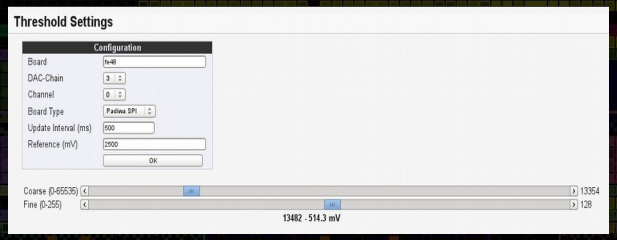
TDC
readout & channel
monitoring & control



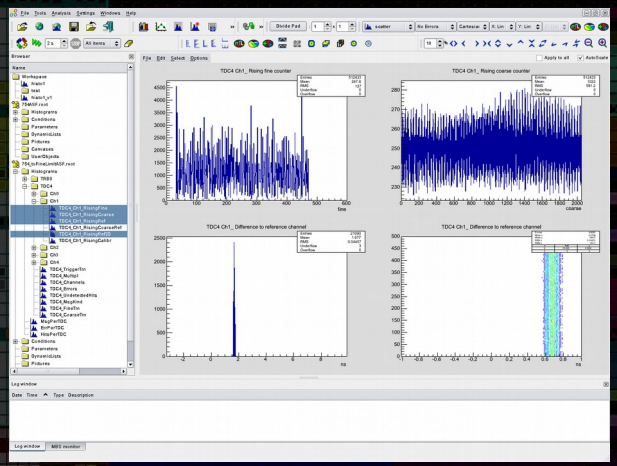
Console based
slow control software
with many features



Trigger
processing & control



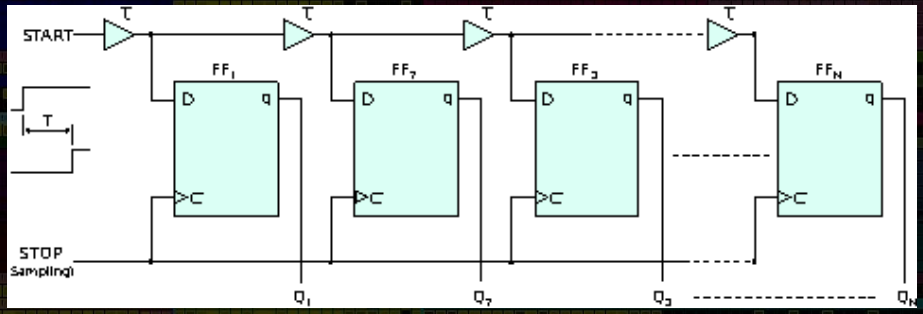
Threshold setting



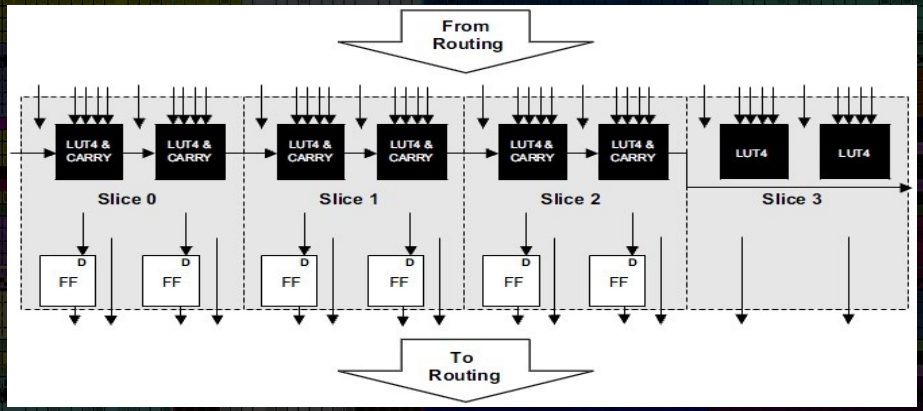
Unpacking & Online Analysis

Tapped Delay Line Method

- Tapped delay line is used for fine time measurements – suits well with the FPGA architecture
- Delay elements are realised by LUTs
- Fast carry chain structure forms the delay line
- Registers are used to sample the delay line

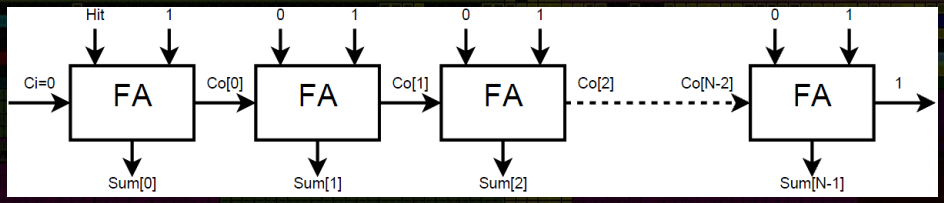


Tapped Delay Line Method

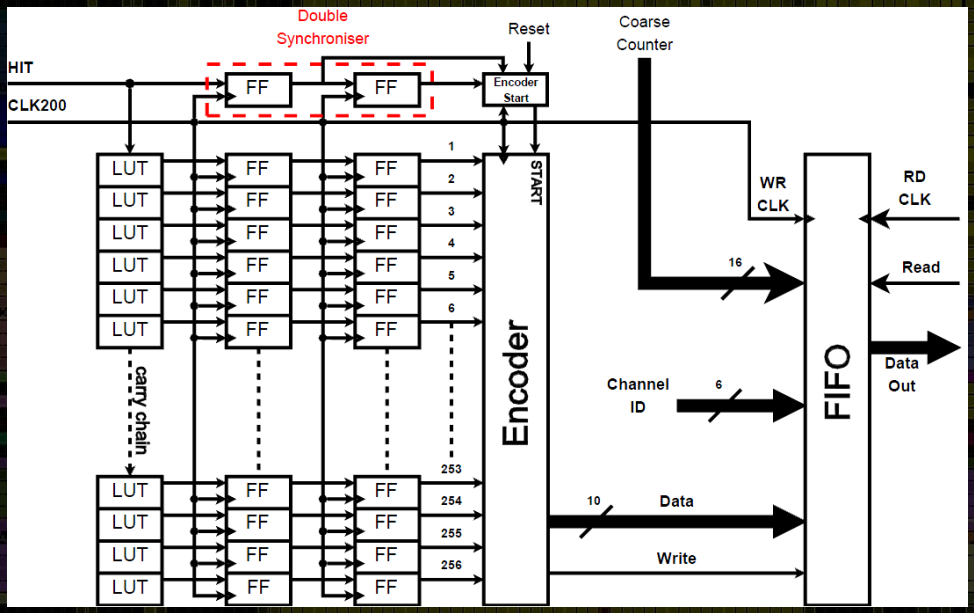


PFU Diagram

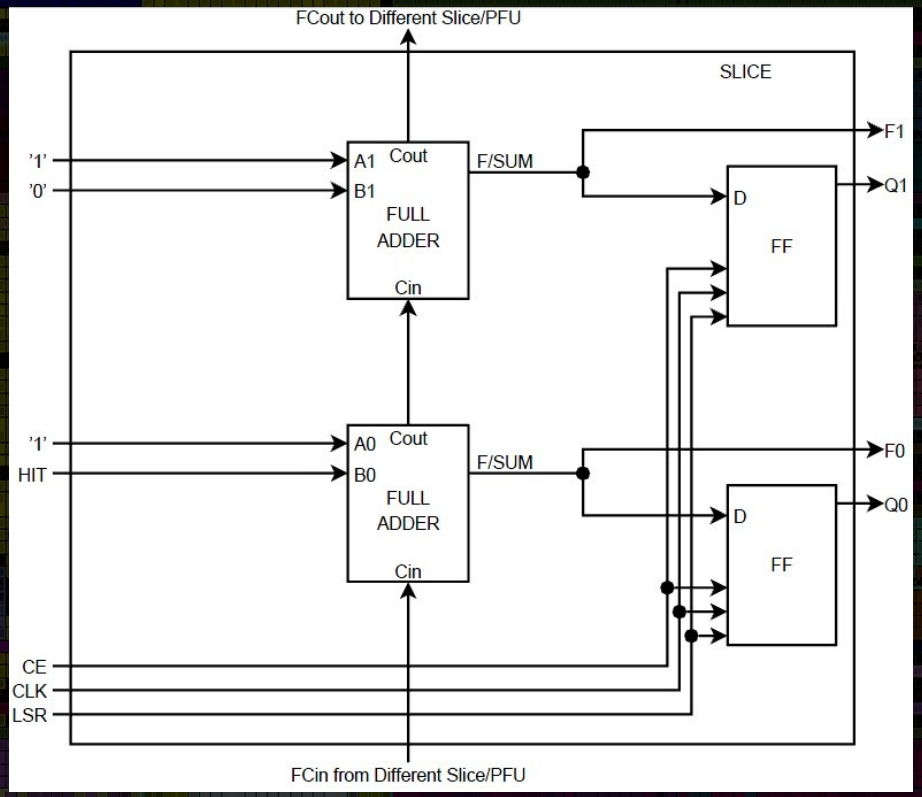
Architecture of the TDC



Delay line is realised with Full Adders [3]



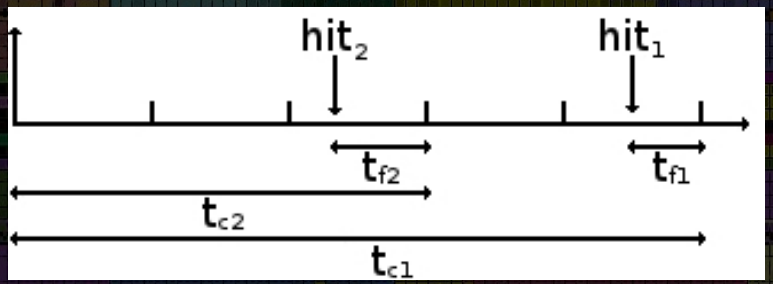
TDC Architecture



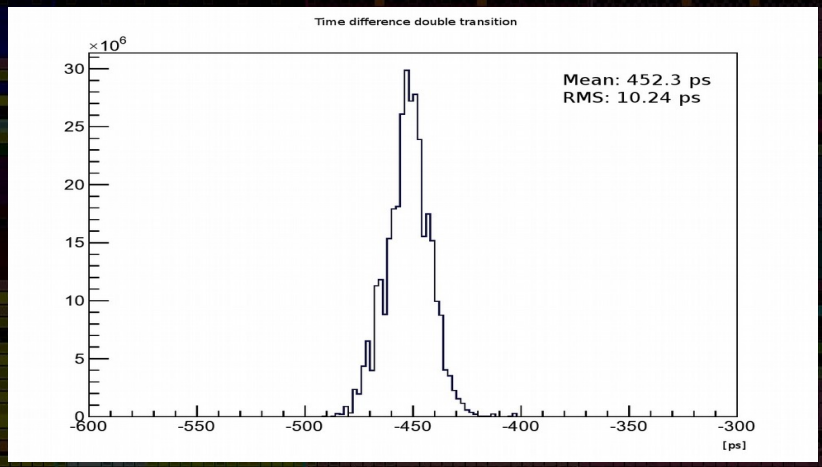
Slice diagram with LUTs programmed as Full Adders

Laboratory Test Results

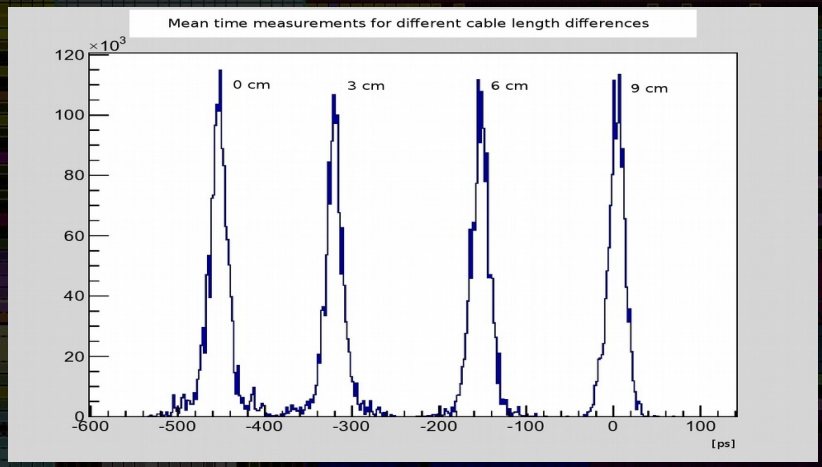
- Time difference measured between 2 channels
- $\Delta t = (t_{coarse1} - t_{coarse2}) - (t_{fine1} - t_{fine2})$
- RMS measured: 10.34 ps against the same clock
- Precision: 10.34 ps / √2 = 7.3 ps RMS



Time difference between two measurements

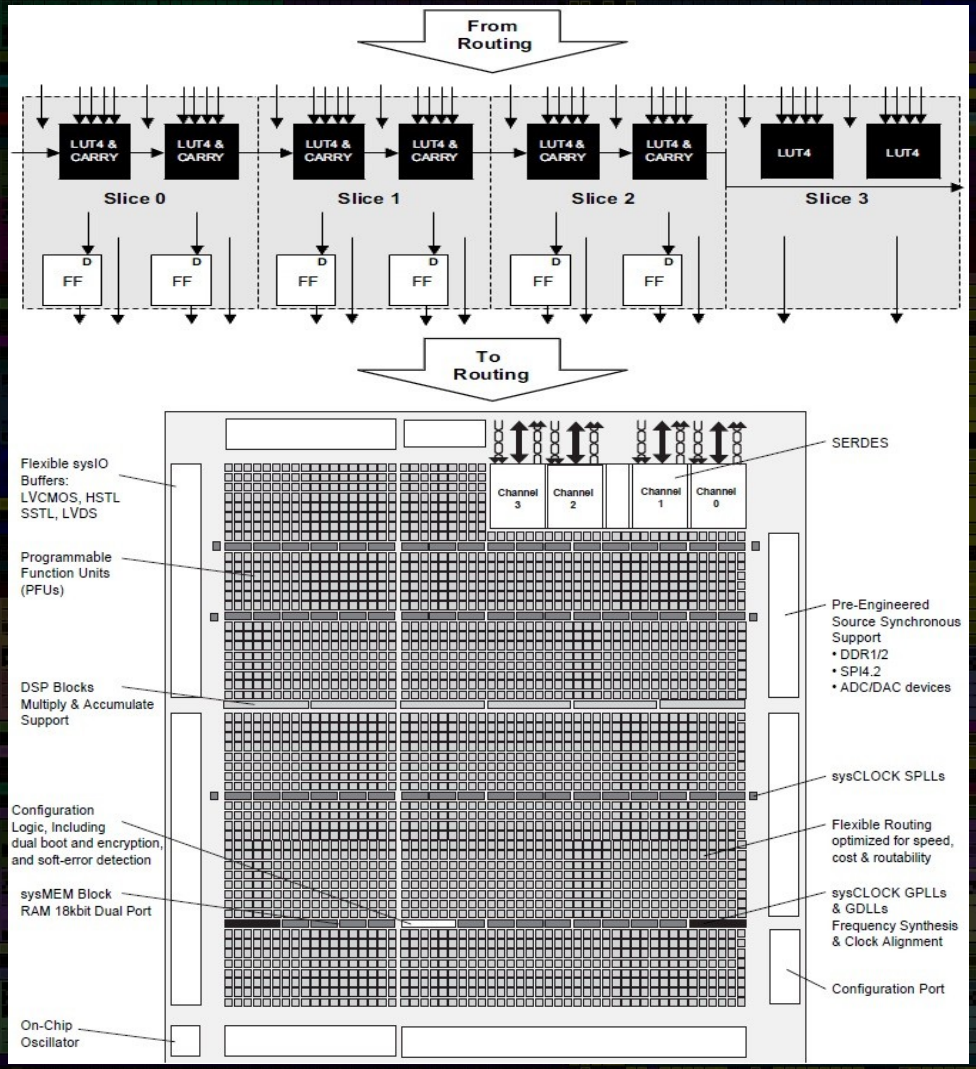


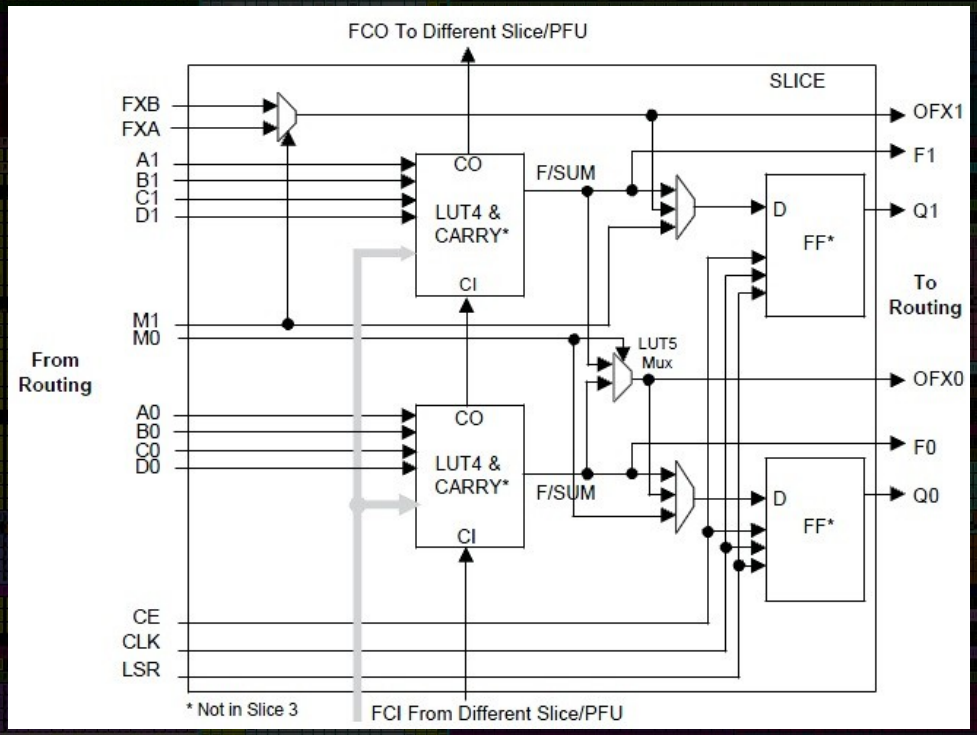
Time precision test



Mean measurement test

Architecture of TDC

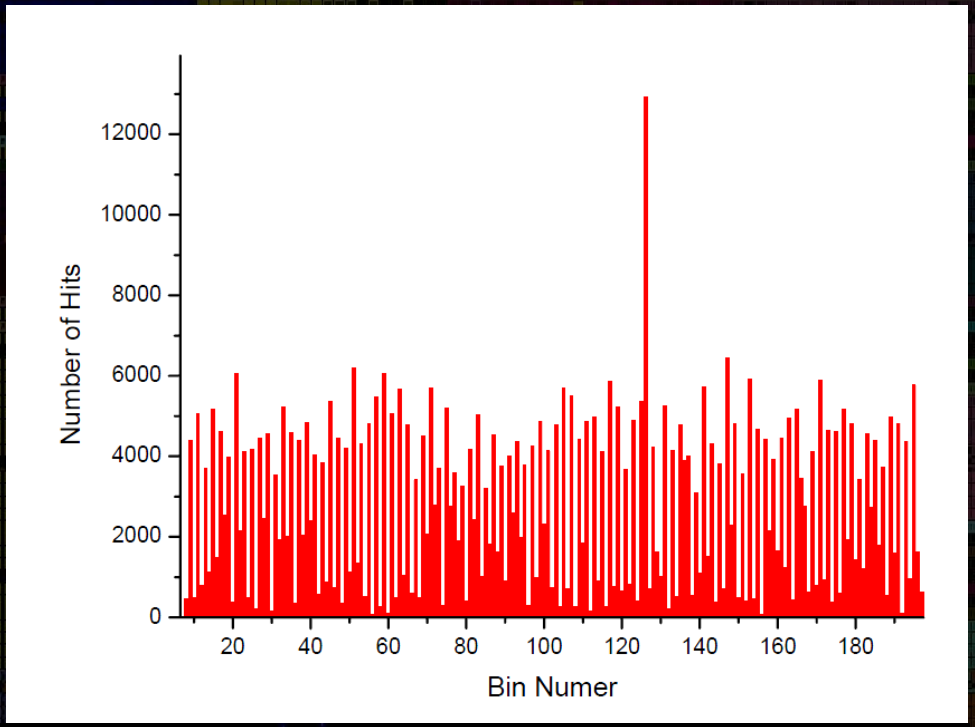




Lattice ECP2M FPGA Slice Diagram, PFU Diagram and Floor-plan

Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
- Effect of longer inter-slice routings
- Effect of PFU architecture



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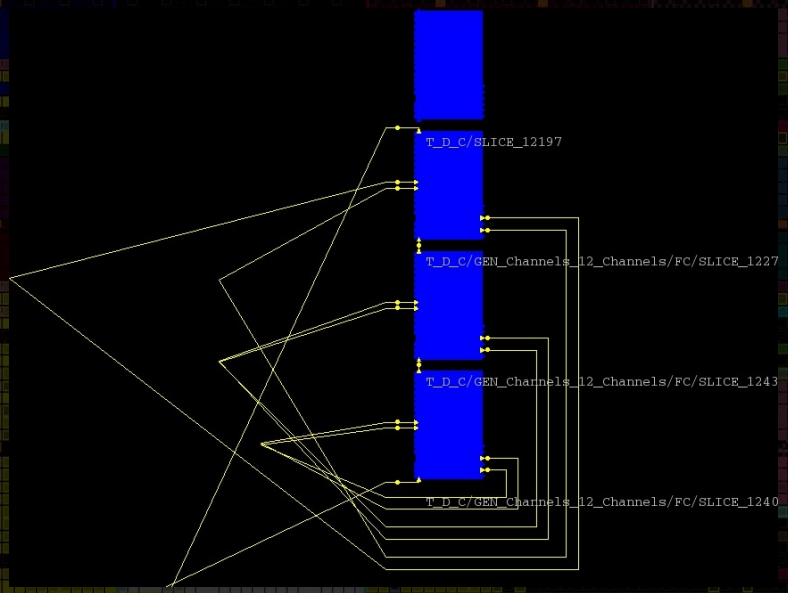
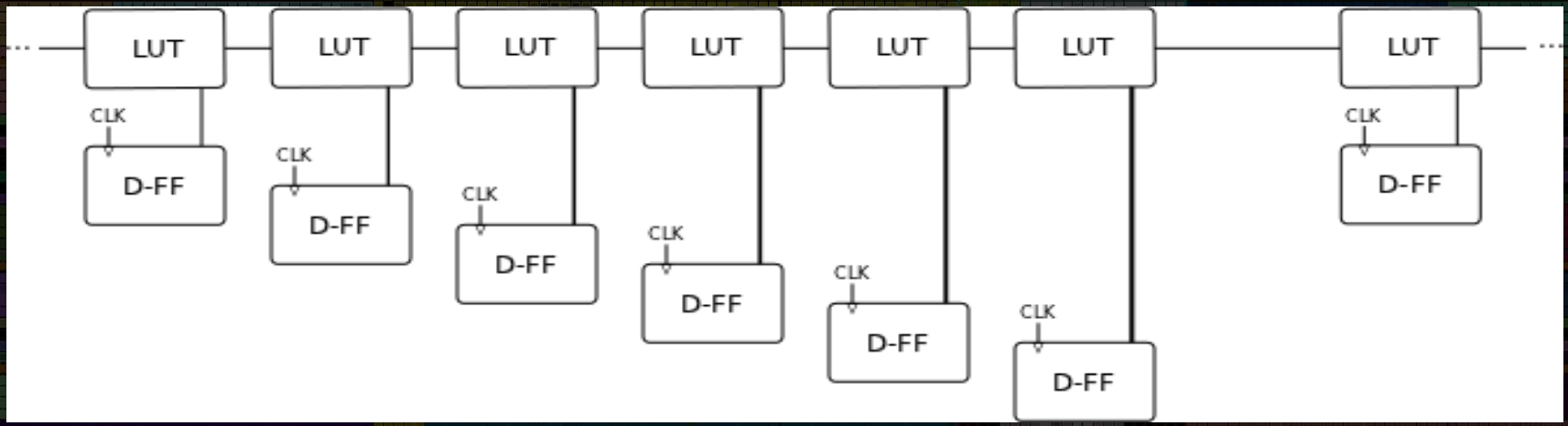
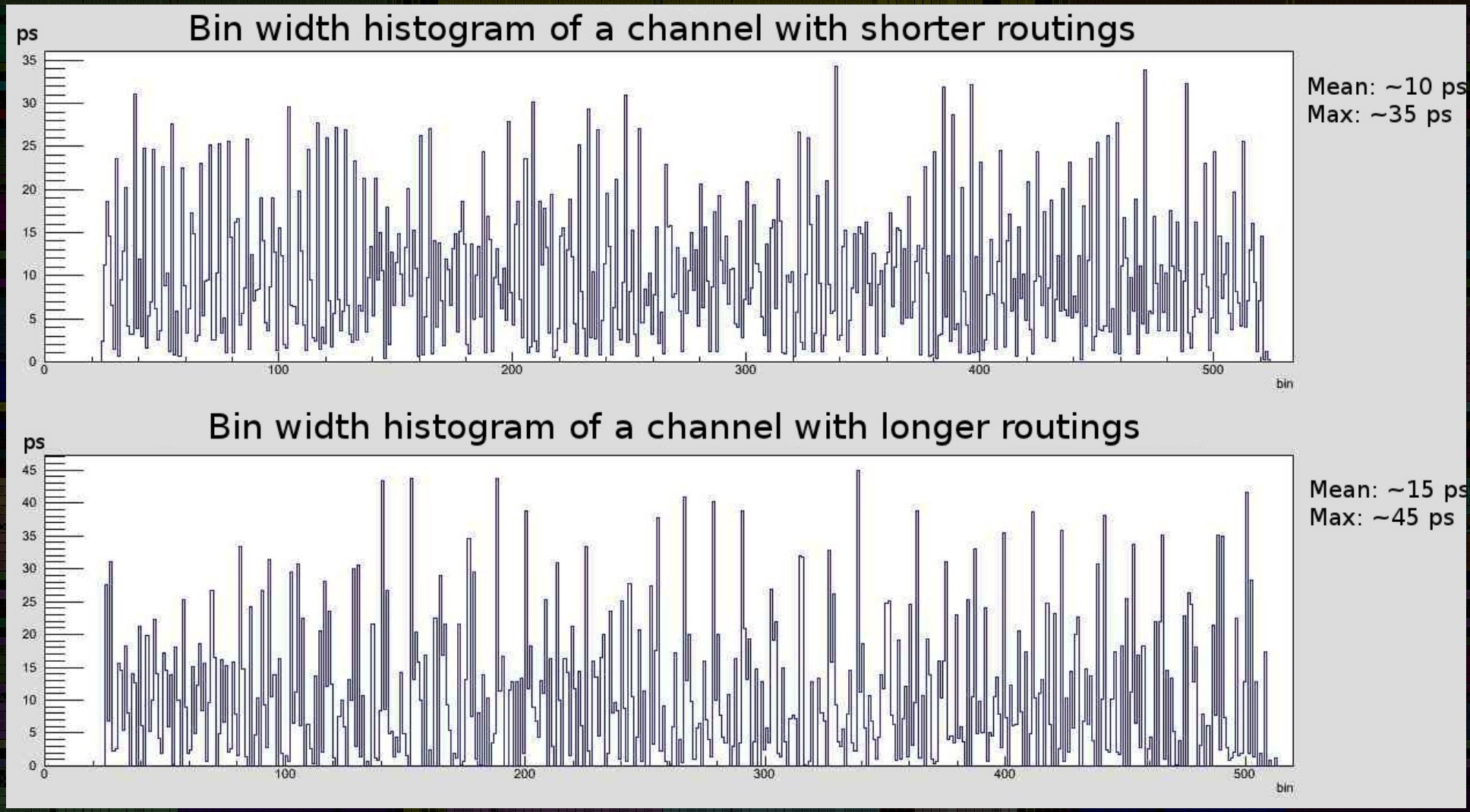




Architectural Effects of FPGA



Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
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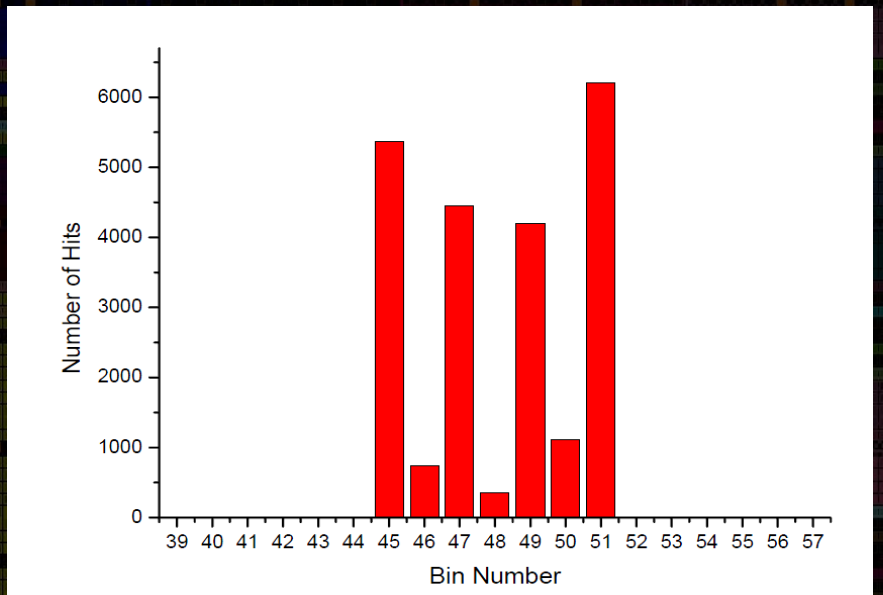
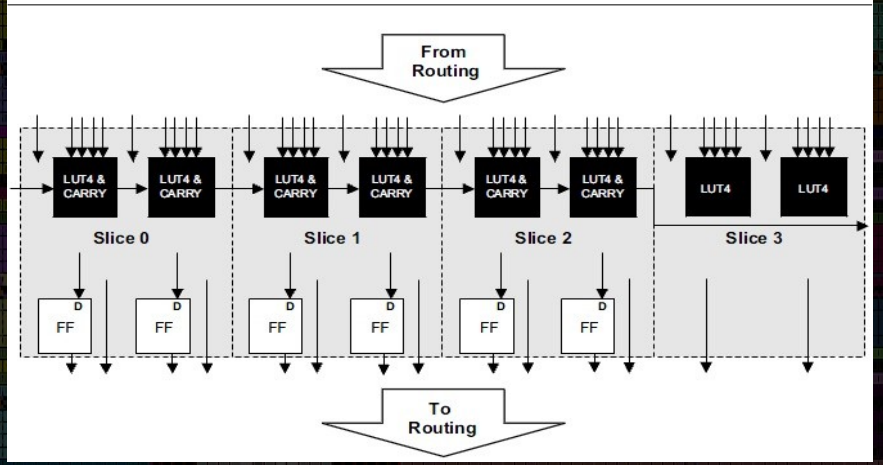
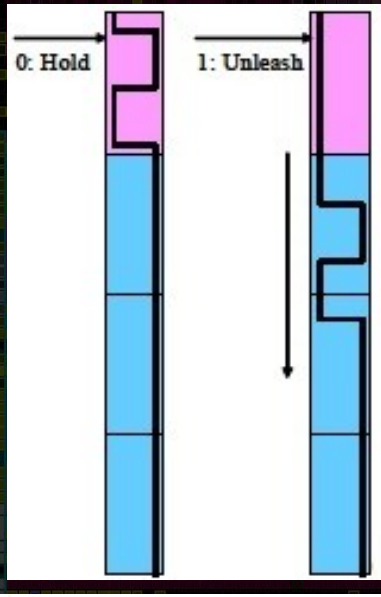
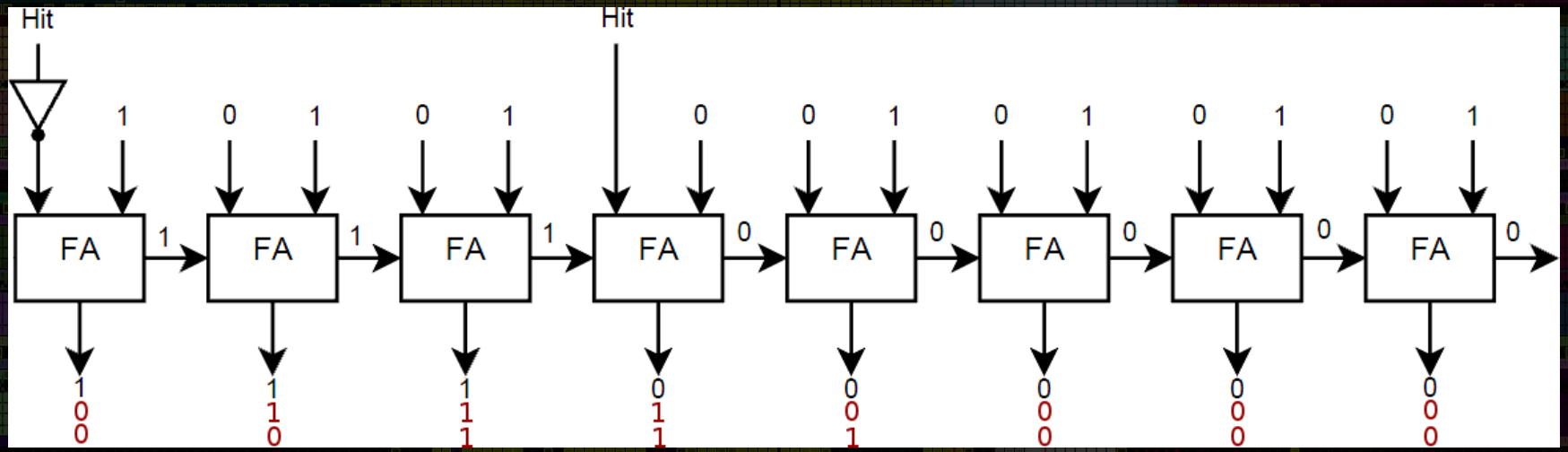




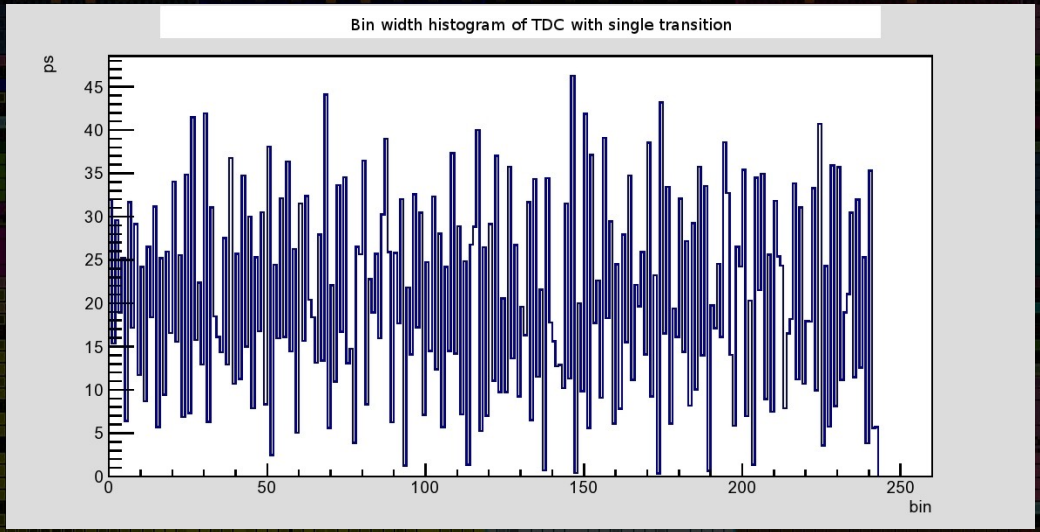
Wave Union Launcher

- More than one delay line is necessary in order to reduce the effect of wide bins
- Wave union launcher is implemented
- Bin widths & non-linearities are reduced



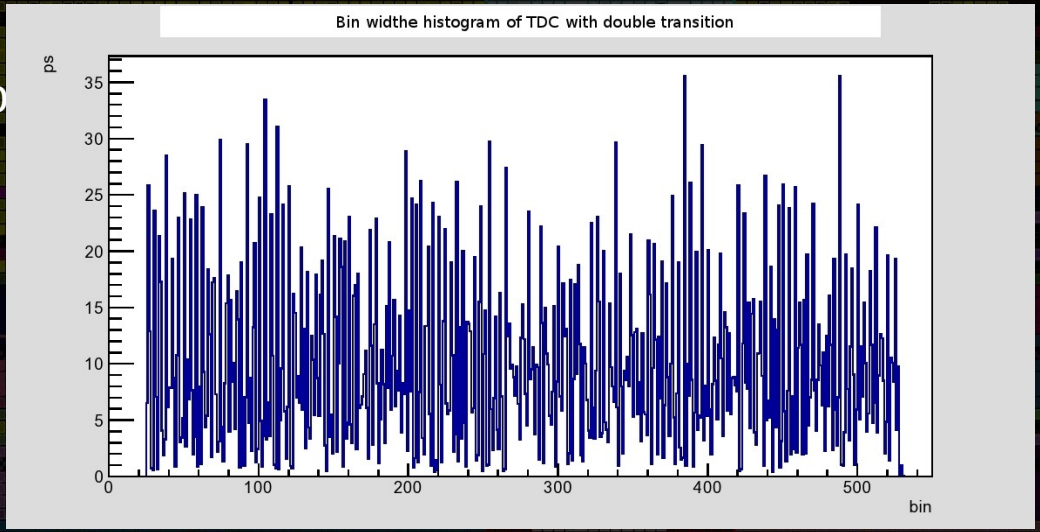


Wave Union Launcher



Bins: ~240
Mean: ~20 ps
Max: ~45 ps

- More virtual bins
- Narrower bins
- Homogeneous bin distributio



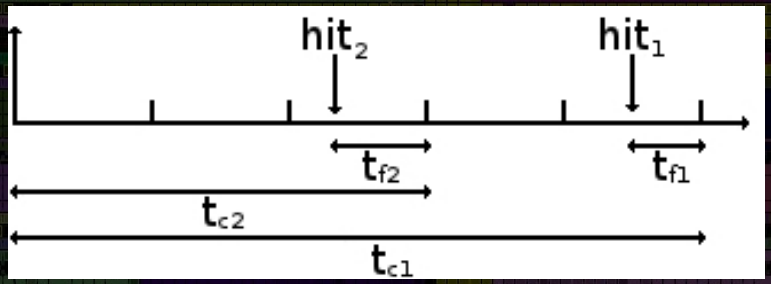
Bins: ~520
Mean: ~10 ps
Max: ~35 ps

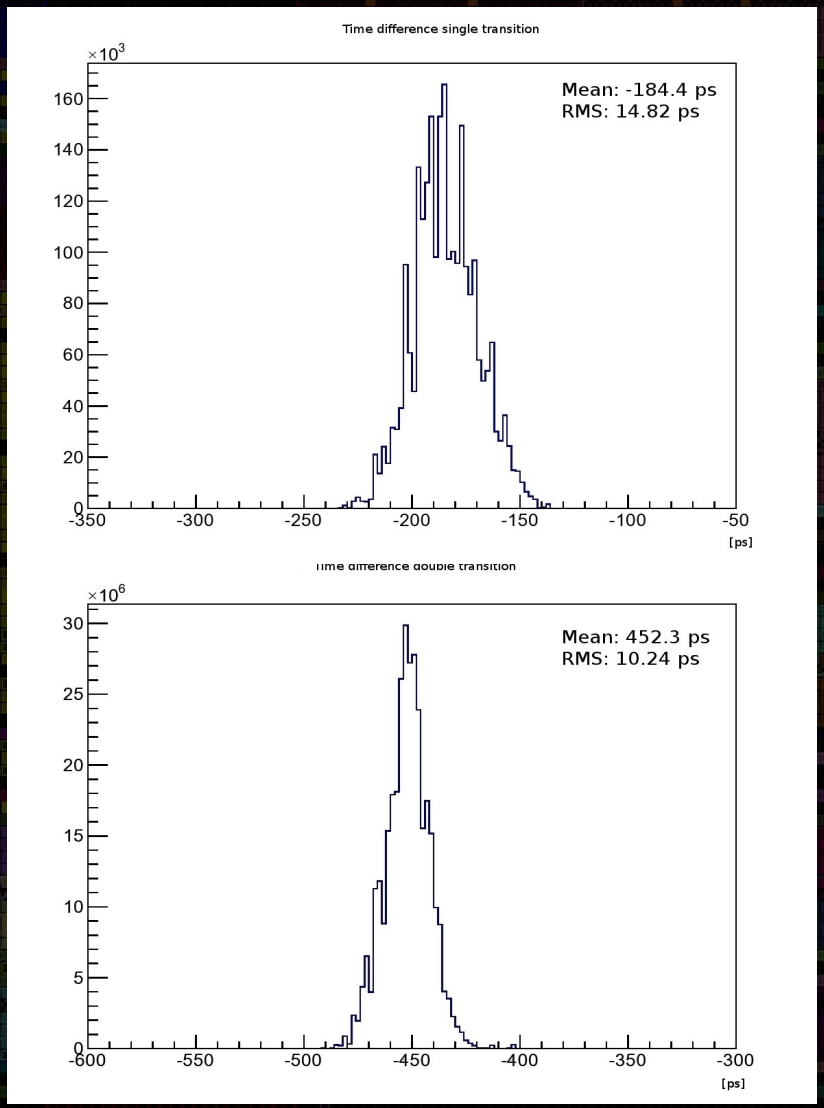
Statistical Error & Precision

- Time difference measured between 2 channels
- $\Delta t = (t_{coarse1} - t_{coarse2}) - (t_{fine1} - t_{fine2})$
- RMS measured: 10.34 ps

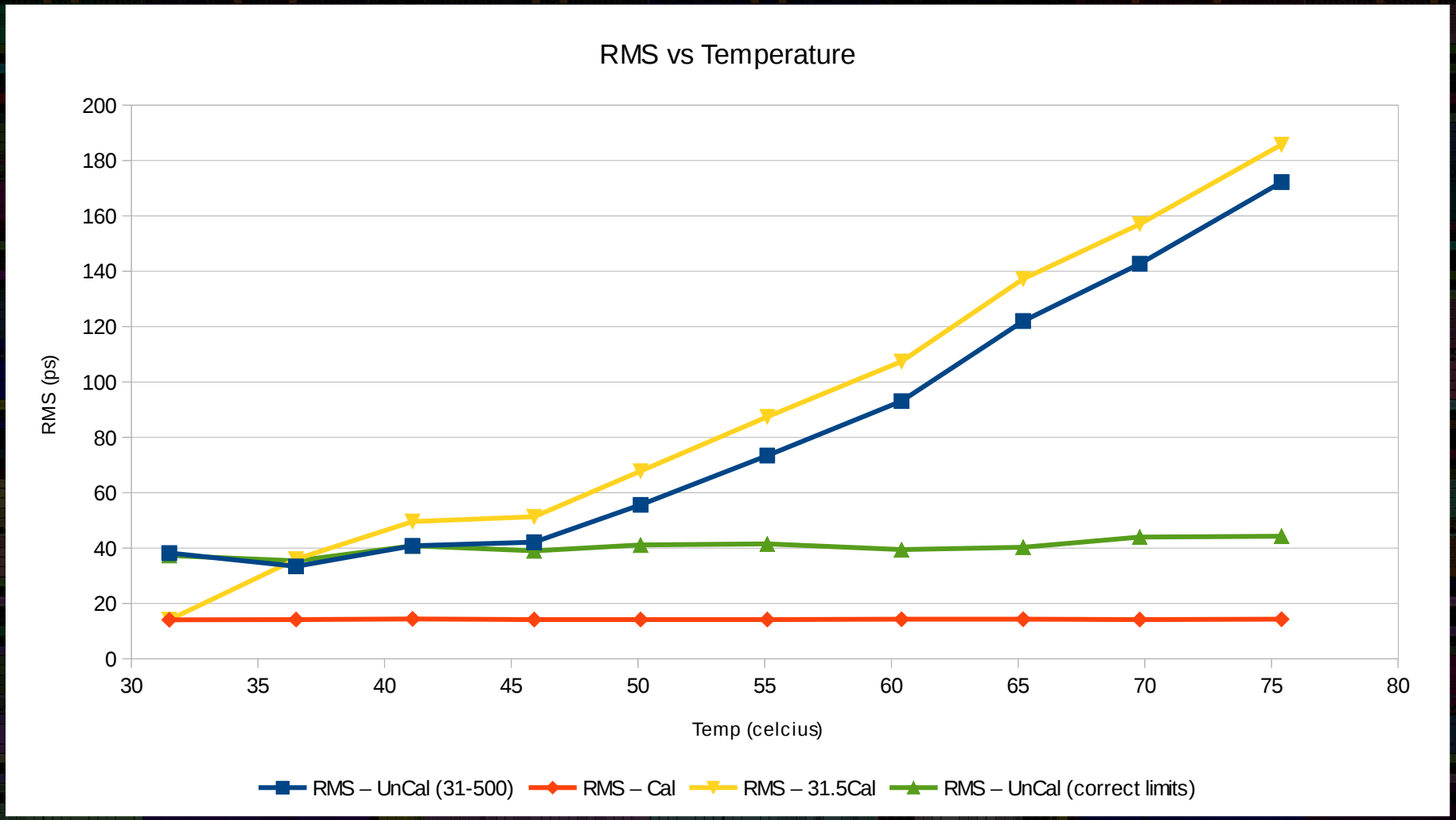
  against same clock
- Precision: 10.34 ps / √2 = 7.3 ps
- Effect of 2 transitions:

  14.82 ps / 10.34 ps = 1.43 factor

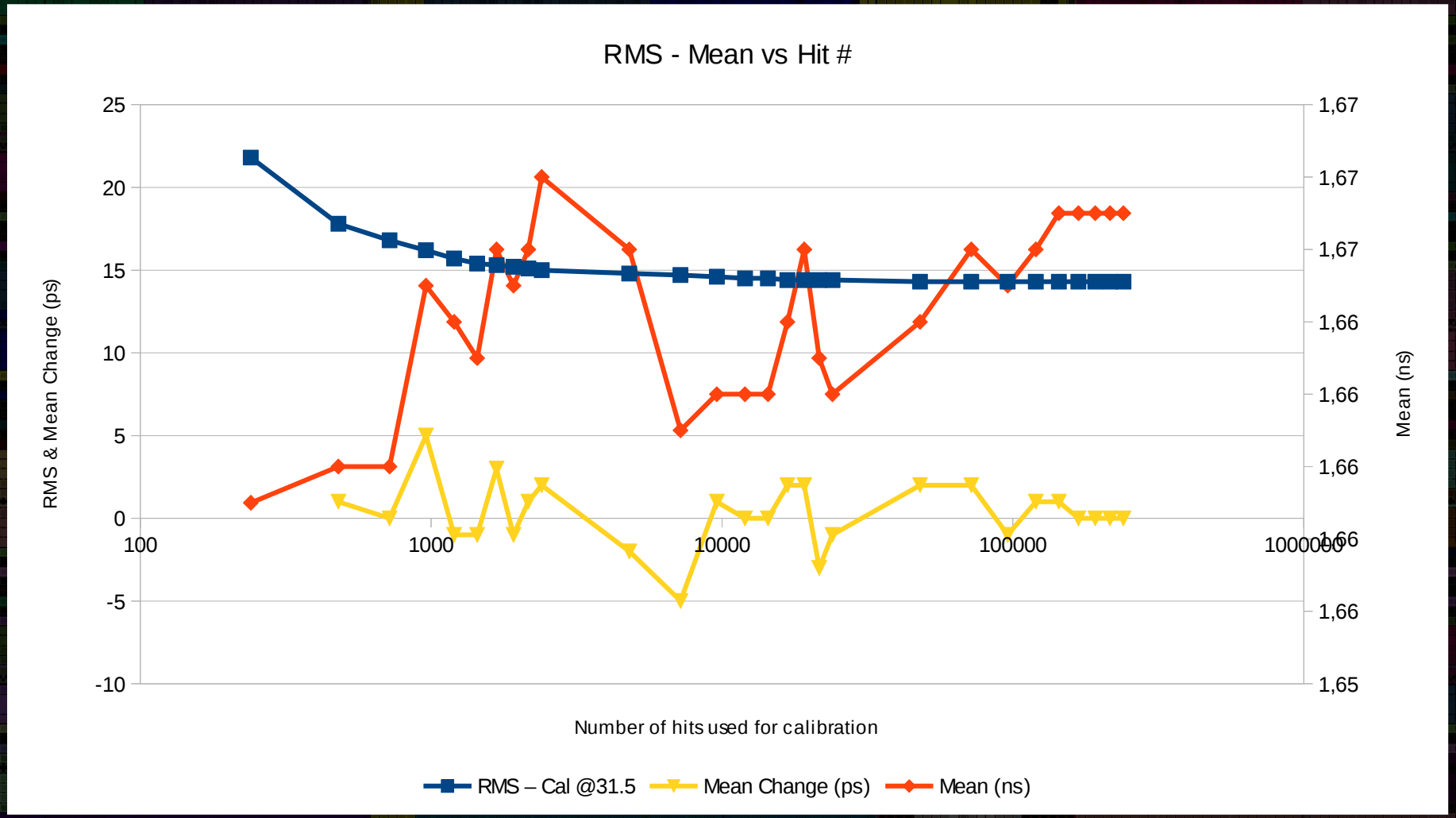




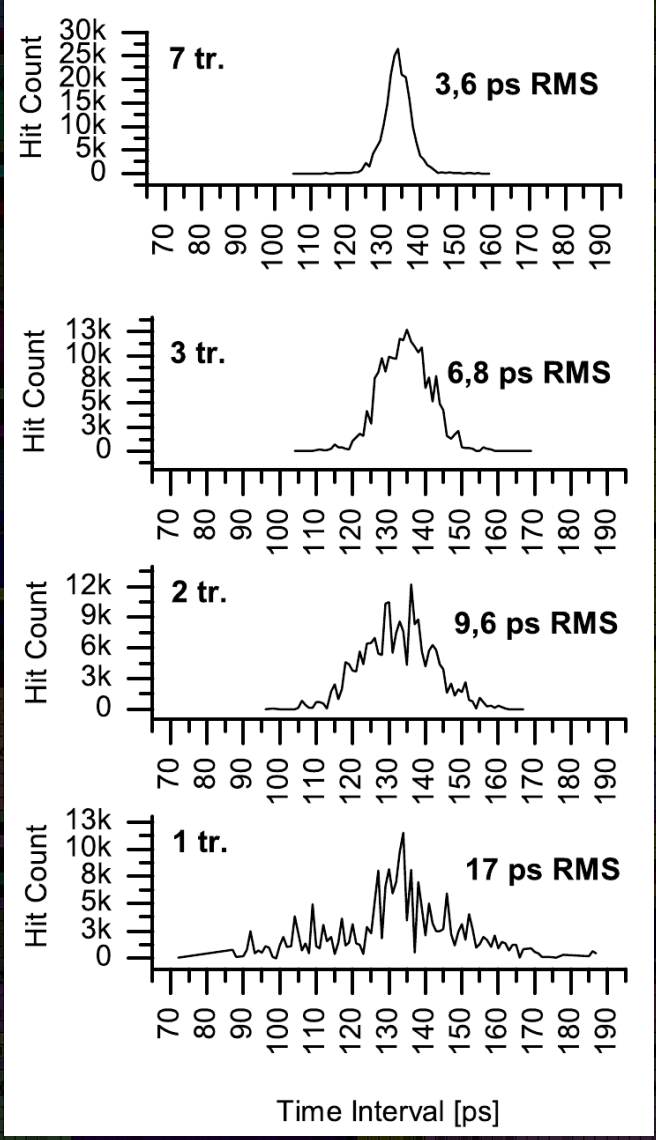
Precision vs Temperature



Precision & Mean vs Statistics



Precise TDCs in FPGAs



Published IEEE 2011, E.Bayer et al.

- TDC time precision down to 3.6 ps [RMS] (between two channels) using the wave union method [Jinyuan Wu] are possible
  - No cut on tails!
- Trade-off for number of channels, time precision and dead time can be adjusted to the needs of the application
  - 65 channels in an FPGA
  - <20 ps RMS time precision on each channel [RMS]