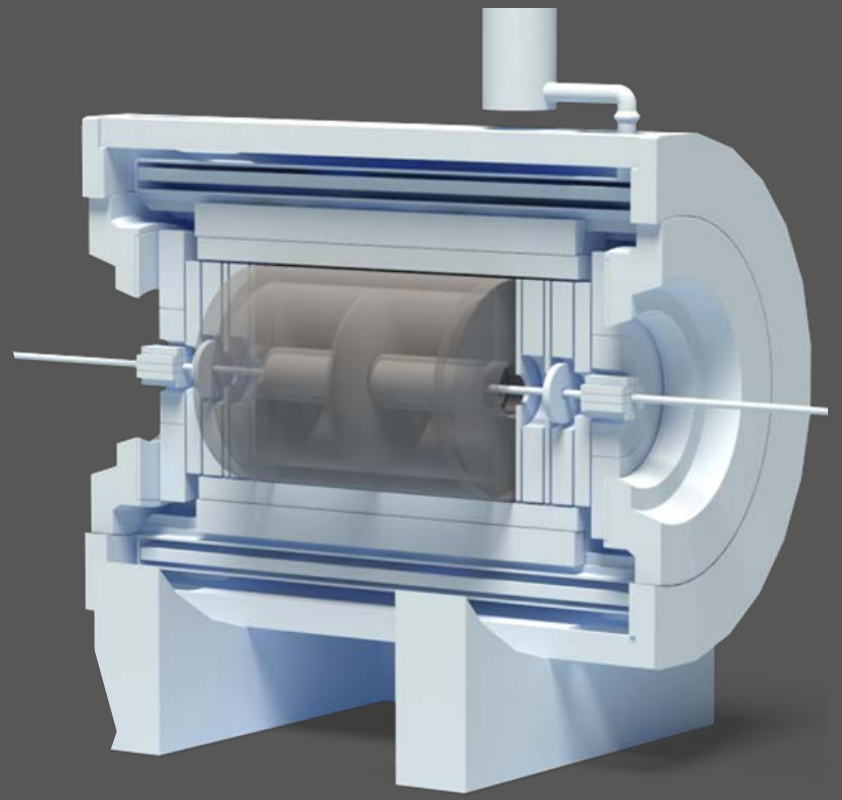
Front-End Electronics development for TPC/MPD detector of NICA project

Stepan Vereschagin, on behalf of the TPC/MPD group, LHEP, JINR



NICA

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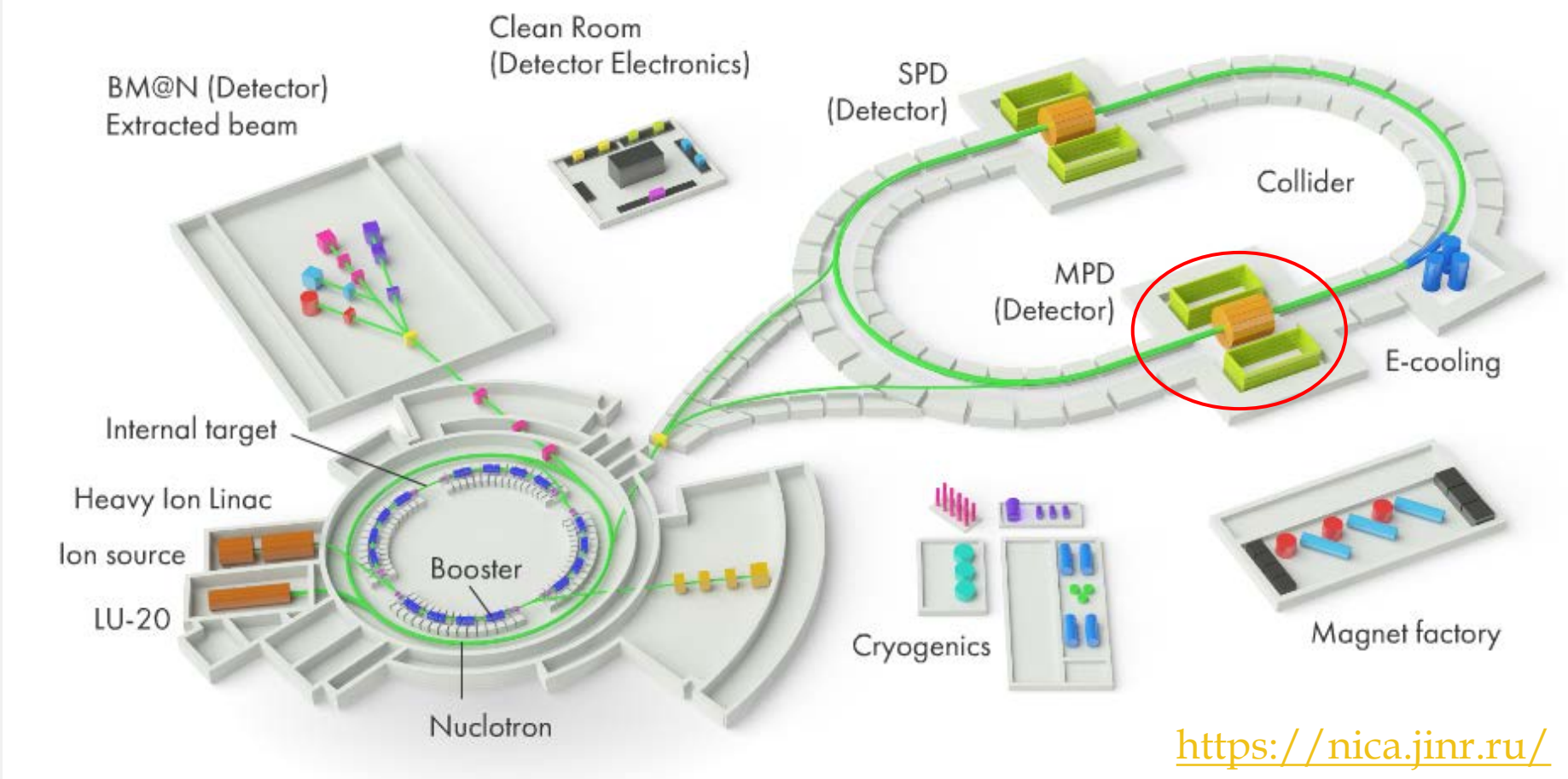
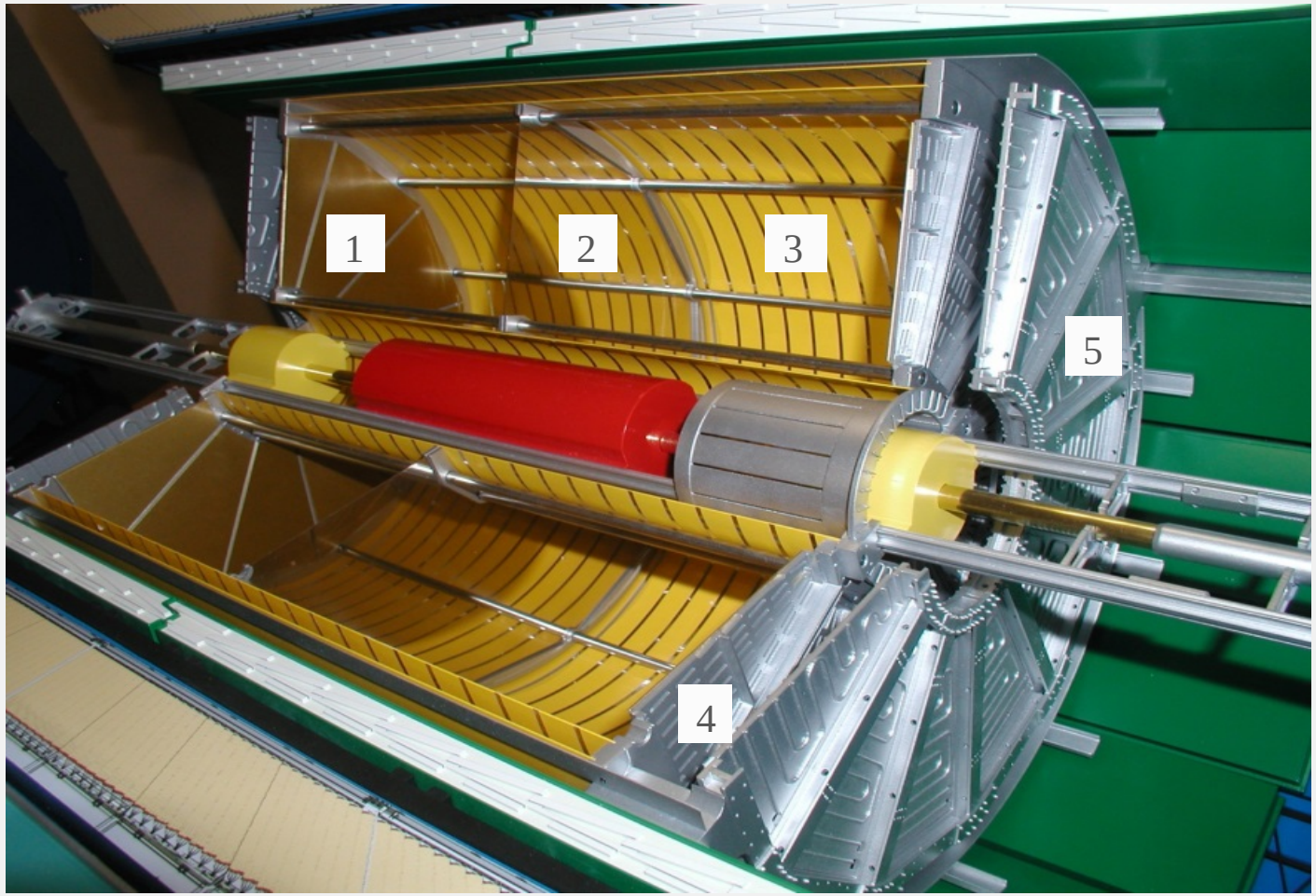
NICA Complex



Central part of the MPD mock up with TPC cut



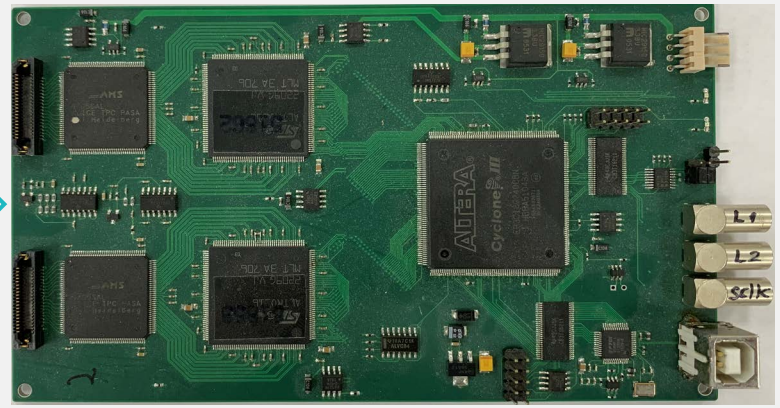
The TPC/MPD design requirements:

- The overall acceptance: $\eta < 1.2$
- The momentum resolution for charged particles is under 3% in the transverse momentum range $0.1 < pt < 1$ GeV/c
- Two-track resolution is of about 1 cm
- Hadron and lepton identification by dE/dx measurements - with a resolution better than 8%
- Data flow rate up to 100 GBps at trigger rate 7 KHz

1- MWPC;
2 - HV electrode;
3 - Field cage;
4 - FEE position;
5 - End cap thermal screen.

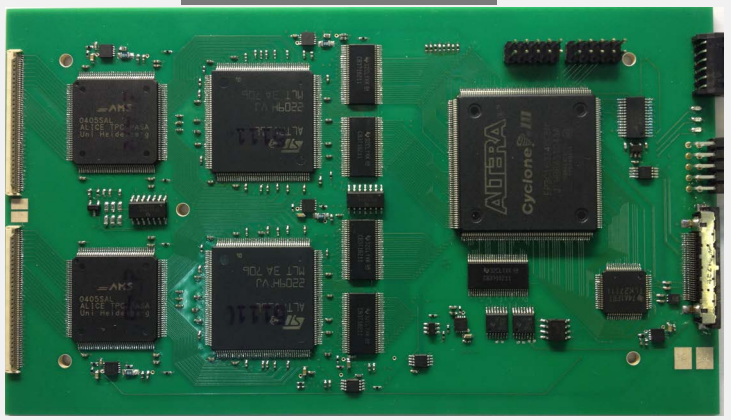
TPC/MPD FEC evolution

ALTRO FEC prototype



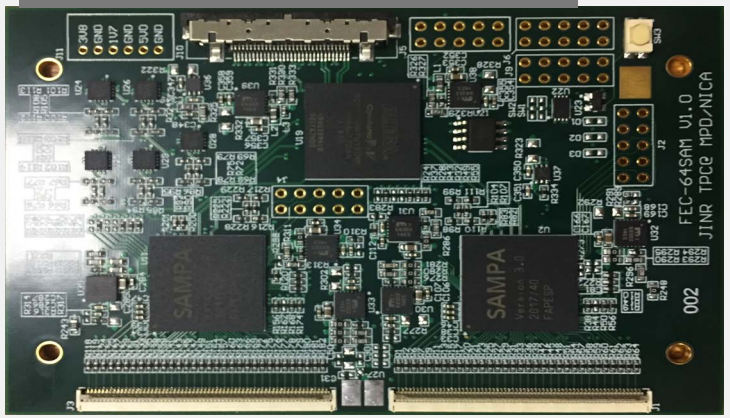
100x170 mm^2

ALTRO FEC



95x167 mm^2

SAMPA FEC prototype

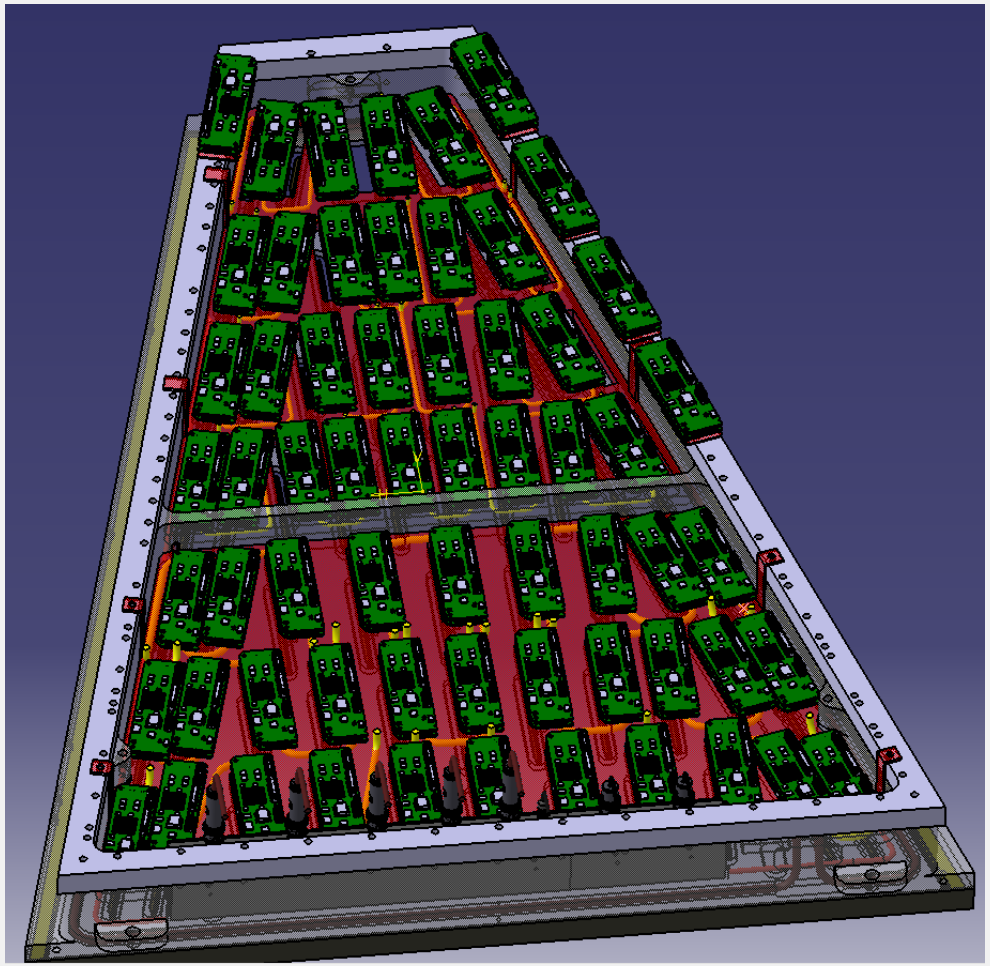


One PCB form factor 65x95 mm^2

SAMPA FEC

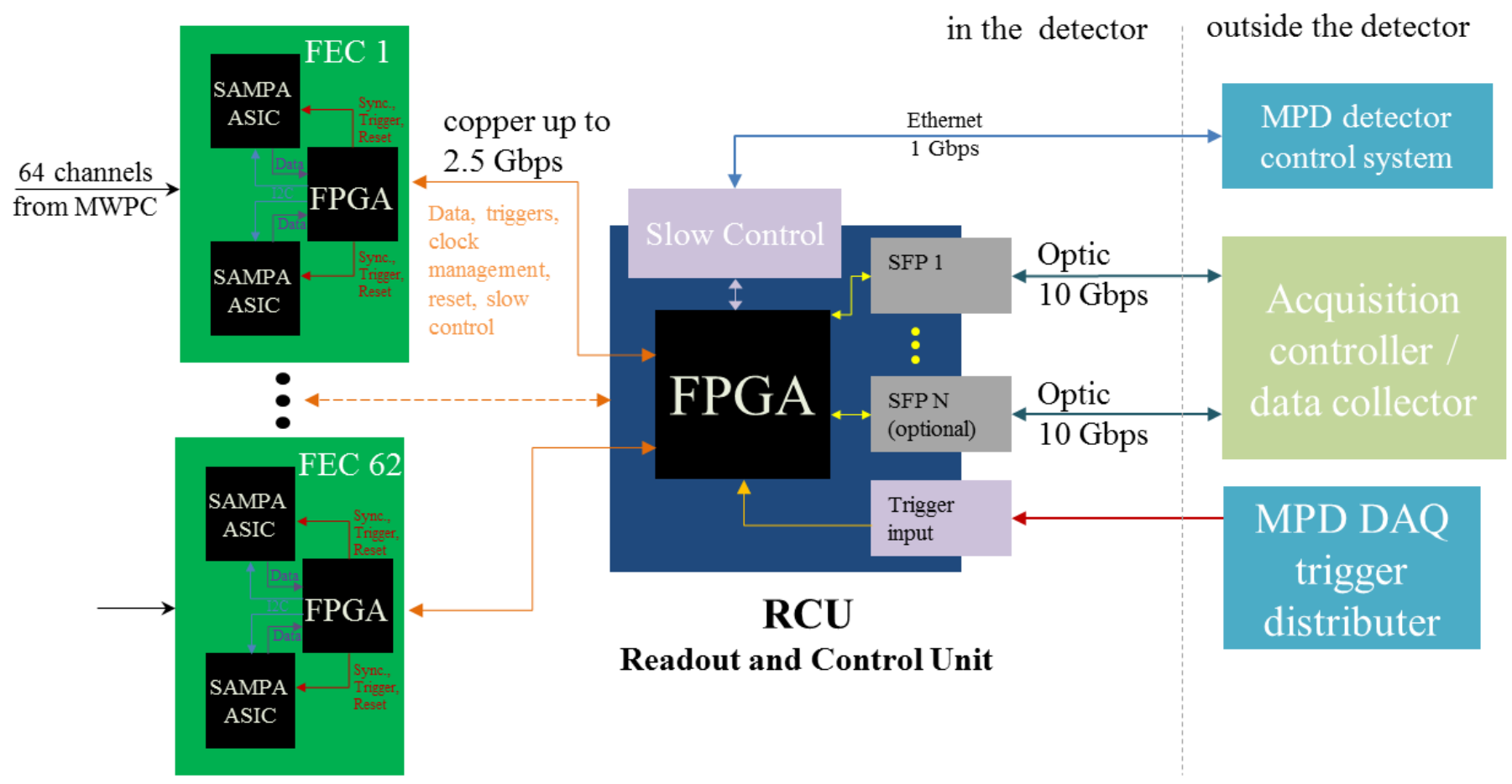
Two PCB form factor 28x91 mm^2

Concept of electronics integration on ROC



Design goal is to reduce the amount of material at the TPC endcaps and to distribute it evenly. That was achieved with double PCB card form factor.

Block diagram of one chamber readout (1/24 TPC)

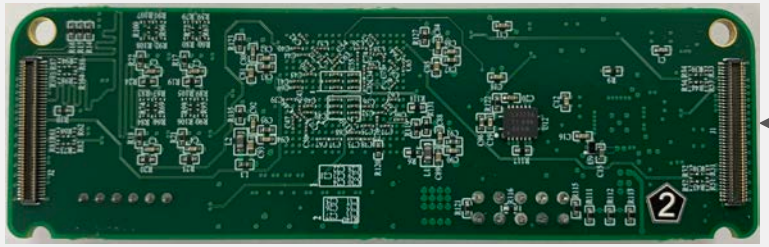


FEE status

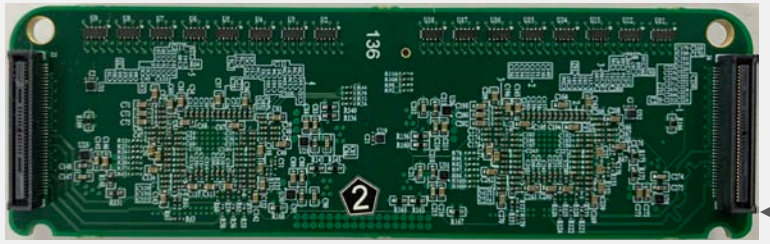
- Concept of the TPC data readout system has been determined.
- Actual size FEC (28x91 mm^2) satisfying integration demands has been designed, 34 FECs produced and tested right after manufacturing: 33 FECs are fully operational.
- RCU prototype based on Arria 10 development board has been prepared (firmware and transition cards for connection with FECs).
- Cable assembles for multichannel gigabit communication have been designed, produced and tested.
- Half-ROC testing system (2048 ch.) has been prepared. Testing is going.

The view of 64-channel FEC

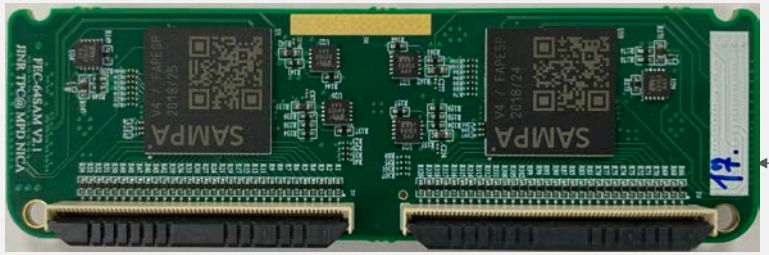
FEC controller
Top view



FEC controller
Bottom view

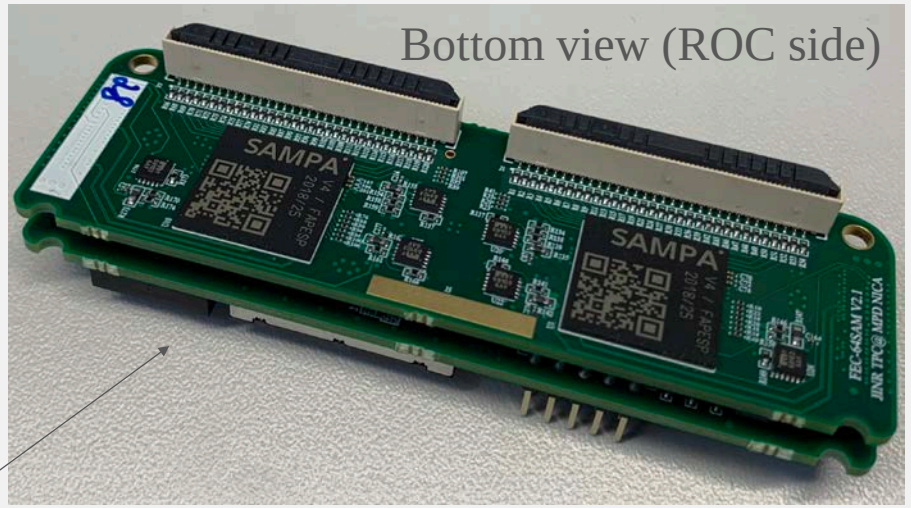


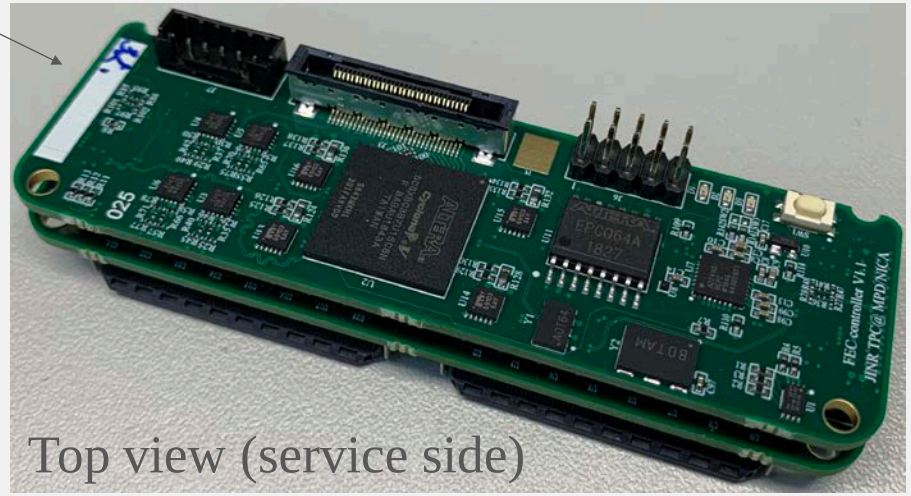
FEC assembly
view



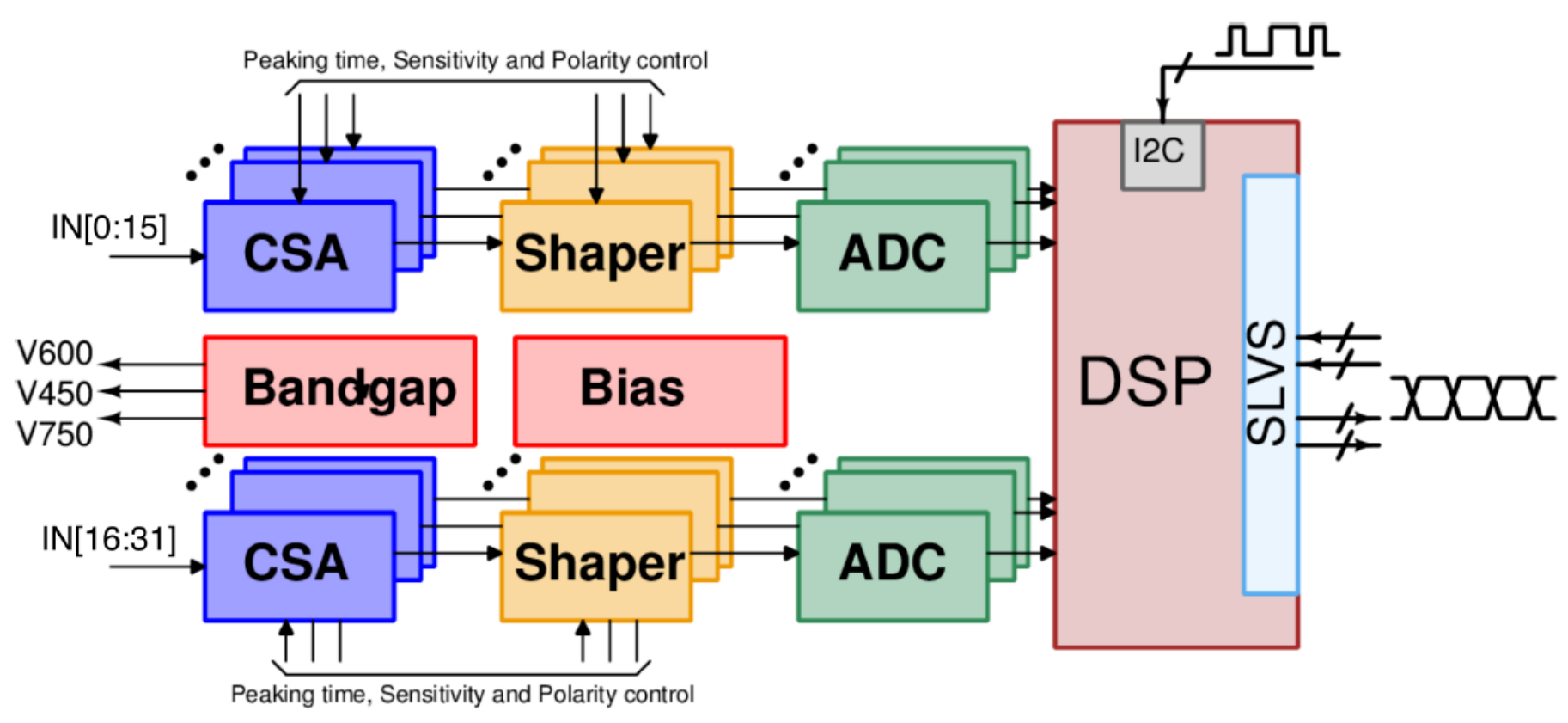
SAMPA FEC
Top view

SAMPA FEC
Bottom view





SAMPA ASIC: the core of FEE



[1] J. Adolfsson, et al., SAMPA chip: the new 32 channels ASIC for the ALICE TPC and MCH upgrades, JINST 12 (04) (2017) C04008.

FEC main parameters and functionality:

- The total number of registration channels: 64
- Input signal dynamic range: 100 fC
- ADC resolution: 10 bit
- ENC: les than 1000e^-
- SAMPA chips configured and controlled via FPGA
- Readout serial interface: up to 2.5 Gbps

➢*Double-PCB FEC provides opportunities for possible upgrade of the card readout.*

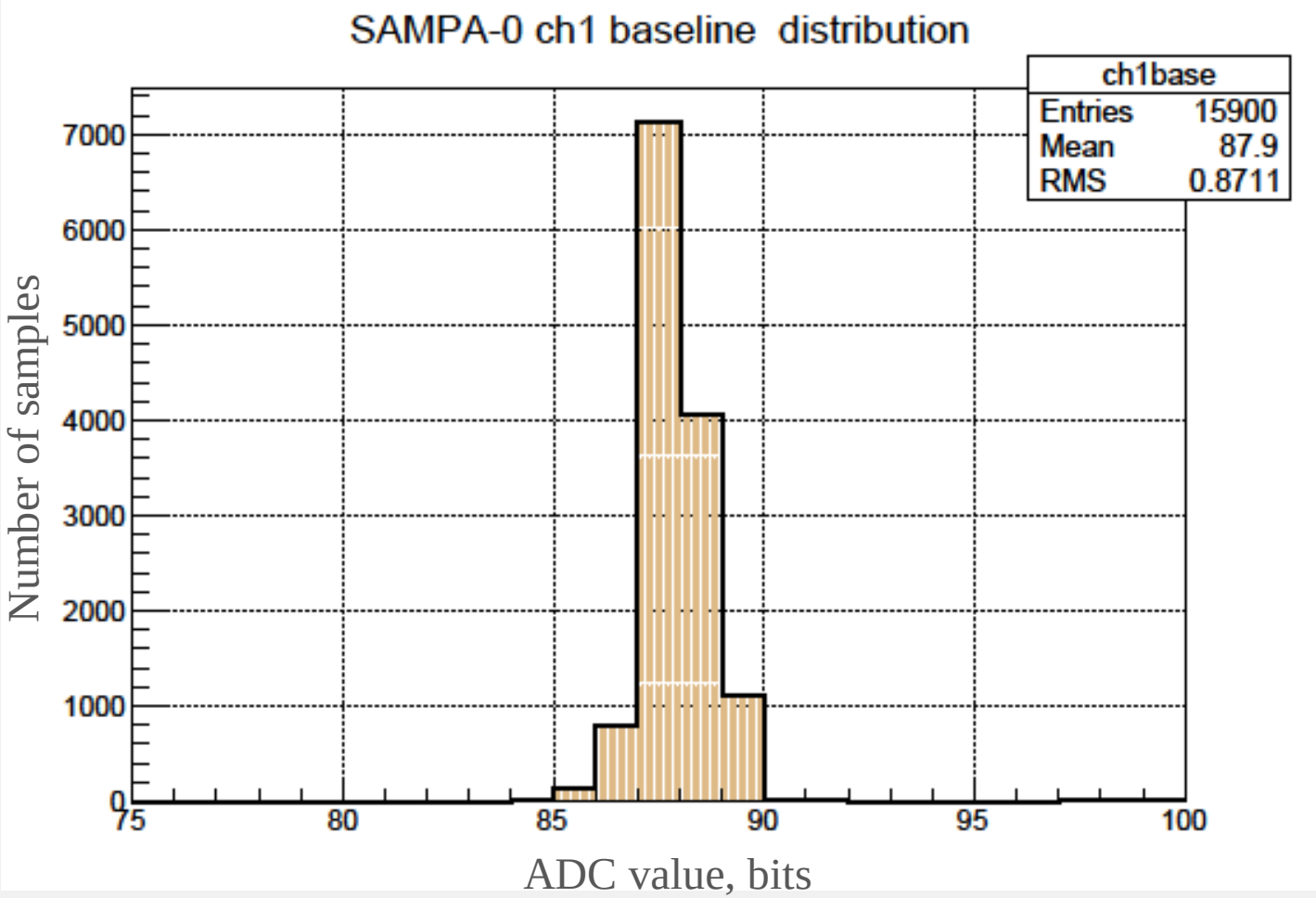
➢*Transfer of data and trigger signals was realized with the same high-speed serial interface.*

➢*16 values of currents, voltages and board temperatures are controlled with ADC.*

➢*Onboard circuit and embedded protection functionality against SEU are provided.*

➢*Remote system update for FEC firmware was provided.*

Typical noise distribution of a SAMPA channel

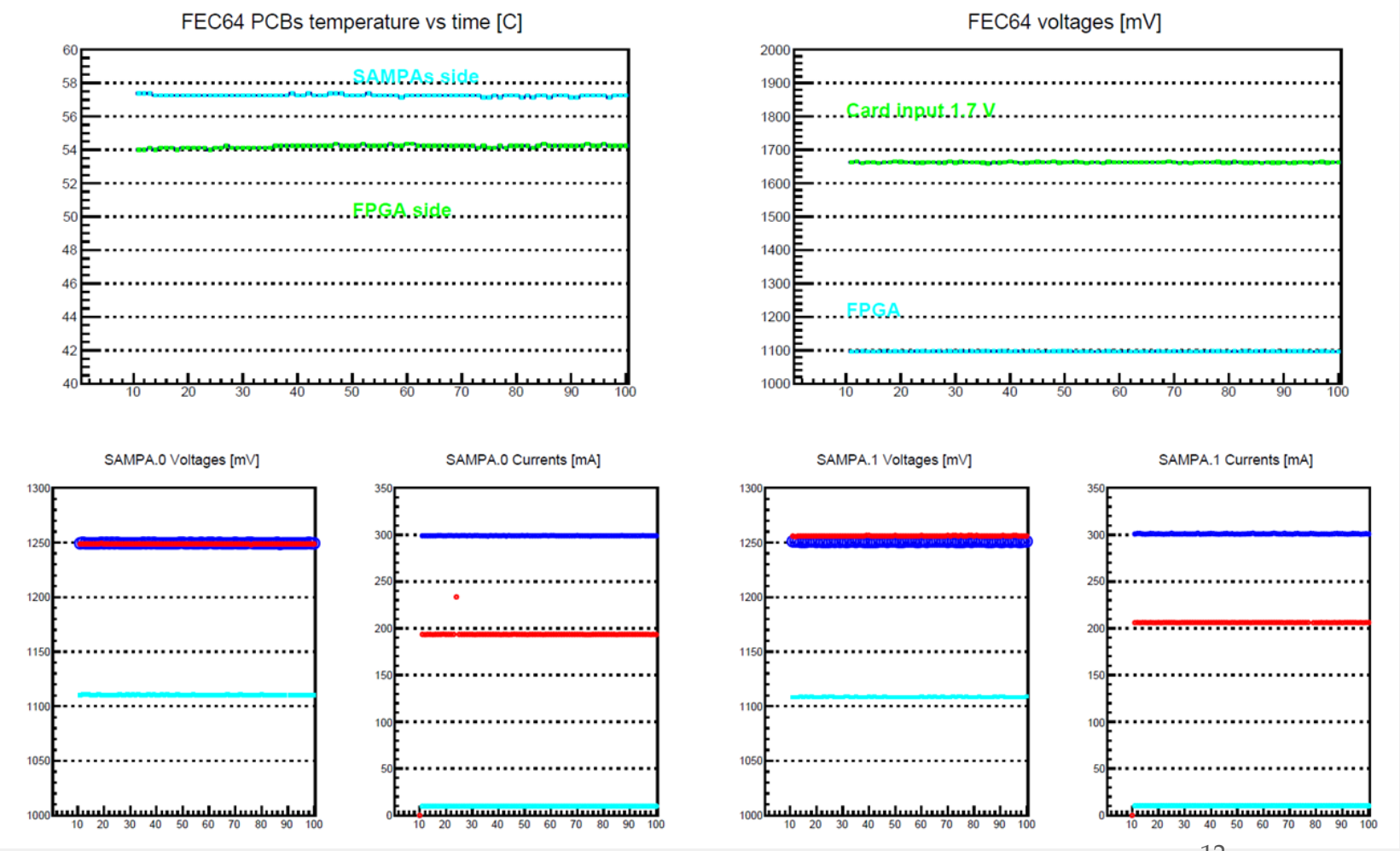


1 ADC LSB = 670 e^-

Measurement was done without connection with ROC

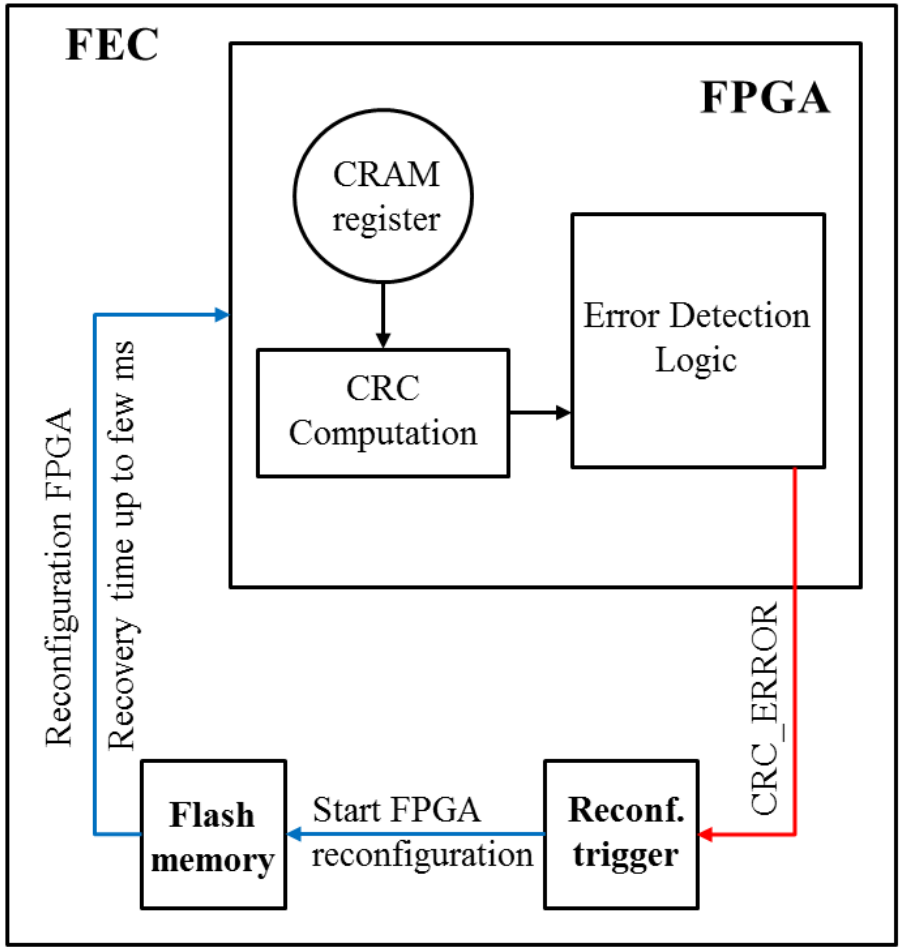
FEC slow control data

16 values of voltages, currents and temperatures are continuously measured on each FEC. The FPGA control state machine processes the data of the ADC and can form an interrupt vector.

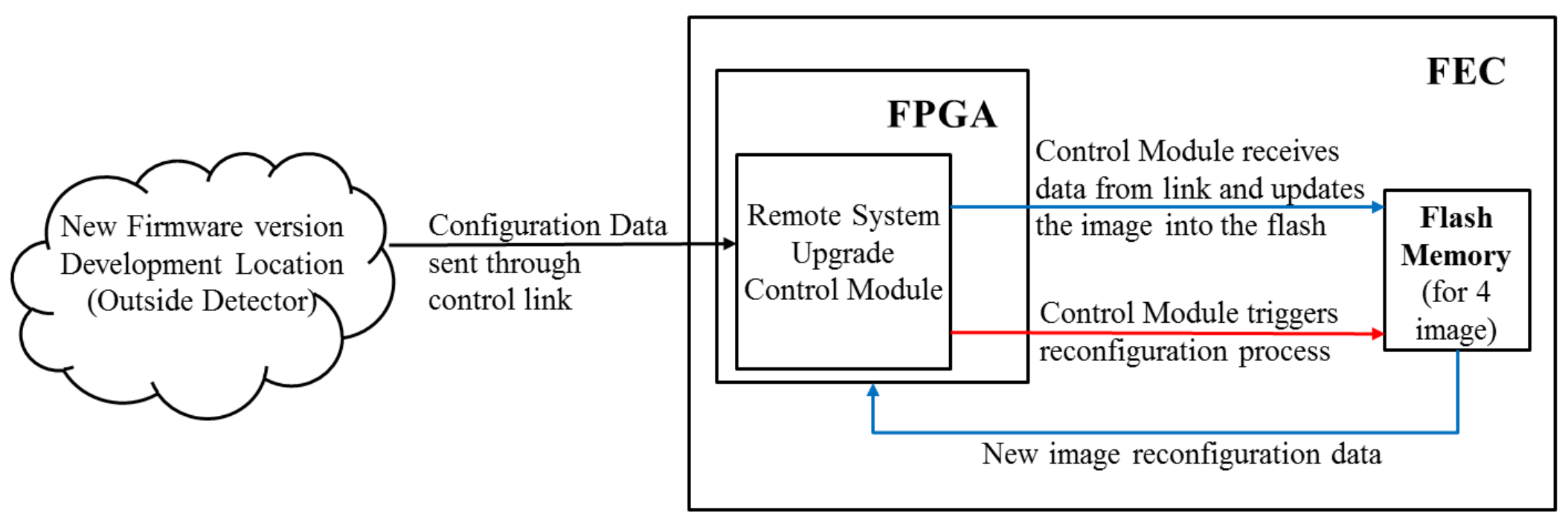


SEU recovery circuitry

- Due to the FECs operation in a radiation environment, it is reasonable to have mechanisms to protect the FPGA firmware from SEU.
- The CRC circuit can detect all single-bit and multi-bit errors within the FPGA configuration memory.
- In the case of detecting a firmware error, the onboard trigger initiates the reconfiguration process from the external flash memory.



Remote firmware update



Anticipating limited access to the electronics installed on the detector, it is desirable to provide a remote update of the firmware. Remote firmware upgrade feature was implemented into the FPGA design of the FEC controller.

Key features of Intel 20nm FPGA for RCUs system core:

- Intel 20nm FPGA Arria 10 was selected as a base of data readout.
- Embedded 72 transceivers are sufficient to implement the RCU on a single FPGA.
- ALMs and memory resources allow implementing all the necessary data transfer system algorithms
- Excess FPGA resources allow further system improvement

Flow Summary

<<Filter>>

Flow Status	Successful - Fri Sep 27 13:48:04 2019
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Pro Edition
Revision Name	top
Top-level Entity Name	top
Family	Arria 10
Device	10AX115S2F45I1SG
Timing Models	Final
Logic utilization (in ALMs)	22,658 / 427,200 (5 %)
Total registers	44746
Total pins	178 / 960 (19 %)
Total virtual pins	0
Total block memory bits	29,797,388 / 55,562,240 (54 %)
Total DSP Blocks	3 / 1,518 (< 1 %)
Total HSSI RX channels	34 / 72 (47 %)
Total HSSI TX channels	34 / 72 (47 %)
Total PLLs	44 / 144 (31 %)

Resources estimate for RCU design.

Half-ROC (2048 ch. ~ 2%of full TPC) readout system

1) RCU prototype;
2) Optical interface to upstream system;
3) Micro-coaxial cable assemblies;
4) FECs;

Conclusion

- ✓The FEE for the TPC has been designed on the base of the ASIC SAMPA and Intel FPGAs with high-speed serial links.
- ✓The FECs form factor of 28x91mm^2 conforms to the detector design constraints.
- ✓34 actual size FECs have been produced and tested: 33 are good.
- ✓TPC readout system prototype testing has started. The system is considered as a starting point for full-featured TPC readout system design.

Thank you!