Upgrading and Commissioning of the Inner Tracking System of ALICE

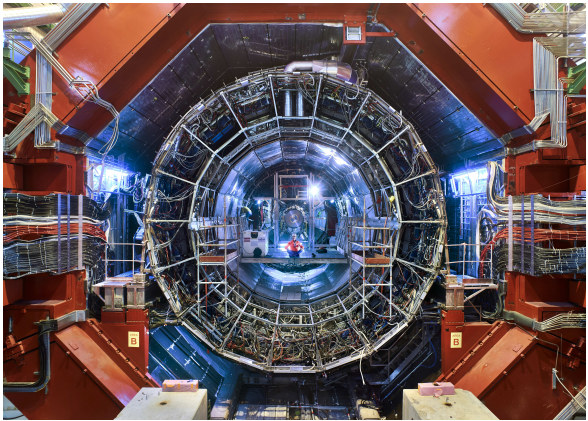
INSTR'20

James Iddon [1] on behalf of the Alice Collaboration

[1]University of Liverpool

February 25th, 2020

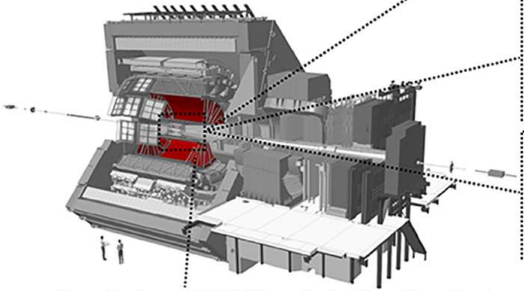
Introduction



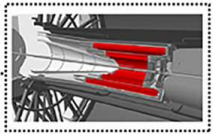
- ALICE is the dedicated heavy ion experiment at the LHC
- The main goal of ALICE is to characterise the Quark-Gluon-Plasma
- At extreme temperatures and densities colour confinement of quarks and gluons breaks down
- Heavy flavour measurements and low-mass dielectrons are a prominent part of the Run 3/4 physics programme
- The Pb-Pb interaction rate during Run 3/4 will be $50 kHz$

Outline of the ALICE upgrade

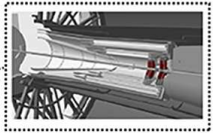
ALICE O2 Project:
- New online and offline data processing
- To cope with data rate of 1TB/s for Pb-Pb, two order of magnitudes higher than Run 1



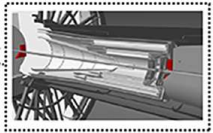
New design of **TPC** (Time Projection Chamber):
- Uses GEMs instead of MWPCs
- Readout rate improved from 2-3kHz to 50kHz



New **ITS** (Inner Tracking System):
- Entirely MAPS design
- Improved pointing resolution
- Improved tracking efficiency
- Improved readout rate



New **MFT** (Muon Forward Tracker):
- Same technology as the ITS
- Increased pointing resolution for muon tracks at low transverse momentum

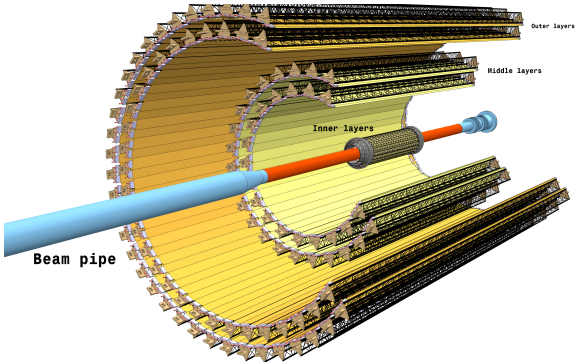


New **FIT** (Fast Interaction Trigger):
- Primary forward trigger, luminosity and collision time measurement detector
- Also determines centrality, multiplicity and reaction plane in Heavy Ion collisions

The ITS upgrade

Improve physics reach for low-mass dielectrons and rare probes at low p_T e.g.: B mesons, D meson, Λ_c baryon by improving vertex resolution, tracking efficiency and readout rate.

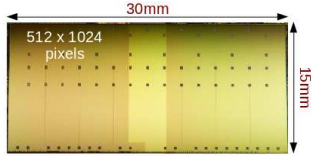
- 7 cylindrical layers with $10m^2$ of active area based on Monolithic Active Pixel Sensors (MAPS)
- increase the readout rate to $100kHz$
- reduce pixel size from $425\mu m \times 50\mu m$ to $O(30)\mu m \times O(30)\mu m$
- reduce the radius of the innermost layer from $39mm$ to $23mm$
- Material budget:
  - Inner Barrel: material budget of $0.35\% X_0$/layer
  - Outer Barrel: material budget of $1.1\% X_0$/layer

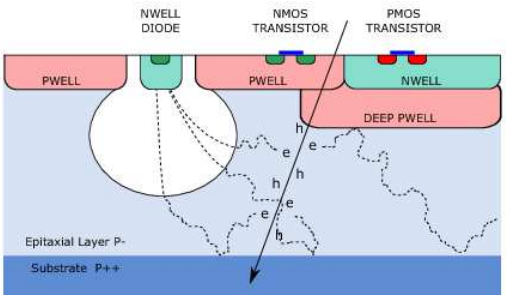


Total 12.5G pixels

ALice PIxel DEtector

- TowerJazz 180nm imaging process
- Deep p-well shields PMOS transistors
- Radiation tolerant: 270$krad$ TID, 1.7x10^{12} Mev/n_{eq} NIEL (expected dose after 10 years operation in ITS)
- Reverse substrate bias to increase depletion
- 1 $k\Omega cm$ epitaxial layer
- 2 μm diameter, low capacitance n-well diode (pixel size: 27μm x 29μm)
- 100μm and 50μm thick silicon for the Outer and Inner Barrels respectively
- Ability to mask pixels



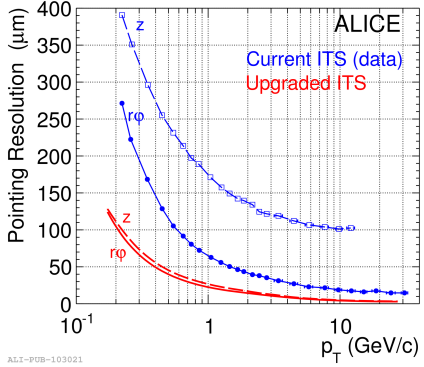


- 130,000 pixels/cm^2
- spatial resolution: $\approx 5\mu m$
- power: $\approx 300nW/pixel$, $40mW/cm^2$
- fake hit rate: $\ll 10^{-6}$

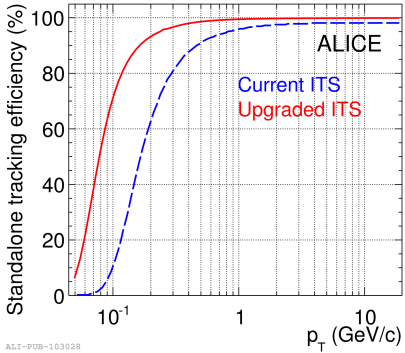
The ALPIDE chip is a MAPS. It has an amplifier, signal shaper, discriminator and multiple event buffers in-pixel. As well as in-matrix data sparsification.

ITS upgrade performance

- x3, x6 improvement in rφ, z for 0.5Gev/c π
- $\approx 40\mu m$ at $500MeV/c$ (low p_T)

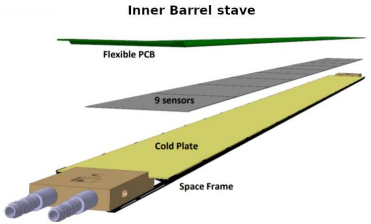


- $> 60\%$ for 0.1Gev/c π
- $> 95\%$ for π with $p_T > 0.3GeV/c$

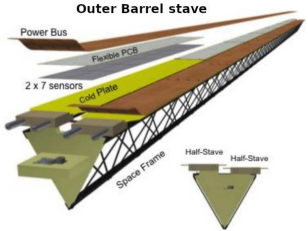


Design of the ITS

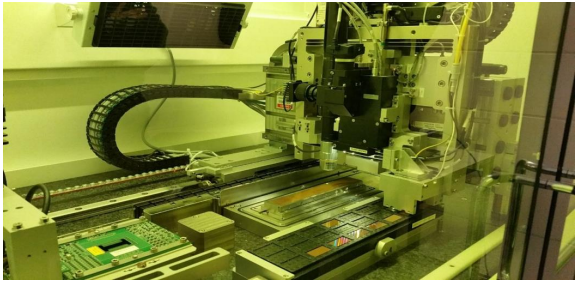
- **Inner Barrel stave:**
  - Consists of one inner barrel module and support structure
  - Length: 270*mm*
  - Three layers at avg radial position (mm): 23, 31, 39
  - Number of staves: 12, 16, 20
  - Number of chips per stave: 9



- **Outer Barrel stave:**
  - Split into two half staves
  - Length: 844*mm* (middle layer (ML)), 1475*mm* (outer layer (OL))
  - Four layers at avg radial position (mm): 194, 247, 353, 405
  - Number of staves: 24, 30, 42, 48
  - Number of chips per stave: 112 (ML), 196 (OL)

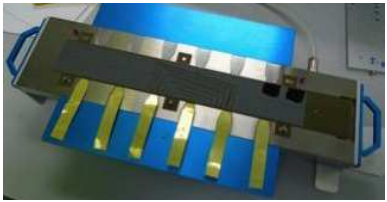


Module Assembly

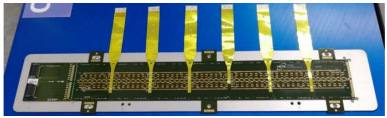


Module Assembly Machine

- automated chip placement
- accuracy of $5\mu m$
- $\approx$ 7M pixels per module



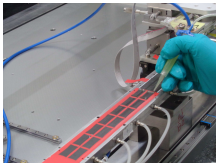
One Outer Barrel module seen from the silicon side



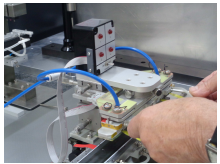
One Outer Barrel module seen from the FPC side

Construction of Outer Barrel Staves

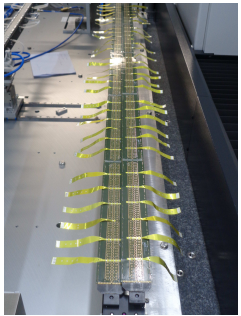
- **Construction steps**
  - Align Hybrid Integrated Circuit (HIC) above cold plate with Coordinate Measuring Machine (CMM) ($<$50 μm)
  - Glue HIC to cold plate
  - Align half stave to space frame with CMM
  - Glue half stave to space frame
  - Solder power bus to each half stave
  - Fold power bus



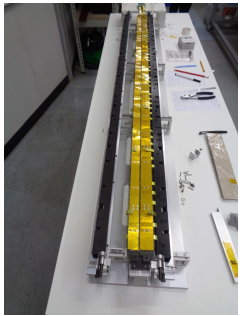
prepare glue mask on cold plate



align HIC above cold plate

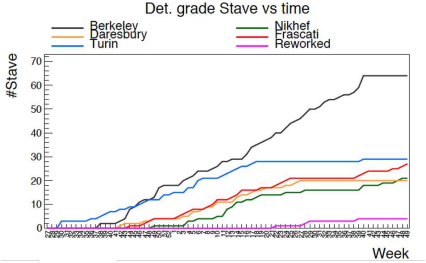


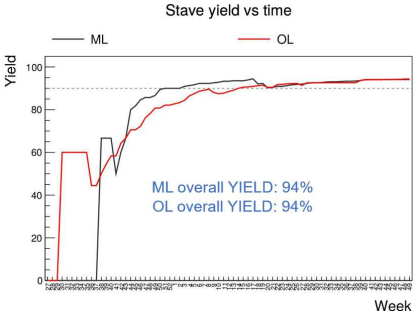
Stave without the power bus. The gold strips are the cross cables to which the power bus is soldered.



After folding the power bus. The power bus, once folded, protects the delicate wirebonds connecting the FPC to the chips.

Outer Barrel production summary

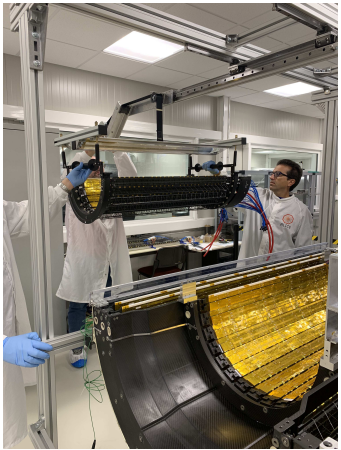




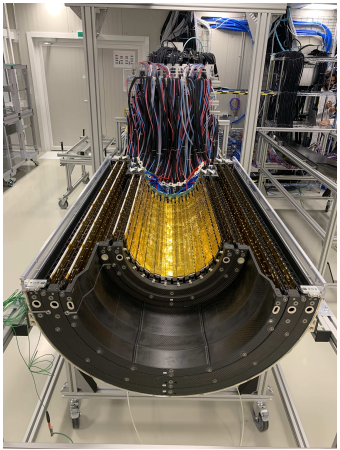
- Target yield: 90%
- 90 detector grade outer layer staves constructed at an overall yield of 94%
- Outer Layer (OL) production completed in December 2019
- 54 detector grade middle layer staves constructed at an overall yield of 94%
- Middle Layer (OL) production completed in October 2019

Assembly of Staves into Half Barrels

- All staves were verified during production, after arrival at CERN and again after installation in the Half-Barrels with a test system
- All staves are now assembled into Half-Barrels
- Basic verification with the production readout system done by reading PRBS pattern on the high-speed link
- Simultaneous operation of half barrels with final readout chain to ensure stability



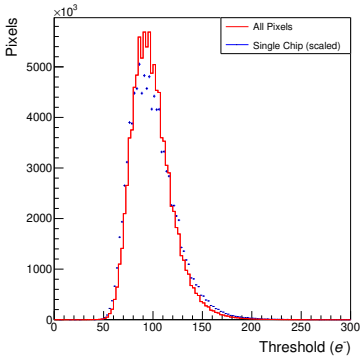
Installation of half layer 3



Outer barrel half barrel, fully installed

Half layer validation tests

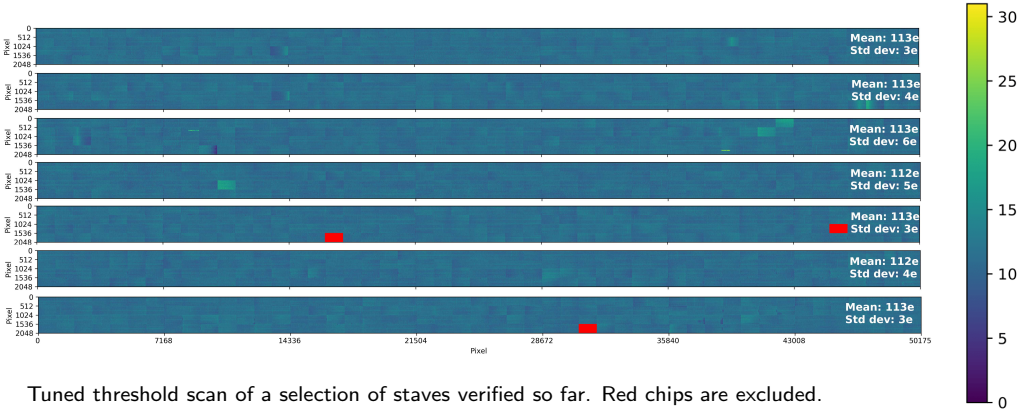
- Half layer:
  - Simultaneous readout of all staves connected to the same readout server
- For each stave:
  - Power stave and measure current consumption
  - Test of the control interface with read and write transactions
  - Threshold tuning adjustment of the front-end settings to achieve an average threshold of $100e^-$ for all chips
  - Fake-hit rate measurement: aquisition of events without external stimulus:
    - Measurement of cosmic muons and noise



Example result: threshold distribution of all 5×10^7 pixels on a stave (mean $99.4e^-$, spread $20.6e^-$) in comparison to a single chip (mean $100.2e^-$, spread $23.5e^-$) after tuning. Electron hole pairs liberated by an MIP $\approx 80\mu m^{-1}$

Half layer validation: Threshold Tuning

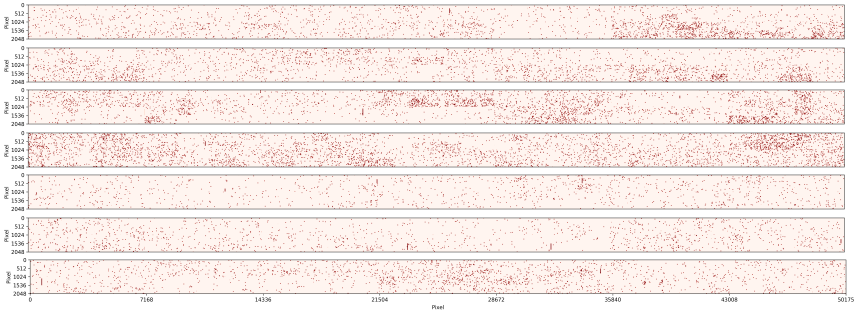
The threshold at which a pixel records a hit should be uniform across an entire stave and is tuned on a chip by chip basis. The average threshold value over the staves shown after tuning is $113e^-$, with a standard deviation of $3.6e^-$.



Tuned threshold scan of a selection of staves verified so far. Red chips are excluded.

Half layer validation: Fake Hit Rate

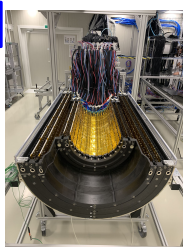
Each stave was left taking data with no stimuli to get a measure of the fake hit rate. Fake hit rate of these staves shown: $3.2x10^{-10}$/pixel/event. This is quieter than the requirement of 10^{-6}/pixel/event



Fake hit scan of a selection of staves verified so far. Carried out at $100kHz$ with tuned thresholds. Hit pixels are enlarged for visibility.

Timeline

November 2020: ITS fully assembled into Half Barrels and connected to services



December 2019: Construction of all staves (including spares) completed:
- ~ 280 staves, ~ 72000 chips, ~ 2600 HICs
- > 10 production sites in Asia, Europe and the USA

February 2020: Comprehensive verification of the Outer Barrel

March 2020: Collection of cosmic muon events with the Outer Barrel

July 2020: Installation of ITS in ALICE cavern

October 2020: Commissioning in ALICE Cavern

March 2021: Start of Run 3

Outlook

- The ITS is fully constructed and connected to services
- The readout software is nearing the end of development
- Simultaneous operation of multiple OB staves has been demonstrated
- Commissioning of the detector is ongoing
- **Next step:** measure cosmics in the Outer Barrel

Thank you for listening