The Readout system of the CBM Projectile Spectator Detector at FAIR

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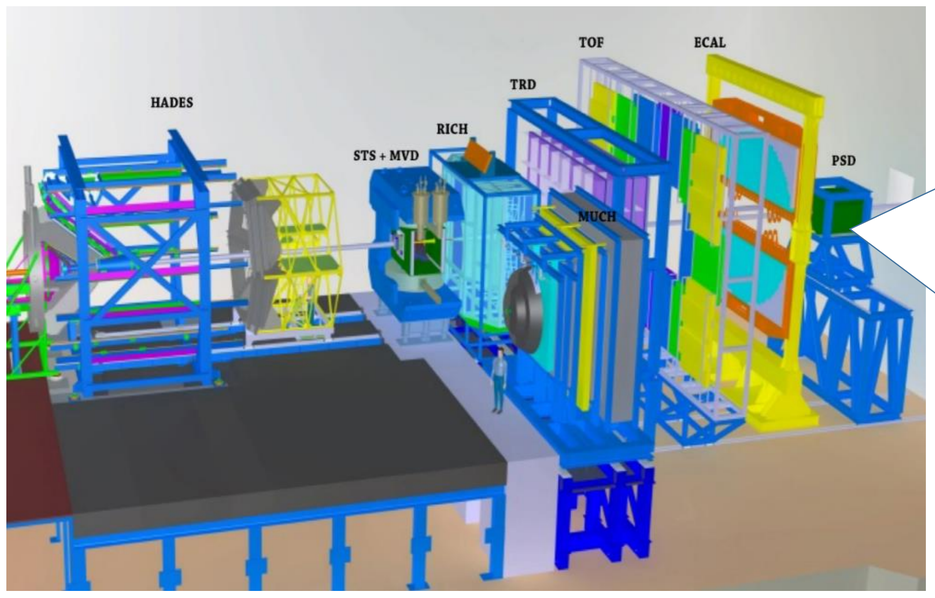
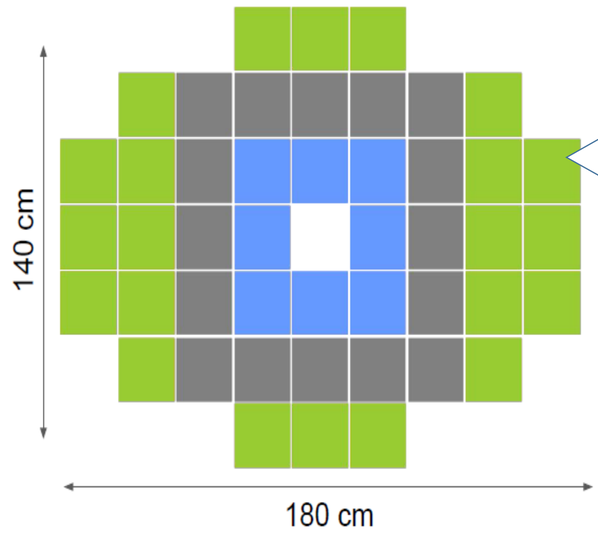
The Projectile Spectator Detector (PSD), a sampling lead/scintillator forward hadron calorimeter with transverse and longitudinal segmentation and with MPPCs photodetectors, will be used at the Compressed Baryonic Matter (CBM) experiment at FAIR to measure the centrality and orientation of the reaction plane in nucleus-nucleus collisions. After amplification in the FEE, signals from the MPPCs are readout with LMT9011 ADCs with 14 bit digitization and up to 125 Msps rate which has been developed for the ECAL of the PANDA experiment at FAIR. The Kintex 7 FPGA is used for signal processing and data collection. The trigger-less readout is based on the GBT-FPGA. Clock source switching from onboard generator to the RX clock transmitted via GBT has been implemented to integrate the ADC board into the CBM DAQ system. One PSD module has been integrated into the mCBM experiment at the SIS18 facility of GSI/FAIR joining the FAIR Phase-0 program. Details of the PSD readout electronics and first results of the data processing and transmission within the common, synchronized mCBM data transport taken during the data campaign in November/December 2019 will be presented are shown.

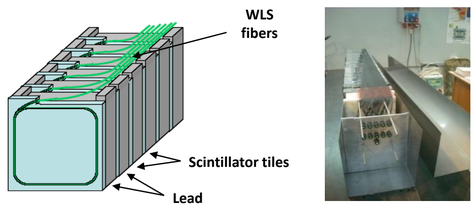


CBM will explore strongly interacting matter at highest net-baryondensities by investigating nucleus-nucleus collisions in fixed-target mode with extracted beams from the SIS-100 [1]

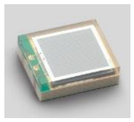
- high-rate capability of up to 10^7 interactions per second
- CBM will employ fast and radiation-hard detectors and readout electronics
- free-streaming data acquisition system
- self-triggered front-end electronics



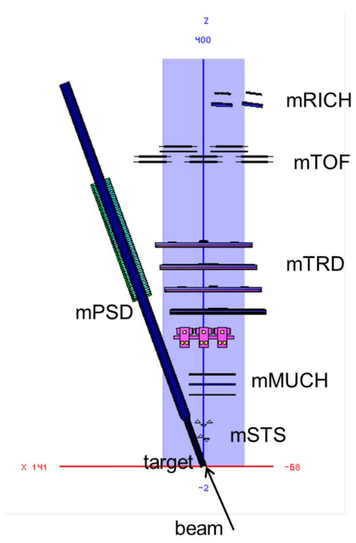
46 modules; 200x200mm² ; Beam hole 20x20 cm²; Total weight – 22t All modules already constructed by the end of 2017



- **Module transverse size 200x200mm² .**
- **Longitudinal structure: 60 Pb/Scint tiles layers: (Pb(16mm), Scint(4mm) grouped in 10 sections.**
- **Total length is 5.6 λ_{int}.**
- **Weight of each module 500 kg.**
- **Light collection – by WLS fibers from 6 sequentially placed scintillator tiles in one section to one optical connector at the end of module.**
- **Light readout: 10 MPPC (3x3mm²) per module.**
- **Readout electronics: sampling ADC.**



Hamamatsu S12572-010P
Sensitive area 3x3 mm²
Number of pixels 90 000
Nominal gain 1x10⁵
Pixel recovery time 10 ns



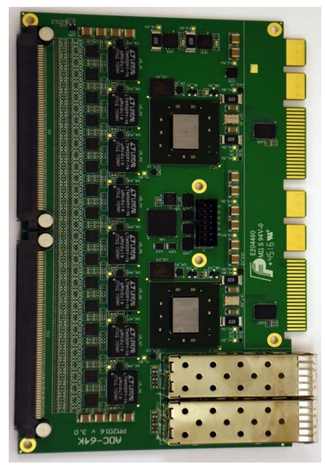
- mCBM focuses on the system performance aspect integrating existing (or currently under construction) prototype modules of all CBM detector subsystems into a common, high-performance free-streaming data acquisition (DAQ) system.
- mCBM facilitates detailed high counting rate tests for CBM detector components or Front-end Electronics (FEE)
- A single PSD prototype-module will be positioned directly under the beam pipe, 5° tilted relative to the beam axis while pointing to the target

PSD readout integration into mCBM DAQ

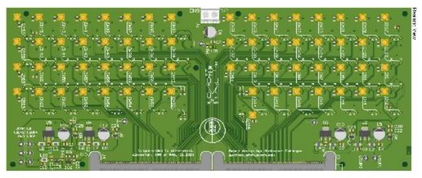
- One of PSD@CBM module was installed into mCBM cave in November 2019 for beam tests
- ADC board developed for ECAL@PANDA used for signal digitization and processing
- GBT protocol used for data readout, clock distribution and slow control
  - GBT REFCLK and ADC clock sourced from GBT frameclock
  - Implemented clock switching procedure from internal clock generator to GBT frameclock
- Integration into time synchronization system is implemented

ADC board features

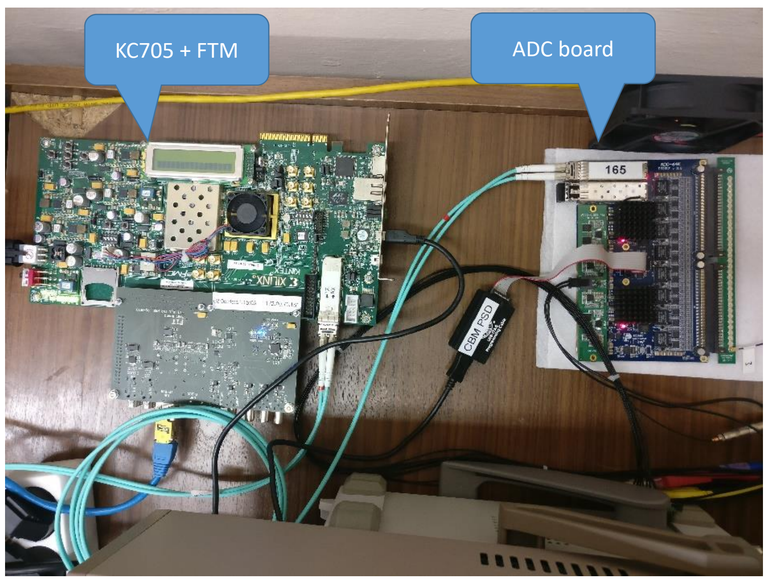
- LTM9011 ADC
  - 125Msps / 80Msps (used now)
  - 14-bit digitization
  - Selectable Input Ranges: **1VP-P (used)** to 2VP-P
- Two FPGA Kintex 7
  - 32 channels per one FPGA
  - Separated optical link for each FPGA
  - Signal processing on the fly
- Readout rate
  - 3.2 Gbit/s (GBT 80bit@40MHz)
  - Top limit: 3.2 Gbit/s / 32 channels / 1 MHz readout rate = 100bit/hit (80bit used now)



ADC board addon



- Add-on board is constructed to provide a single-ended interface for an ADC board.
- 64 single-ended to differential converters.
- Based on AD8138 IC, 50 Ohm terminated.
- Provides an adjustable input offset



Readout workbench based on Kintex 7 evaluation board in INR RAS, Moscow

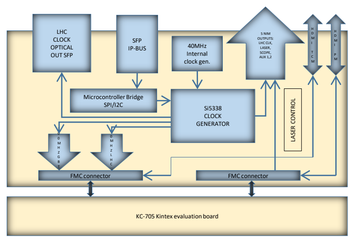
- **<u>FTM addon allow to collect to PC data send via GBT</u>**
- FTM addon used with Kintex 705 evaluation board
- Generate GBT MGTREFCLK clock
- SFP port for Ipbus communication (UDP based protocol)
- FTM addon developed for readout tests with FIT@ALICE

- Designed for FIT readout development in ALICE (LHC, CERN)
- KC-705 Development Board with XC7K325T-2FFG900C chip is used as FPGA
  - **Si5338** - I2C-PROGRAMMABLE QUAD CLOCK GENERATOR

Input clocks:
- 40 MHz internal

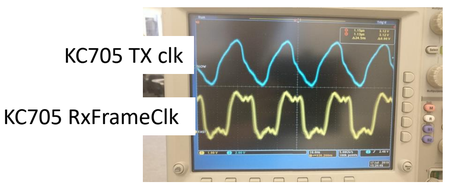
Output clocks:
- phase-controlled "LHC clock"
- phase-controlled Laser clock
- 200 MHz clock for GBT

- **"LHC Clock" Optical output**
- **IP-Bus** SFP connector
- **Microcontroller** for
  - Si5338 power-up configuring
  - SPI/I2C bridge to control Si5338
  - Clock status monitoring



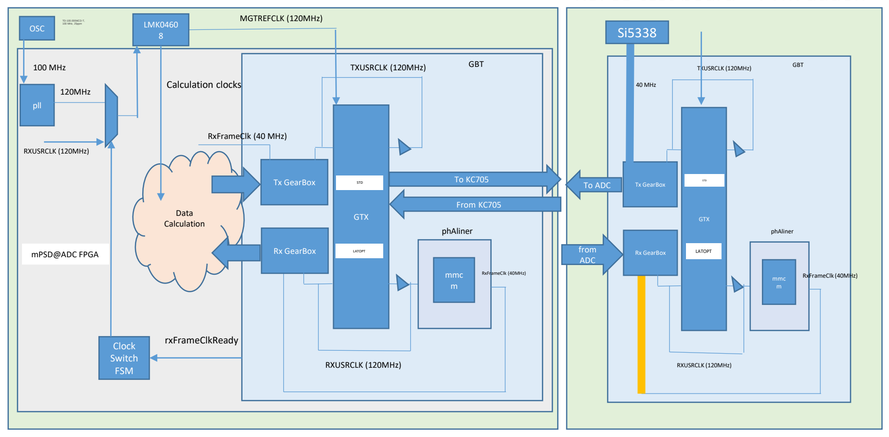
TEST board Incorporates
- CLOCK SUBSYSTEM
- IP-BUS INTERFACE
- GBT READOUT
- LASER PULSE SUBSYSTEM

GBT MGTREFCLK switching setup

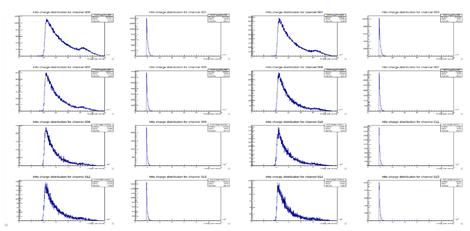


KC705 test board + FTM addon

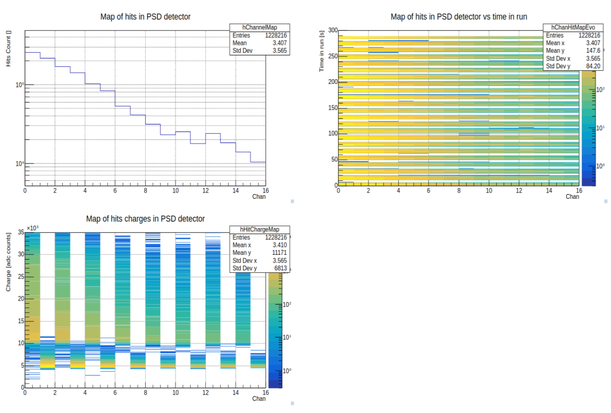
mPSD @ ADC board



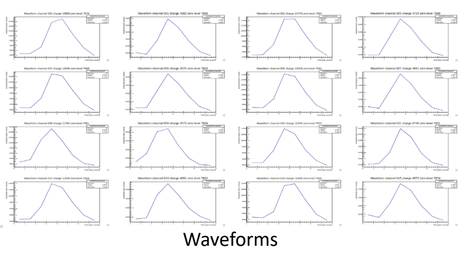
Online monitoring and data analysis



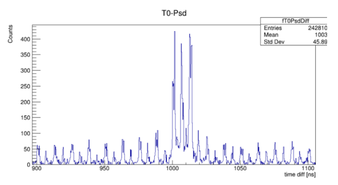
Charge spectra



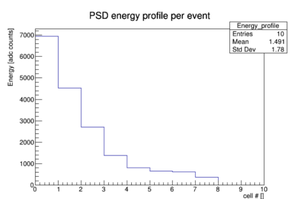
Monitoring summary



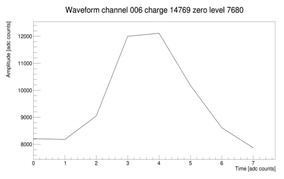
Waveforms



PSD – T0 event time correlation



PSD profile



Digitized waveform

During engineering run in November - December 2019 was tested:
- ADC readout firmware with real spills data taking
- Seen stable time correlation with other subsystems
- Reasonable energy spectra obtained
- Event monitor and Event digitization tested

[1] A CBM full system test-setup for high-rate nucleus-nucleus collisions at GSI / FAIR