Fast Interaction Trigger for MPD Experiment at NICA

V. I. Yurevich, S. A. Sedykh, S. V. Sergeev, V. Yu. Rogov, V. V. Tikhomirov, N. A. Lashmanov, A. A.Timoshenko, N. A. Kozlenko

Joint Institute for Nuclear Research, Dubna

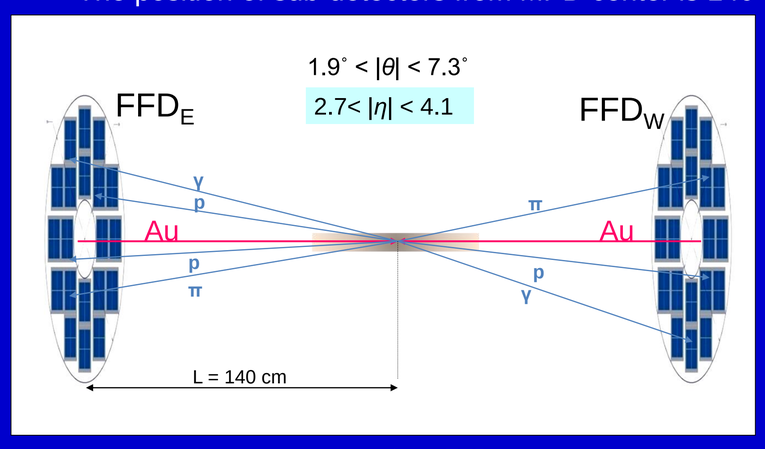
The Fast Interaction Trigger (FIT) System is an important part of the Multi-Purpose Detector (MPD) facility for study of Au + Au collisions with beams of NICA collider. The main aims of the FIT are fast and effective triggering of Au + Au collisions in the center of the MPD setup and generation of the T0- pulse for the TOF detector with time resolution better than 50 ps (sigma).

The FIT system consists of two modular arrays of Fast Forward Detectos - FFD_E and FFD_W with large active area and picosecond time resolution which is achieved by registration of photons from π^0-decays and high-energy charged particles produced in the collisions and sub detectors electronics

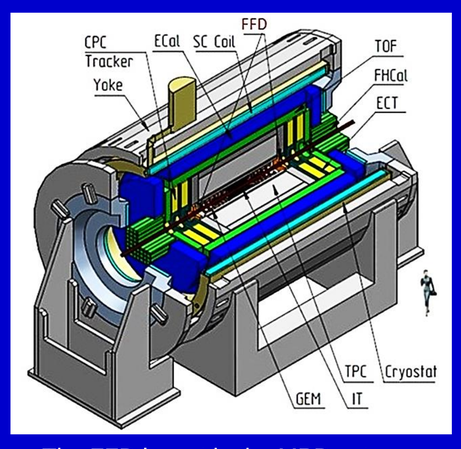
Concept of FFD

Each FFD sub-detector consists of 20 Cherenkov modules with 15- mm quartz radiators and MCP-PMTs XP85012/A1 (Photonis). The sub-detector granularity is 80 channels. It has outer diameter of 400 mm and a hole for beam tube of 96- mm diameter. The position of sub-detectors from MPD center is 140 cm.

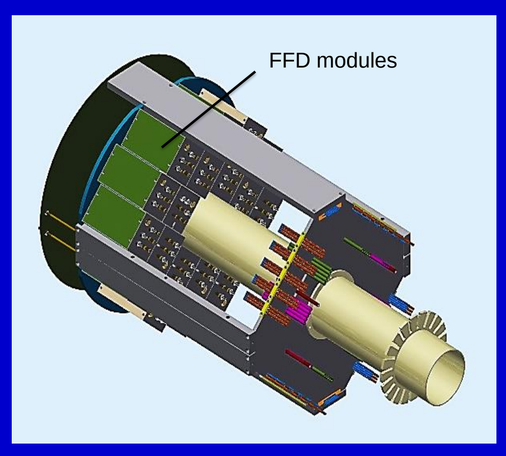
The photons are detected by its conversion into electrons in 10- mm lead plate. The quartz radiator of each module is made from four equal bars optical connected with MCP-PMT's window and it gives four independent channels of particle registration.



A schematic view of the FFD concept

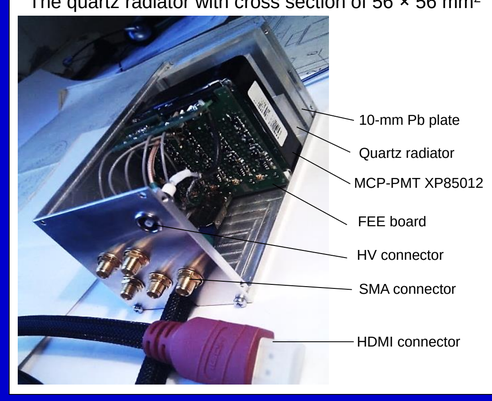


The FFD layout in the MPD setup



FFD sub-detector design

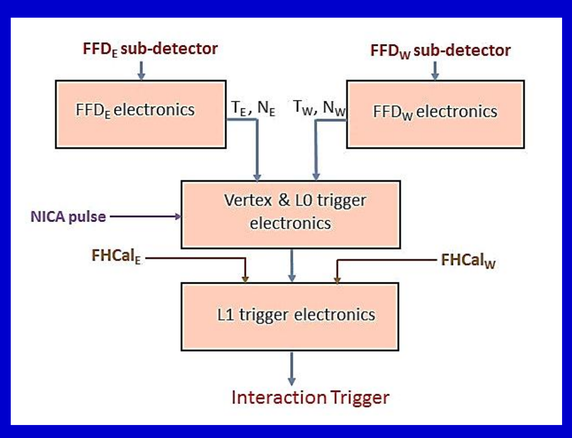
The module size is 66 × 66 × 110 mm³,
The quartz radiator with cross section of 56 × 56 mm²



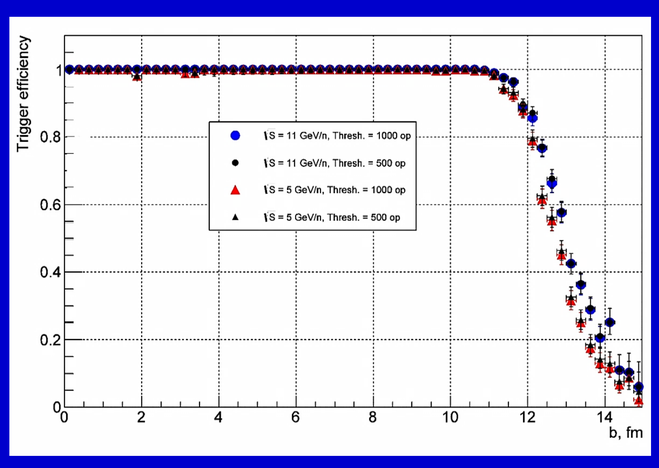
FFD module

Fast Interaction Trigger

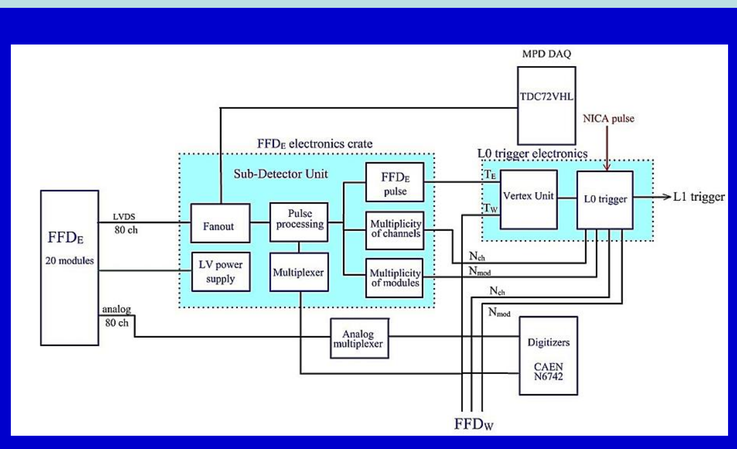
The fast vertex-trigger, provided by FFD, is the L0 trigger in MPD experiment. The fast determination of *z*-position of collision point by the vertex requires two pulses T_E and T_W produced by both sub-detectors FFD_E and FFD_W. The "good vertex" signal in coincidence with NICA pulse generates the L0 trigger pulse



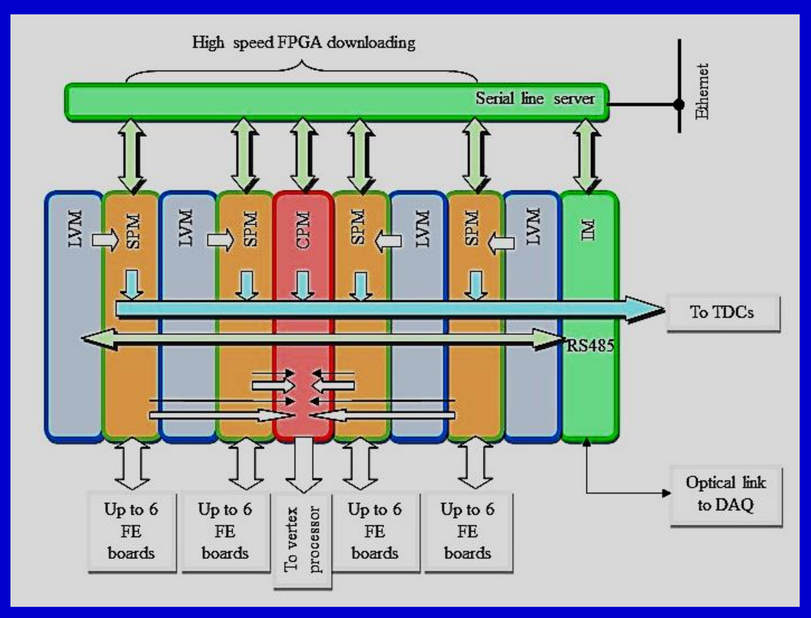
A scheme of the interaction trigger production.



The L0 trigger efficiency as a function of impact parameter of Au+Au collisions for two energies $\sqrt{S_{NN}}$= 5 and 11 GeV and threshold of 500 and 1000 Cherenkov photons



A Block scheme of SDU and L0 trigger electronics



The Sub-Detector Unit (SDU) has a modular structure in VME crate with custom backplane. It consist of:

- SPM – Signal processing module
- LVM – Low voltage module
- CPM – Central processing module
- IM – Interface module
- CLM – Configuration load module

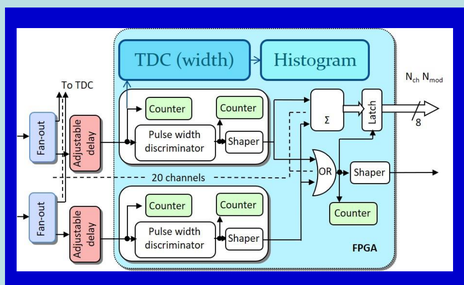
SPM has 20 (plus 4 in reserve) channels and each of them contains following elements:

- a fan-out 1:2 with Microchip chip SY58608U with jitter < 1 ps.
- A precise adjustable delay to align delays in all inputs. The delay value could be set with accuracy 10 picoseconds by a DCS.
- The pulse width discriminator (PWD) is incorporated in the SPM FPGA. The PWD allows to reject signals with low amplitude and therefore having short signal. This PWD could be adjusted with ~0.7 ns step by the DCS using the serial link. We expect that 5-7 ns rejection time could be good enough to suppress small amplitude pulses.
- Summing unit is used to calculate the multiplicity of signals in individual FEE channels and in FFD modules. The output of this unit is latched by the delayed and shaped fastest input signal generated by ORing of all input individual cell signals. The values of multiplicities are transmitted as 8-bit parallel code together with the strobe to the SDU Central Processing Module via back-plane.
- Counters are used for FEE monitoring and for the FEE signals alignment. The counters are red-out from FPGA by the serial link.
- All communications between SPM sub-modules like delay board or a signal processing FPGA and the FFD DCS is performed by the RS485 serial link via the crate back-plane.

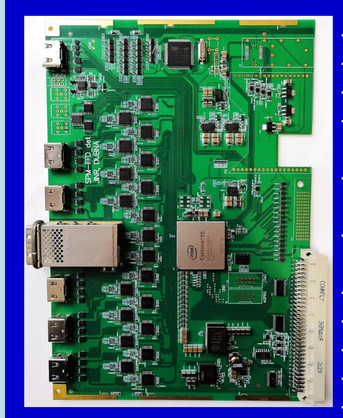
The CPM collects information from all SPMs of SDU and sends sum number of all lighted sub-detector FFD cells and modules to the Vertex processor and to the L0 Trigger processor via a cable with Molex 76105-0585 connector. The same module is connected to a TDC. In addition, this module builds multiplicity distribution histograms for SPM modules and counts SPMs strobe signals. The CPM is also controlled by the via back-plane RS485 serial link.

The Vertex Unit (VU) uses preprocessed data coming from the both SDUs (SDU_E, SDU_W).The length of cable coming from the FFD_W side is as short as possible and its signal arrives to VU before the signal of FFD_E side. The pulse of the right branch is used as the start signal for vertex coordinate processing and it generates the "Vertex gate signal". The arrival of the left branch signal during the "Vertex gate signal" means that the interaction takes place inside an acceptable range in the center of MPD setup. The geometrical boundaries of the acceptable interaction area are selected and tuned by the adjustable delays of the first branch signal and gate length.

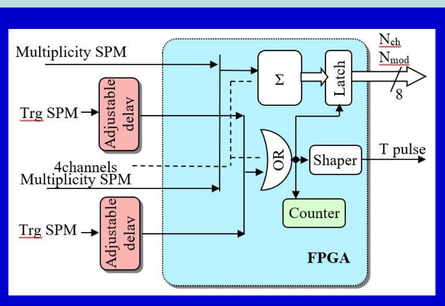
Sub-Detector Electronics Unit



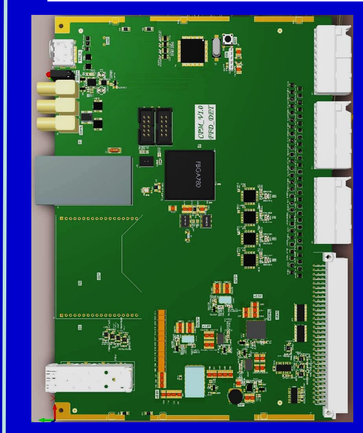
Block diagram of Signal processing module (SPM)



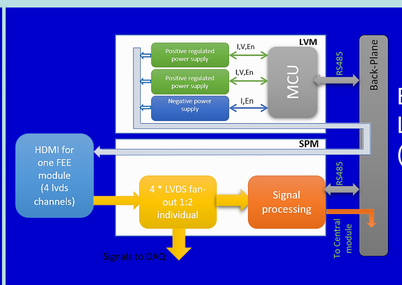
- Up to 5 FEE modules
- 4 IO TTL 50ohm
- 24 output for TDC
- 20 input channels with 10 ns delay and 10 ps step
- 2 input channels with discriminator
- 1 AUX (RST, REF, CLK, Reserved signals)
- Optical link
- 16bit IO backplane bus
- 16 LVDS backplane bus
- RS485
- Configuration load module



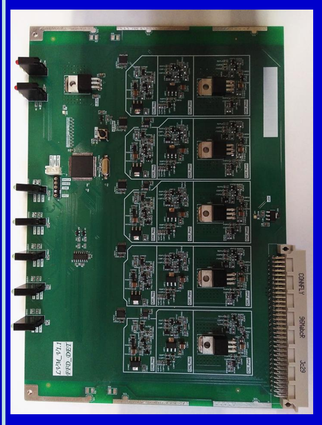
Block diagram of Central proccing module (CPM)



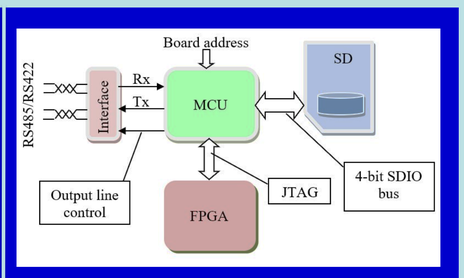
- Support Up to 4 SPM
- 4 IO TTL 50ohm
- 24 output for Vertex processor
- 4 input channels with 10 ns delay and 10ps step
- 2 input channels with discriminator
- 1 AUX (RST, REF, CLK, Reserved signals)
- Optical link
- 16bit IO backplane bus
- 72 LVDS backplane bus
- RS485
- Configuration load module



Block diagram of Low voltage module (LVM)



- Negative voltage channel, max. current 500 mA at 7.3 V,
- 2 positive channels, max. current: 800 mA, voltage range: 4.0 – 8.0 V with ~1 mV step,
- The voltage setting with 12-bit DACs.
- Output voltages and currents are read back with 12-bit ADCs



The CLM is used to download FPGA configuration "in the flight". Since the SDU is located in a restricted access area the special attention has been applied to provide fast FPGA configuration downloading.