Signals in the Well Electron Multiplier with the DLC anode (part II)

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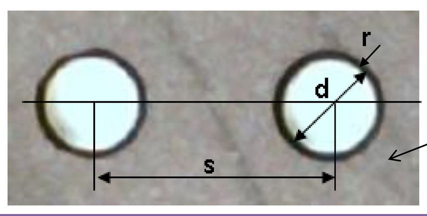
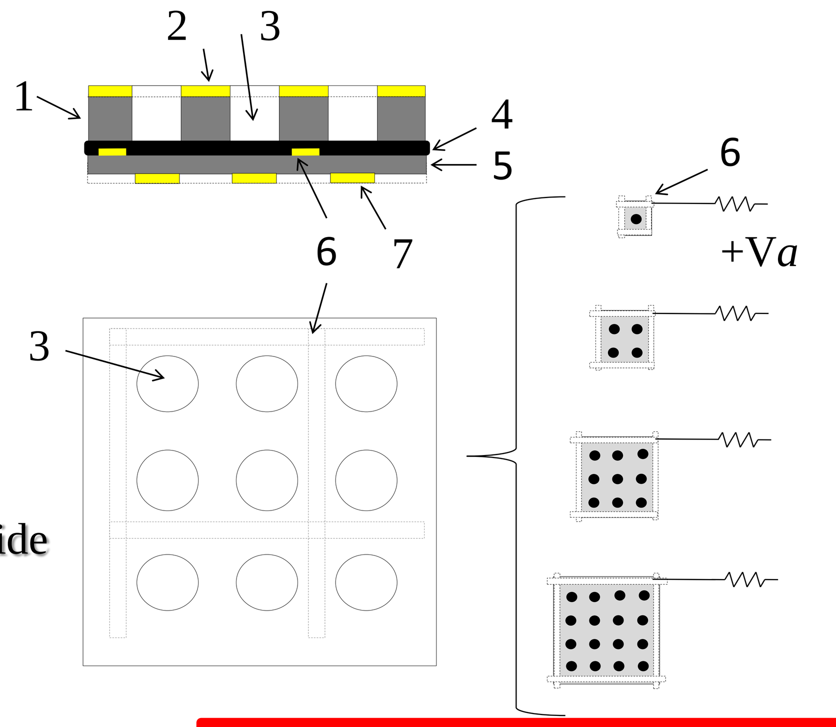
Design details



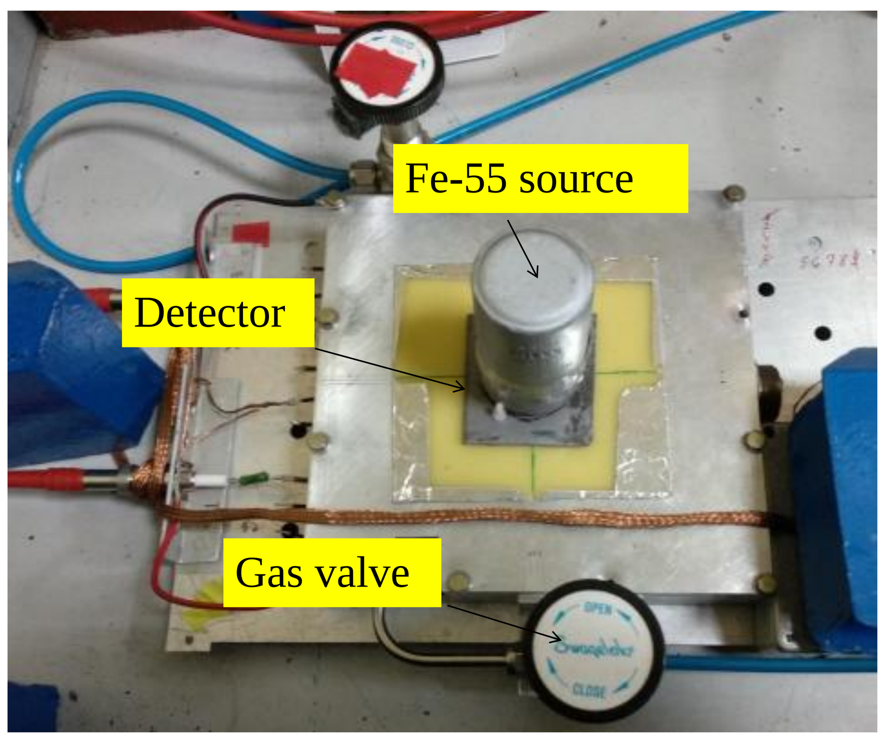
s=500 μm, d=200 μm, r~15 μm
Thickness 500 μm (FR4)



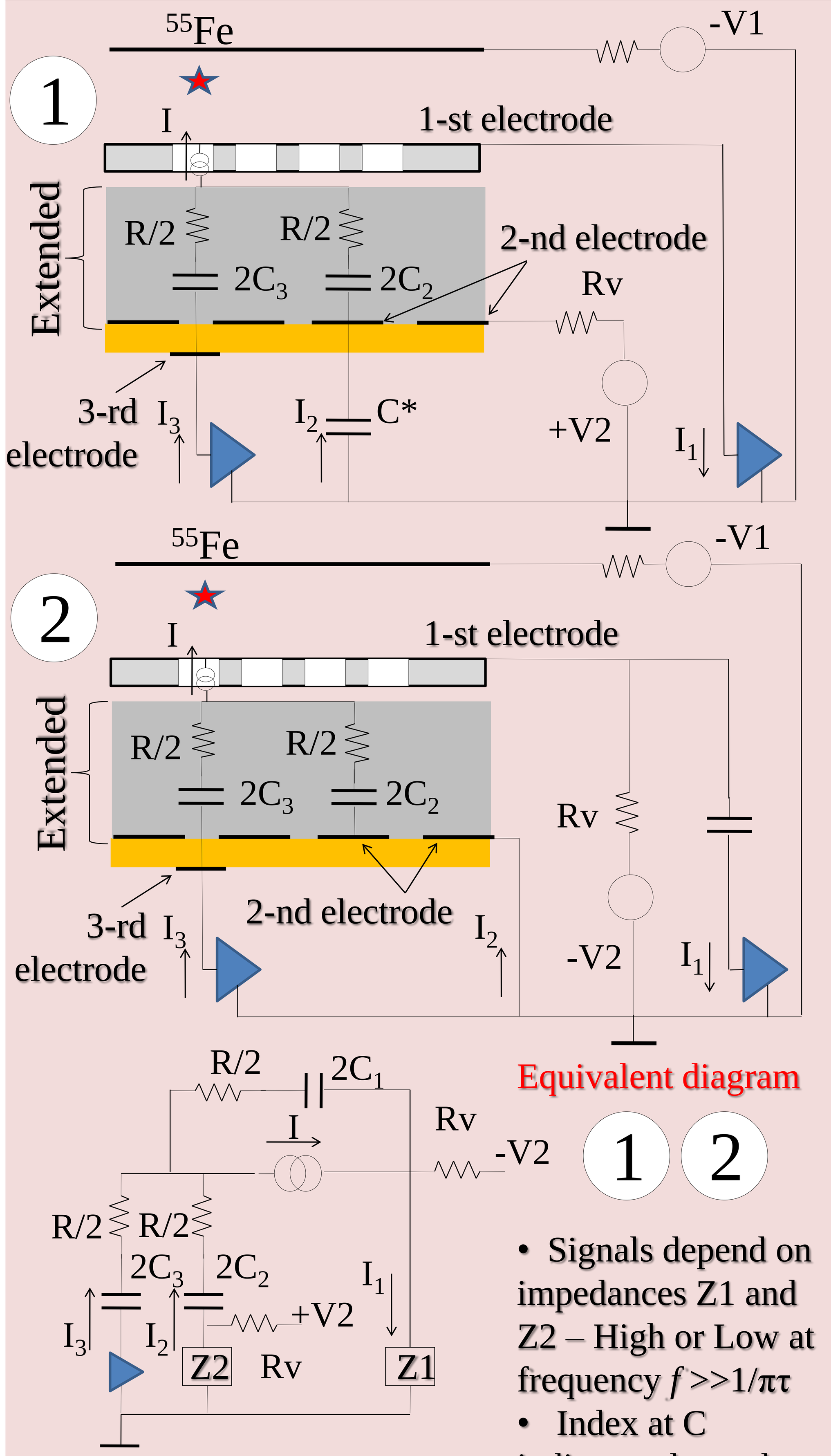
1 Dielectric substrate with Copper on one side
2 1-st electrode (cathode)
3 Well-like hole
4 DLC layer (anode)
5 Dielectric substrate with Copper on both sides
6 2-nd electrode (Copper mesh)
7 3-rd electrode (strip/pixel readout)

Configurations for mesh surrounding 1 hole, 4=2×2 holes, 9=3×3 and 16=4×4 holes

Experimental setup

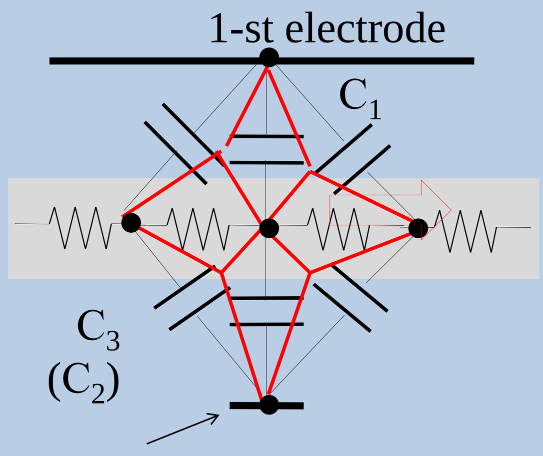


Detector schemas under tests

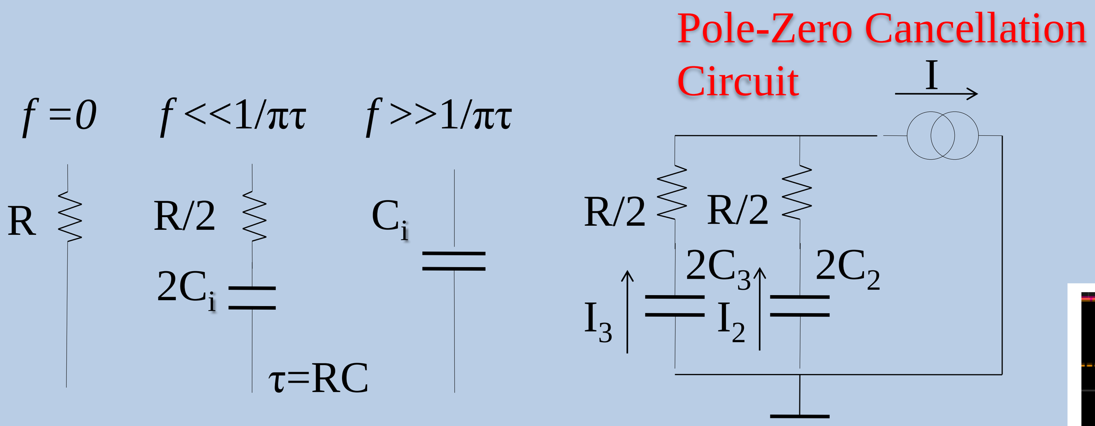


- Signals depend on impedances Z1 and Z2 – High or Low at frequency $f>>1/\pi\tau$
- Index at C indicates electrode number 1,2,3.

Equivalent diagrams for DLC layer as RC-system

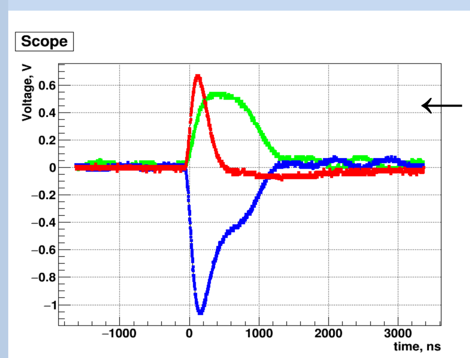


2-nd electrode
(3-rd electrode similar).
Capacitors normalized to RC-cell (per one hole)

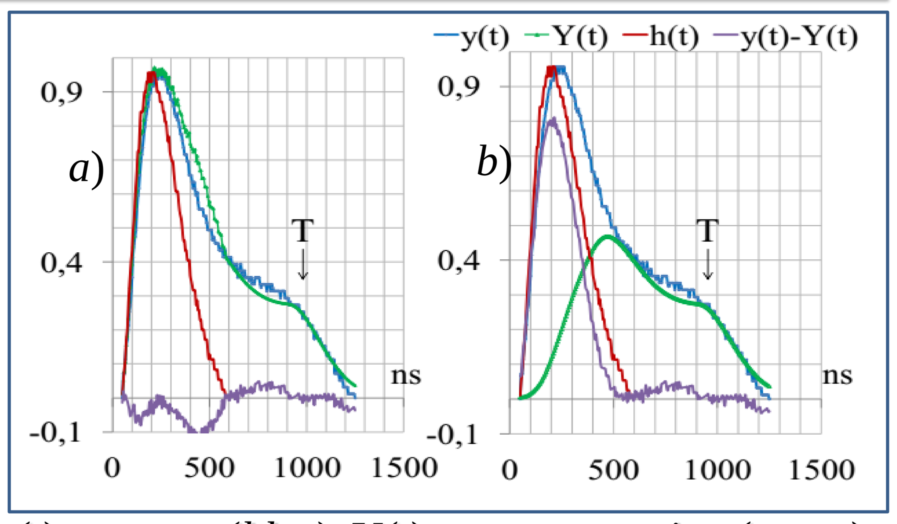


- At f=0 (d.c.) DLC layer is R.
- At low frequencies $f<<1/\pi\tau$ DLC layer is R/2 and $2C_i$ connected in series, where R is the surface resistivity, C_i - local capacitance to electrode i.
- At high frequencies DLC layer is C_i, where i=1 – the 1-st, i=2 – the 2-nd and i=3 – the 3-rd electrode.
- $\tau=RC_i$.

Input Signal Reconstruction delivered with amplifier Tp=150 ns

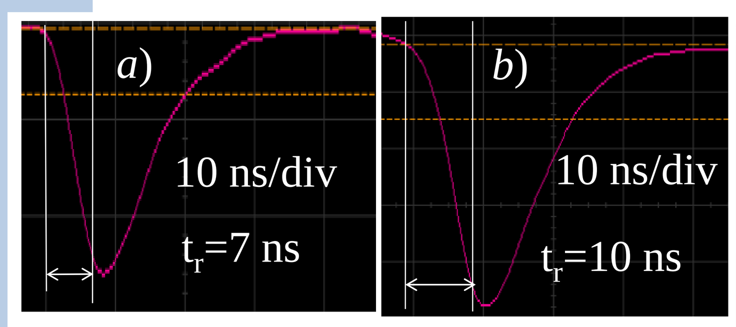


← Signals were inverted by amp. in these measurements:
1-st electrode *(blue)*
2-nd electrode *(green)*
3-rd electrode *(red)*

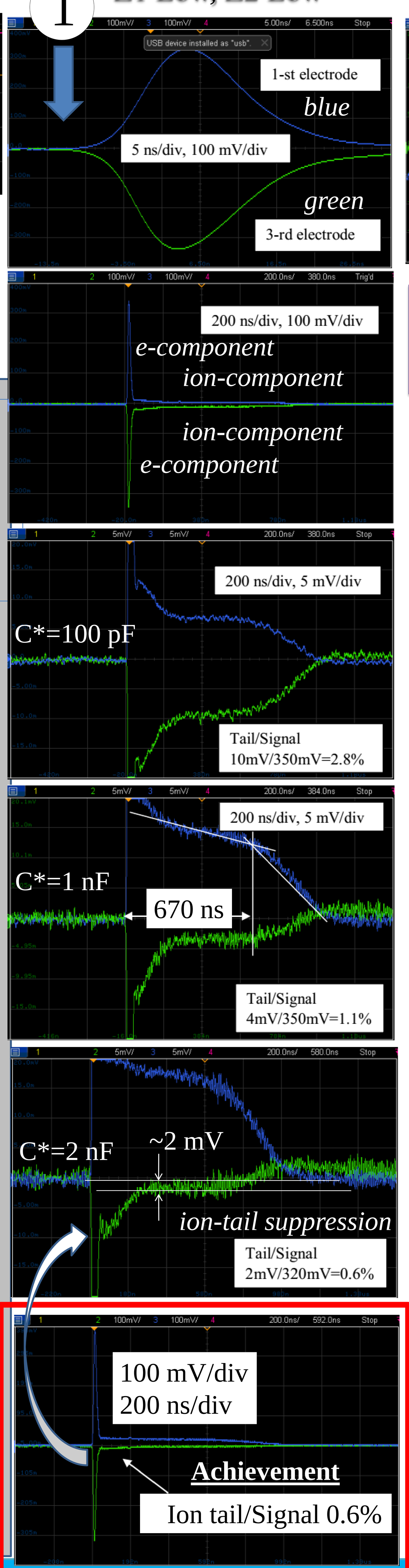


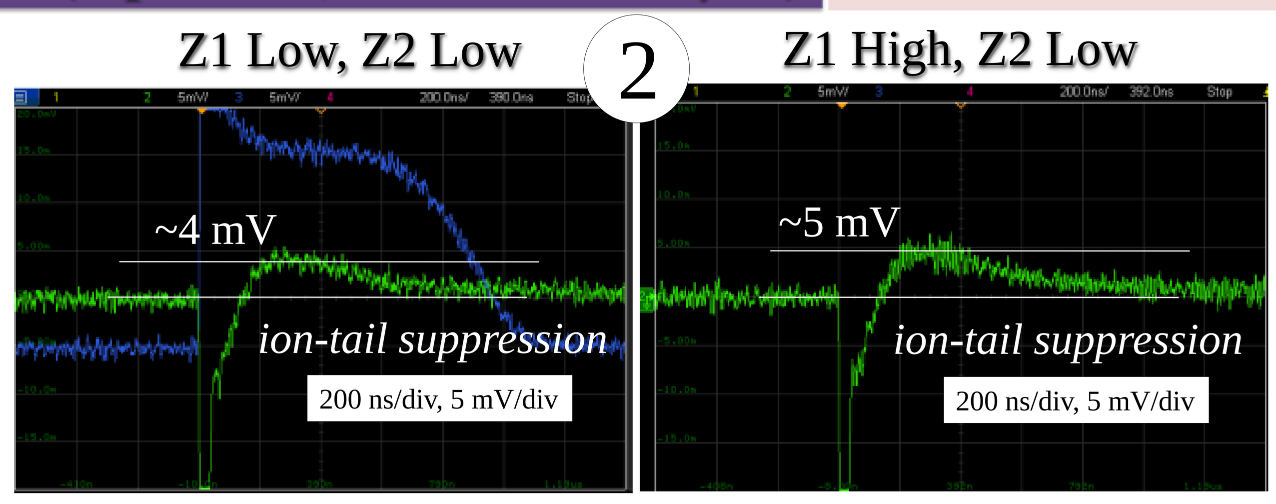
- Reconstruction of the signal in the input done using convolution **y(t)=x(t) * h(t),** where x(t) – input, h(t) – amp. impulse response *(red)*, y(t) – output *(blue)*, Y(t) - reconstruction *(green)*.
- Assuming that x(t) is composed of δ(t) (width 1 ns) and step-function (amplitude 1%) and assuming that T is the end of the input signal we obtain an agreement Y(t) and y(t) within ~10% *(green)*, *a)*.
- The rise time of Y(t) becomes too large *(green)*, if the δ(t) is missing on the input, *b)*.

Signals on electrodes with fast ASIC AST-1-2 (Tp=5 ns, K=100 mV/μA)



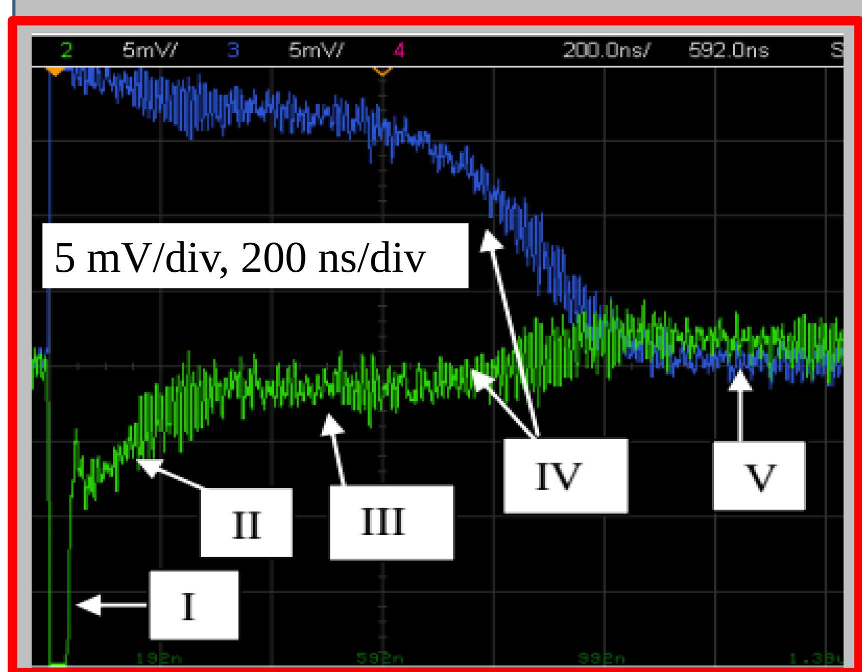
- h(t) – impulse response of the amp., rise time 7 ns (*a*); output signal (^{55}Fe), rise time 10 ns (*b*).
- Difference 3 ns gives the input pulse width.



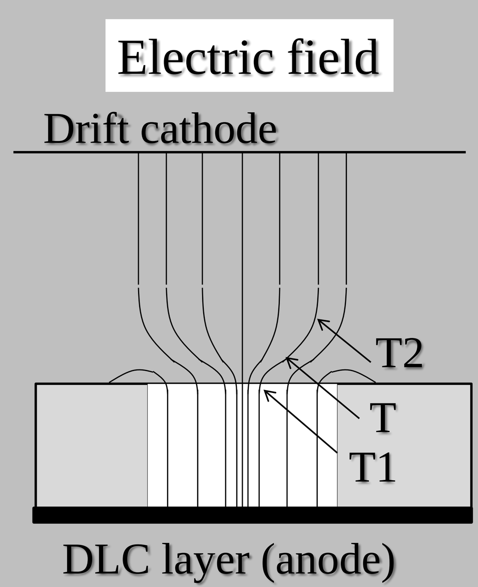


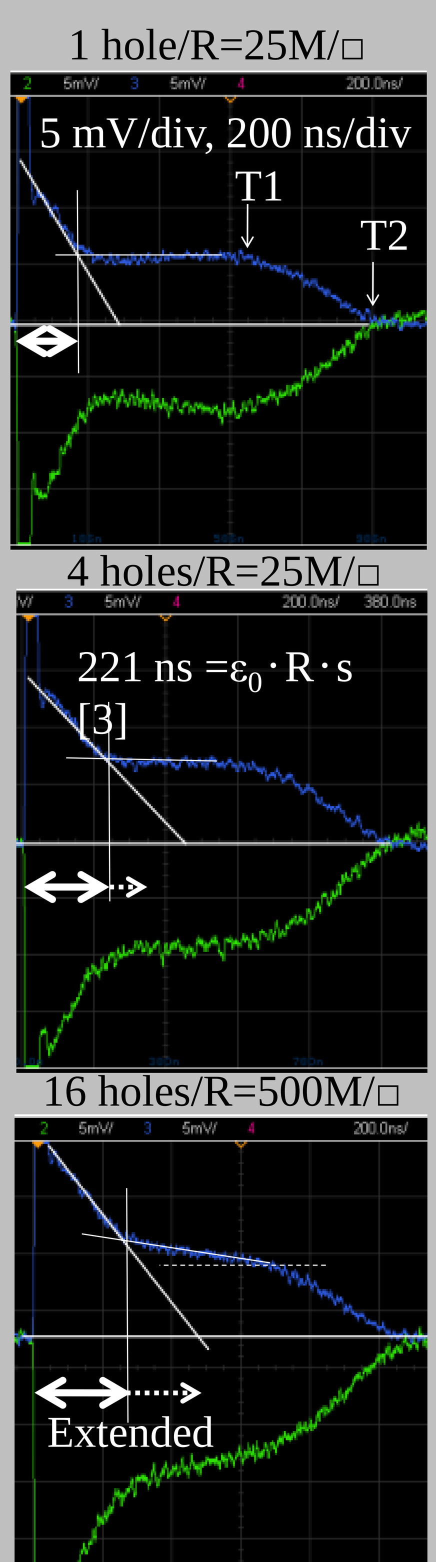
Five characteristic time intervals

- Below we show 5 characteristic time intervals which define the rate capability of the detector:



- A relative influence of the R and size of the mesh to the "bump" induced by electrons moving along the DLC layer (see interval II).
- Useful formulas one can find in ref. [3].





I. Avalanche electrons reach DLC induce the main signal (~30 ns in our case for Fe-55 with fast amplifier Tp=5 ns, the real signal is 10-times shorter);
II. Electrons move along the DLC layer adding some tail ("bump") to the signal induced by ions - about 200 ns in our case;
III. Ions drift along the hole at E~50 kV/cm and induce characteristic ion tail in the signal;
IV. Ions leave the hole (E reduced from 50 to 1 kV/cm);
V. Ions drift to the cathode at E~1 kV/cm.

Conclusion

- The Well (micro-Well *depending on thickness*) detector [1] is a new class of MPGD without induction gap in contrast to GEM [2].
- In many features and characteristics outperforms the GEM/THGEM.
- The Well detector with the DLC anode of thickness ~100 nm with the signal pulse width, as shown in this work, is able to withstand high particles fluxes up to 30 MHz/cm^2.

Possible application at LHCb M2R1 and M3R1 upgrade (project)

•The **LHCb (Large Hadron Collider beauty)** experiment is one of eight particle physics detector experiments collecting data at the Large Hadron Collider at CERN.

- Rates extrapolated to luminosity 2×10^{34} cm^{-2}s^{-1} in the inner-most regions of the LHCb muon detector (Run 4, Run 5):

✓ 3300 kHz/cm² in M2R1 chambers
✓ 1900 kHz/cm² in M3R1 chambers

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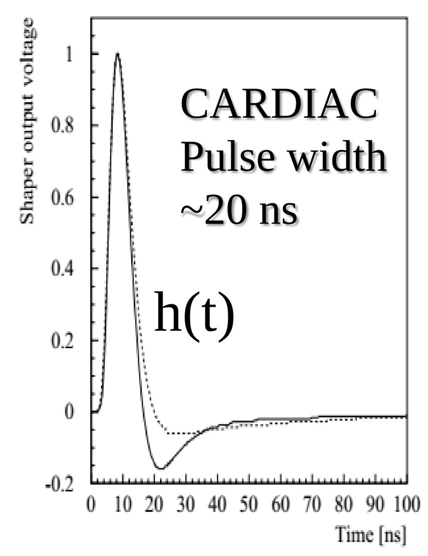
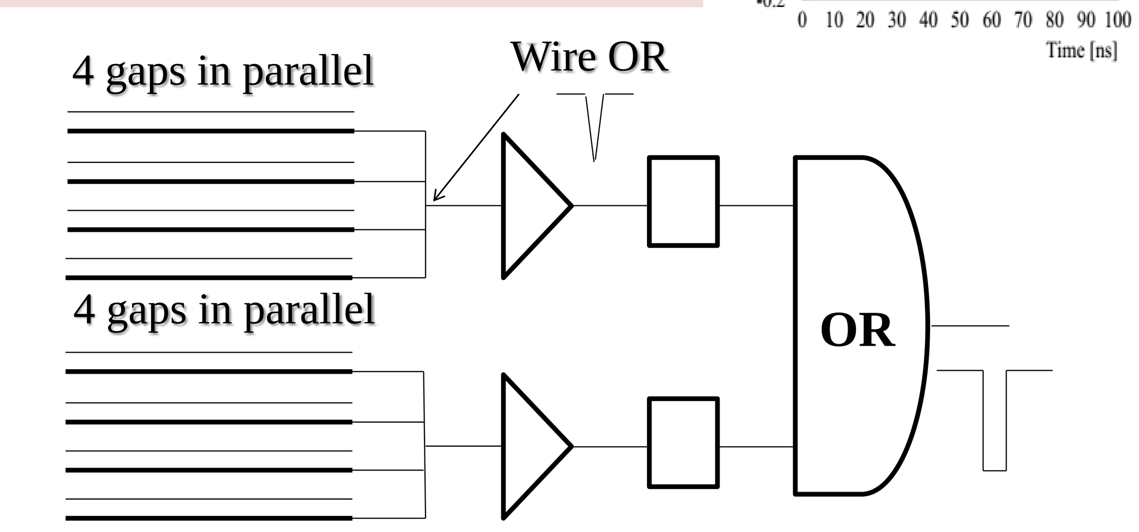
- In order to minimize efficiency losses at high particle fluxes due to the dead time we propose a solution for M2R1 and M3R1 based on the WELL Electron Multiplier with the DLC anode – a key element of the robust and fast 2D-position sensitive MPGD.

- 8-layer M2R1 or M3R1 chamber with narrow gaps (1 mm each).
- Architecture: two 4-layer chambers with digital signals combined by logical OR.
- Within each 4-layer chamber signals are combined by wire OR.
- As foreseen, the existing front-end electronics with Tp=10 ns (CARDIAC) has to be saved.





References
1. R.Bellazzini, et al. The WELL detector. NIM A423 (1999), 125-134.
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