



## Electronics Performance of the ATLAS New Small Wheel Micromegas wedges at CERN

Instrumentation for Colliding Beam Physics INSTR 2020 Novosibirsk, Russia

### Polyneikis Tzanis<sup>1,2</sup>, on behalf of ATLAS Muon Collaboration

1. National Technical University of Athens 2. Brookhaven National Laboratory

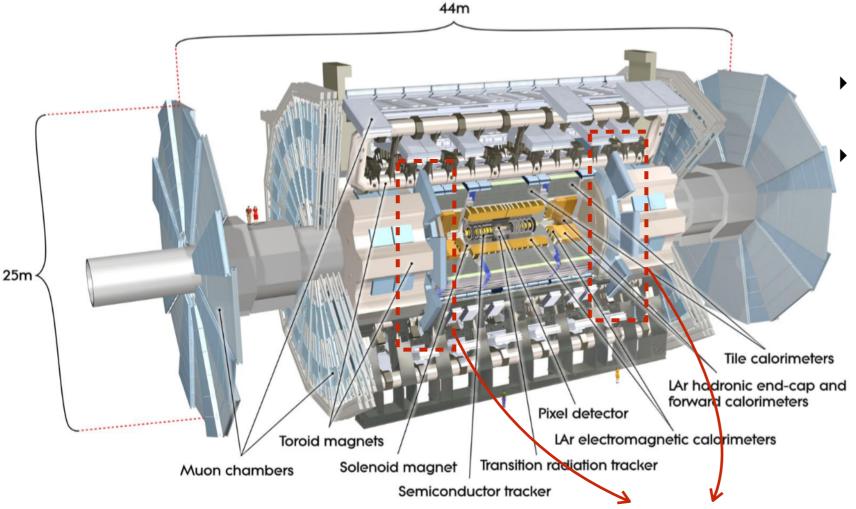


### Outline

- The ATLAS New Small Wheel (NSW)
  - The Micromegas detector
- ▶ The electronics of the Micromegas detectors
- Sector Integration
- Monitoring/Configuration path
- Data Acquisition path
- Test with cosmics rays
  - System Monitoring & Results
- Trigger path
- Summary



### **ATLAS**

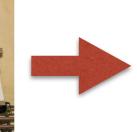


- ▶ Run 3 will have a factor of ~1.5x increase in instantaneous luminosity
- The High Luminosity Large Hadron Collider (2027-...) will have 2-4x larger peak instantaneous luminosity compared to LHC Run 3 (2021 2024)

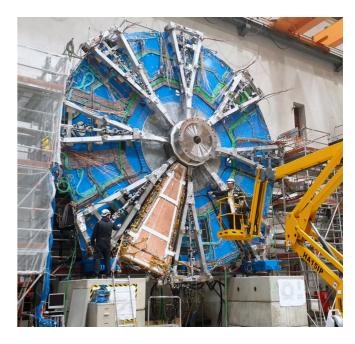
Small Wheel

- The New Small Wheel (NSW)
  upgrade will replace the current Small
  Wheel of the ATLAS muon spectrometer
  to handle larger particle rates
- Important for Run 3, vital for High Luminosity LHC (2028)





#### New Small Wheel

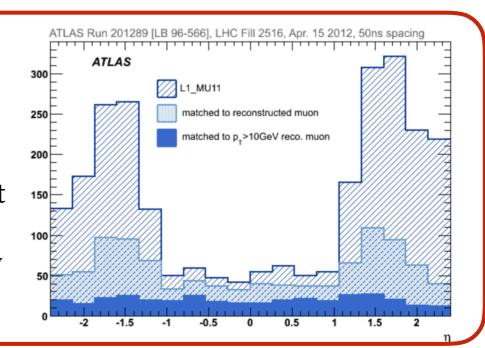


Small Wheels

### New Small Wheel Upgrade

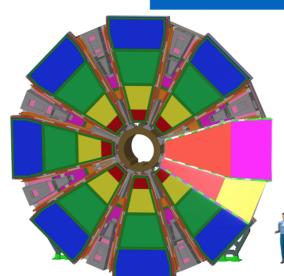
#### Present detectors

- Cathode Strip Chambers (CSC)
- Monitored Drift tubes (MDT)
- Thin Gap Chambers (TGC)
- Tracking: Monitored Drift Tubes will lose efficiency at high hit rates due to higher instantaneous luminosity
- Triggering: Lowest unprescaled muon trigger is dominated by triggers not originating from the interaction point



### New Small Wheels

sTGC MM chamber sTGC



The NSW will provide high precision muon track reconstruction and trigger information to ATLAS, at high rates, thus eliminating the issues of the present SW.

- 16 sectors for each NSW
- 16 layers for each sector

~2.4 million readout channels

#### The NSW detectors:

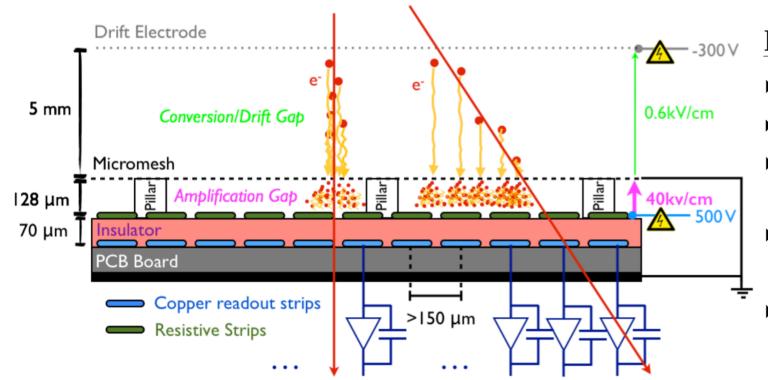
- Micromegas (MM), mainly for precision tracking, also for trigger
- small Thin Gap Chambers (sTGC), mainly for trigger, also for precision tracking



### Micromegas

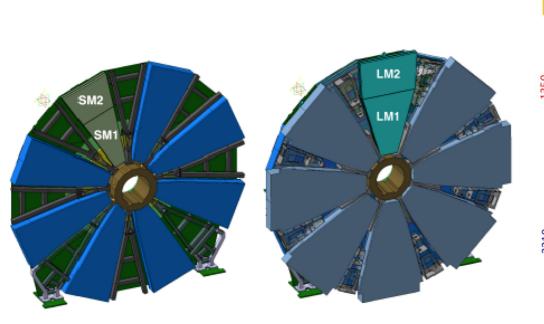
For more Micromegas: See I. Gnesi's talk

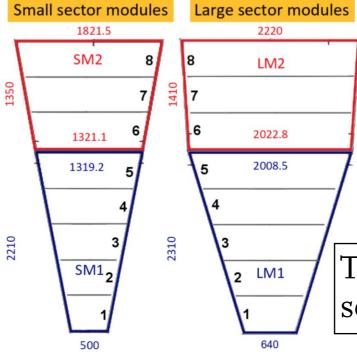
MicroMegas with Resistive Strips technology as a Precision Tracker



#### Main characteristics:

- ▶ Spatial resolution < 100µm</p>
- 0.4 mm readout granularity
- small strip pitch (better particle separation compared to current drift tubes)
- short drift time (~100 ns compared to ~750 ns for drift tubes)
- Resistive anode strips to suppress discharge influence on efficiency





LM1: France

LM2: Greece, Russia

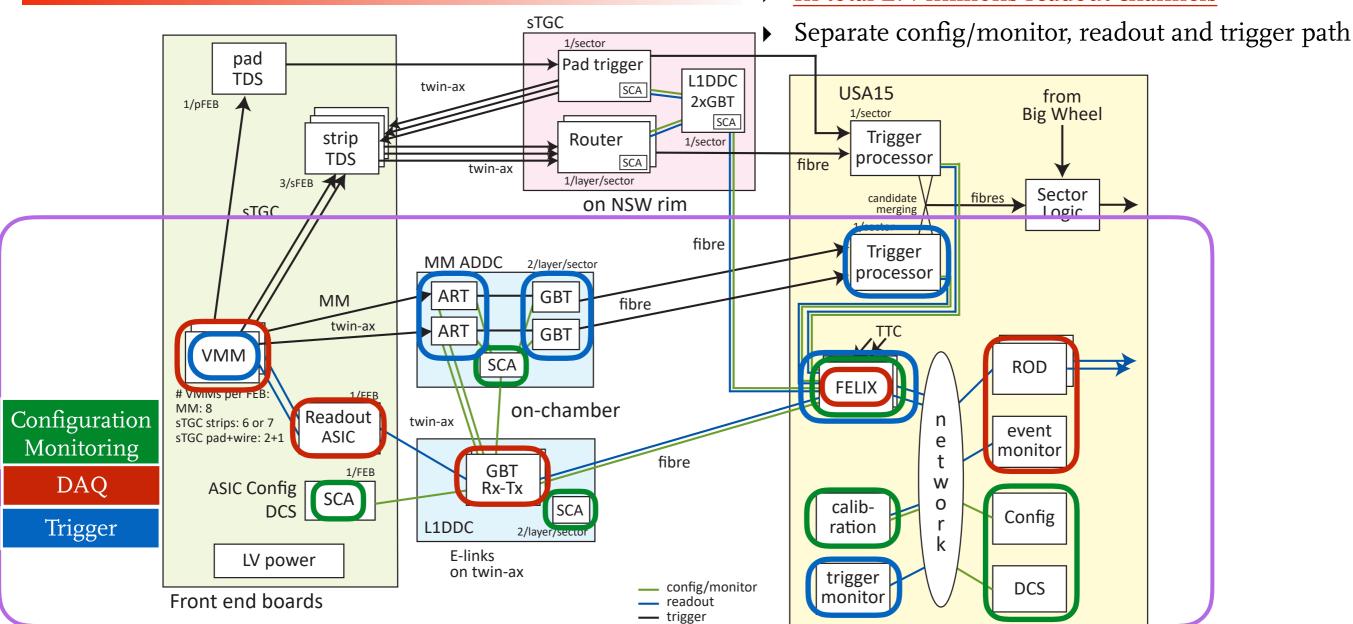
SMI: Italy

SM<sub>2</sub>: Germany

Totally 128 MM modules in 2x16 sectors, ≈3 m<sup>2</sup> active area each

### NSW Electronics Trigger & DAQ data flow

#### ▶ In total 2.4 millions readout channels



#### VMM [Readout]

- ▶ 130 nm CMOS technology
- 64 channels per chip
- → ~200 ns dead time per channel
- Timing resolution in the order of ns
- SEU protection

#### GBTx [Data Transceiver]

The GBTx is a radiation-hard ASIC, acting as a highspeed transceiver between the FEs and the back-end electronics (FELIX). Bandwidth of 4.8 Gb/s

### ART [Timestamp]

The ART ASIC on the ADDC deserializes the ART addresses from several VMMs, appends a 5-bit VMM geographical address and a timestamp. It then forms and forwards a data packet to the MM Trigger Processor through optical fiber.

### FEAST [Power]

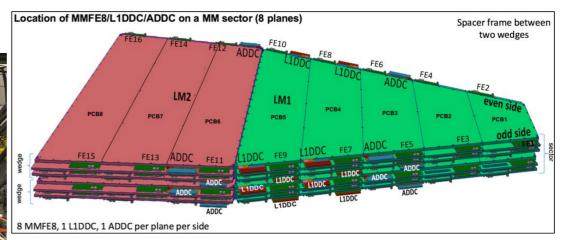
FEAST is a Radiation tolerant 10W Synchronous Step-Down Buck DC/DC converter developed to provide an efficient solution for the distribution of power.





### **NSW MM Electronics**





#### Each MM sector combines:

- 128\* MMFE8 [Front-End]
- 16\* ADDC [Trigger]
- 16\* LIDDC [ Data-Driver]
- 16\* LVDB [Power]

### Micromegas Front-End 8



Houses the 8\*VMM chips that convert analog signal of the detector into digital, which includes the ART data.

#### Art Data Driver Card

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Collect ART data from eight MMFE8s and relay it to the Trigger Processor.

#### Li Data Driver Card



Interface of the MMFE8s and ADDCs to FELIX, passing along configuration data and clock source.

#### Low Voltage Distributor



Provides low voltage power to MMFE8, L1DDC and ADDC

• A lot of people are involved in several stations in parallel

A lot of care and work in order to prepare the MM sector





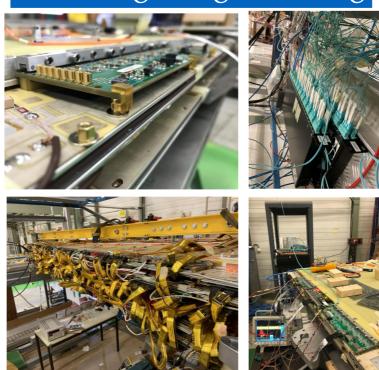
### Sector Eltx integration at CERN

### Board & detector preparation, cable testing



- ▶ Installation of FEB standoffs (chambers)
- ▶ Grounding interconnections (chambers)
- ▶ Cooling pads (chambers & FEBs)
- ▶ Zebra holders (FEBs)
- Cable integrity testing (twinax & fibers)

ready for the cosmics ray stand



- ▶ Installation of FEBs & cabling
- ▶ Small scale readout tests to validate board connectivity and noise

### Sector readout tests



- ▶ Connectivity Validation
- ▶ Eltx cooling validation
- ▶ Configuration & readout of the full Micromegas sector
- ▶ Full scale tests for validation
  - Internal VMM pulsing
  - HV pulsing
  - Cosmics

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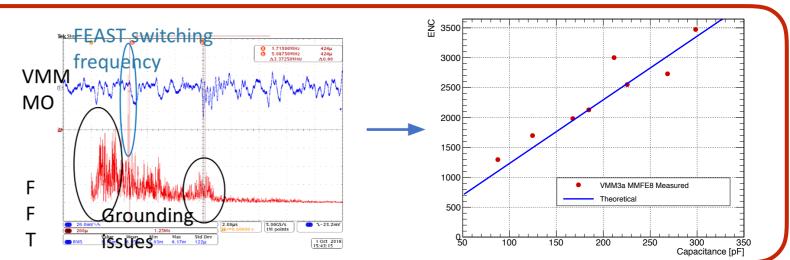


## Integration Highlights

Although the detectors and electronics arrive tested they are put together as a system for the first time @CERN

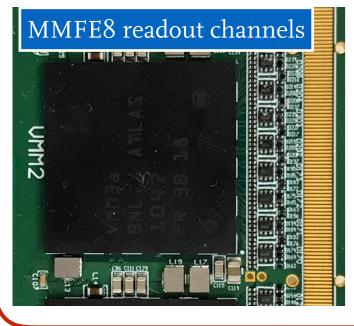
#### Noise investigation

- ▶ Excessive noise has been found mostly due the FEAST on the boards
- ▶ Noise has been brought down to theoretical expectations by improving the FEAST shielding and the grounding of the system

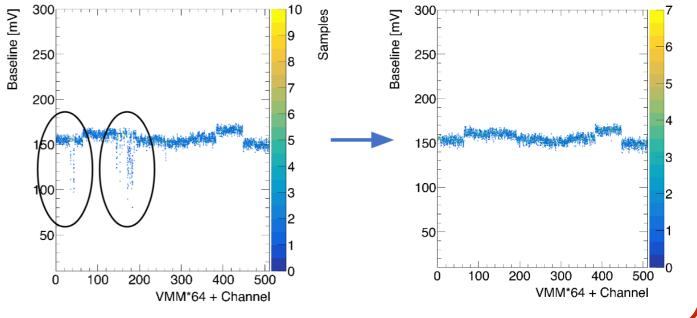


#### Readout Strips connection

- Electronics readout channels connected to detector readout strips using a rubber zebra adapter
- 1st in experimental high energy physics where a connector is not used
- Several cases of bad connectivity between MMFE8 channels and strips
- Understood to be coming from some misaligned/bent precision pins in these first MM modules
- Fabrication of custom boards to identify channels in sort and alignment issues







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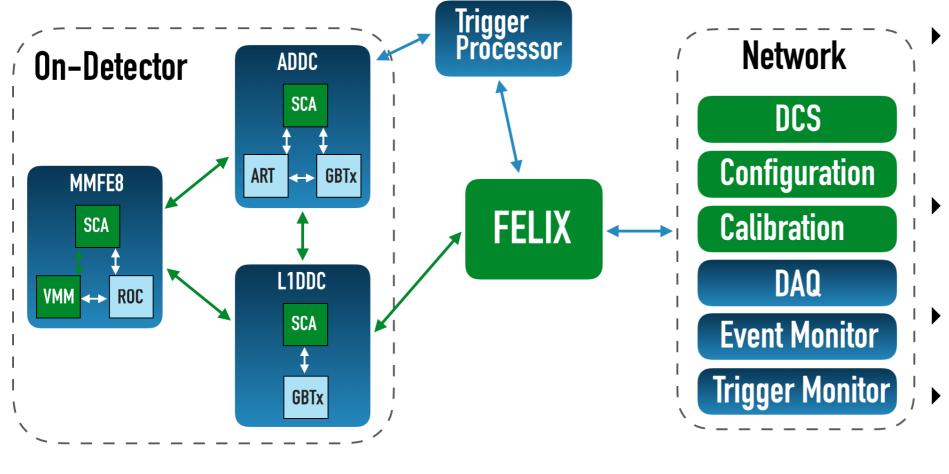


### Monitoring/Configuration path

The GBT-SCA ASIC (Giga-Bit Transceiver - Slow Control Adapter) is the part of the GBT chipset which purpose is to distribute control and monitoring signals to the front-end electronics embedded in the detectors. The user interface ports are: 1 SPI master, 16 independent I2C masters, 1 JTAG master, 4 DAC (8-bit), 32 GPIO and 31 ADC (12-bit)

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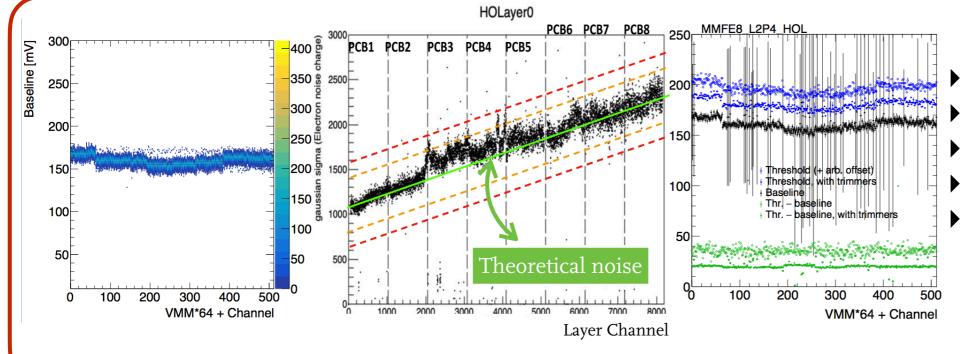
- Perform front end monitoring using the SCA to read Feast PW/temperature, board(NTC), VMM and SCA temperature
- Configuration of VMM, ART, ROC and GBTx chips via I2C and SPI
- ▶ ADC channel is used for the the VMM calibration
  - In total, 5120 SCAs for MMG 100k parameters (voltages, temperatures, GPIOs)





### Monitor (DCS)

- ▶ Front-end monitoring using SCA OPC UA Server to read temperatures ,voltage levels and connection status ~2700 parameters per MM sector
- ▶ Connectivity validation
- Cooling validation using the monitored temperatures
- ▶ Voltage Validation

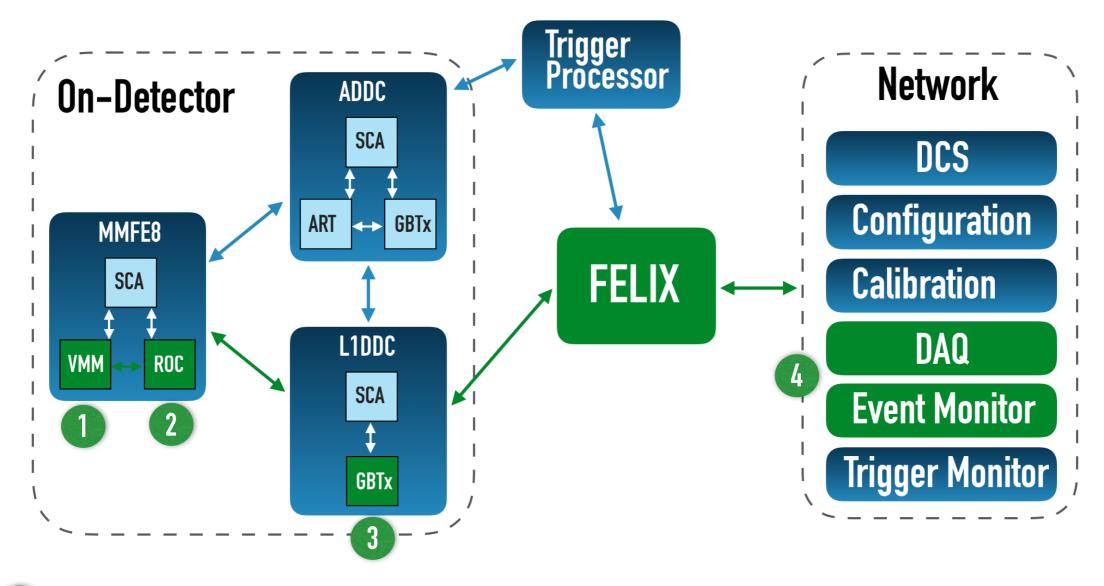


#### Noise & Calibration

- Connectivity to readout strips
- ▶ Baseline/Noise measurements
- ▶ Channels trimmers calibration
- ▶ Channels threshold calibration
- ▶ Map of noise per channel for each layer shows nice linear dependence on the strip capacitance close to theoretical values



### DAQ path



- 1) VMM: digitizes detector signals and send trigger primitives (64 channels)
- ROC: buffers and filters data from 8 VMMs to match ATLAS trigger selection
- GBTx: packs up readout data and sends to FELIX
- 4 DAQ and event monitor





### **Cosmics Tests**



- ▶ The validation of the full MM double wedge requires the readout of 128x MMFE8 (65k channels), 16x L1DDC, 16x ADDC
- ▶ Not at all a small-scale system, readout of ~100 optical links
- ▶ FELIX and DAQ system are also new developments for Phase-I so we are keep learning/debugging/testing these as well

- ▶ The final step in the electronics integration/testing workflow
- ▶ MM sector validation
- ▶ Scintillator trigger(~100Hz) with full coverage along the precision coordinate covering partially the detectors
- Not meant for detailed performance but to validate that the system (detector+electronics) works
- ▶ Nominal HV settings (+570V strips and -300V drift ) and Ar:CO2 gas
- ▶ Look at the basic detector parameters
  - ▶ Charge
  - ▶ Cluster Size
  - ▶ Efficiency distribution
  - ▶ Tracking
- ▶ System test (chamber+electronics) but can be used to spot electronics issues

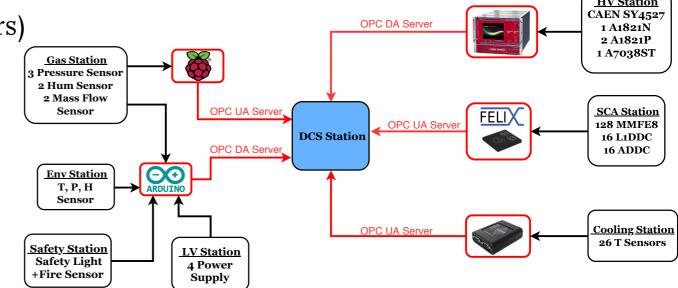


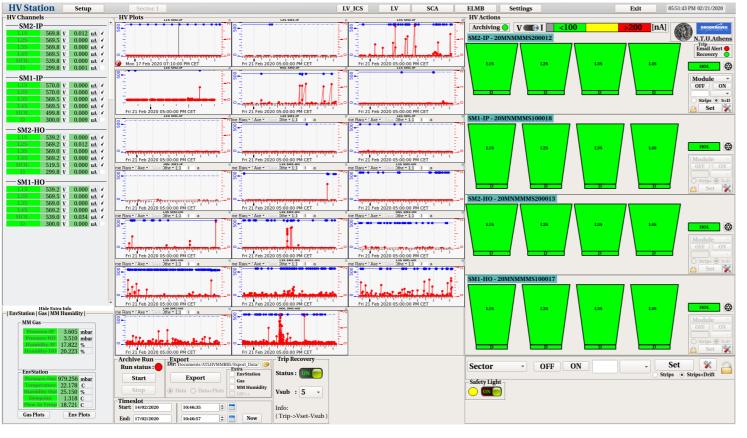
### **Cosmics Control Station**

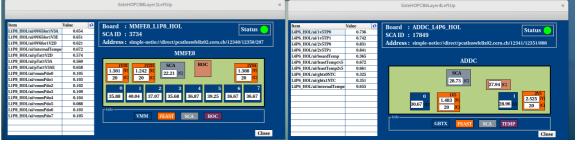
A control station has been developed for the operation of the MM sector & electronics during cosmics run.

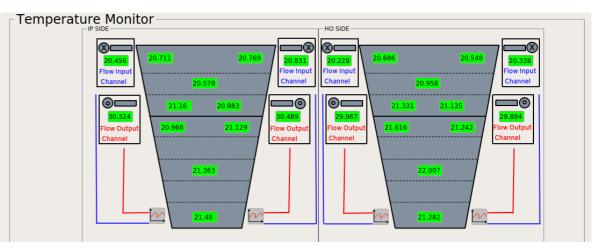
MM operation (HV, gas, humidity, env parameters)

- Electronics (connectivity, temperature)
- Low voltage
- Cooling







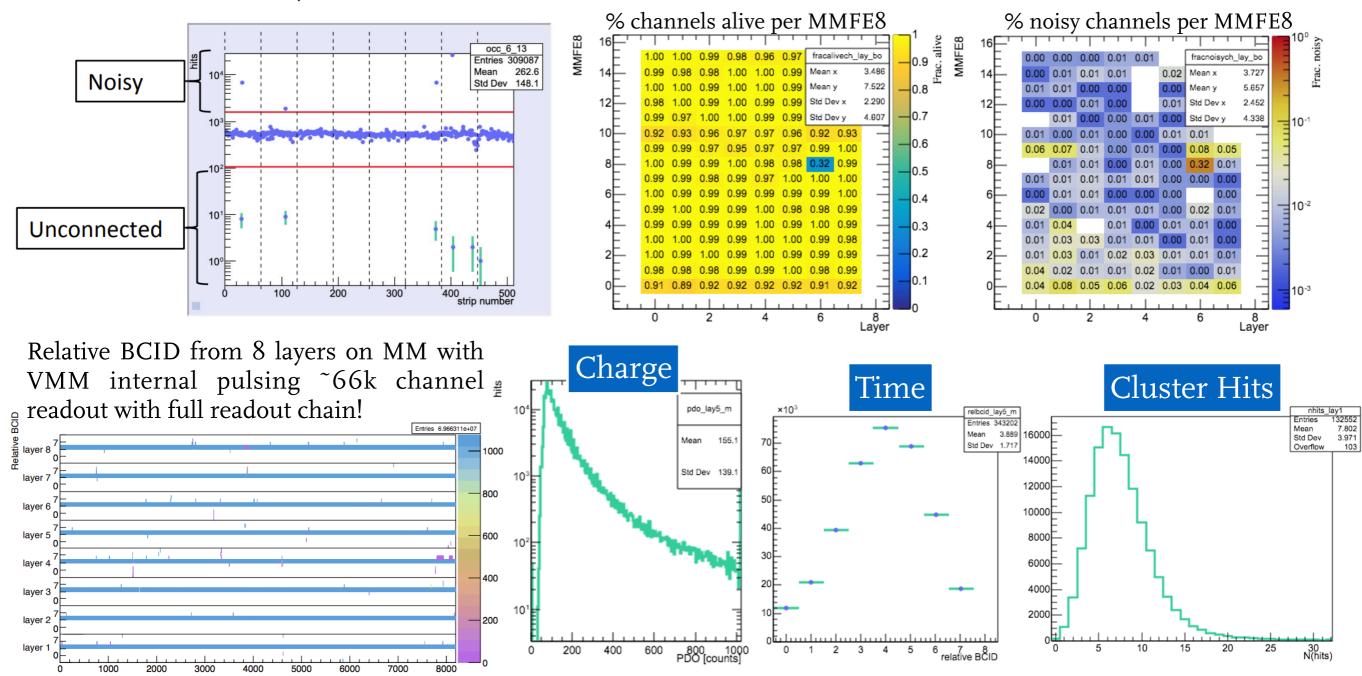




### **Cosmics Tests**

Noisy channels are equally important (should be masked thus dead)

- Can be determined from cosmics/noise run (L1 readout) and/or from baseline measurements (SCA)
- Boards with noisy channels > 5% are checked and replaced
- Produce lists of noisy channels



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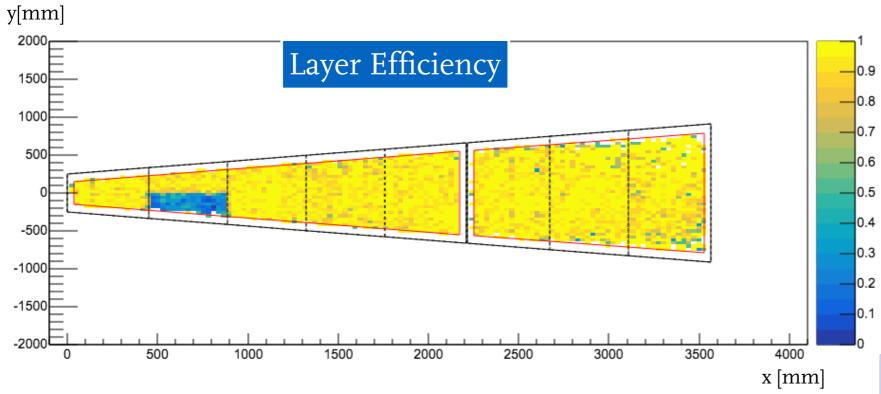
## Tracking Efficiency

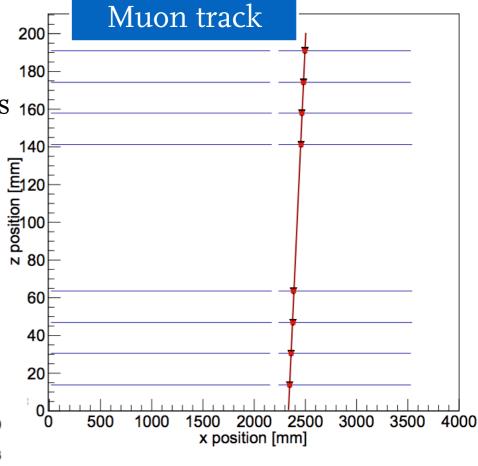
• Measured efficiency is mostly defined by the chamber parameters  $_{160}$  (HV, gas etc.) but can also be used for validating the electronics  $_{140}$  complementary to the other tests

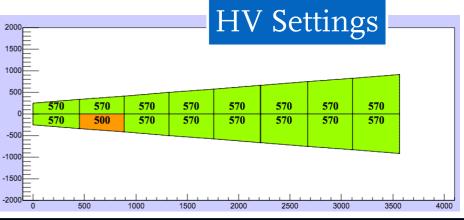
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• Get theoretically expected efficiency based on the HV value and compare to measured

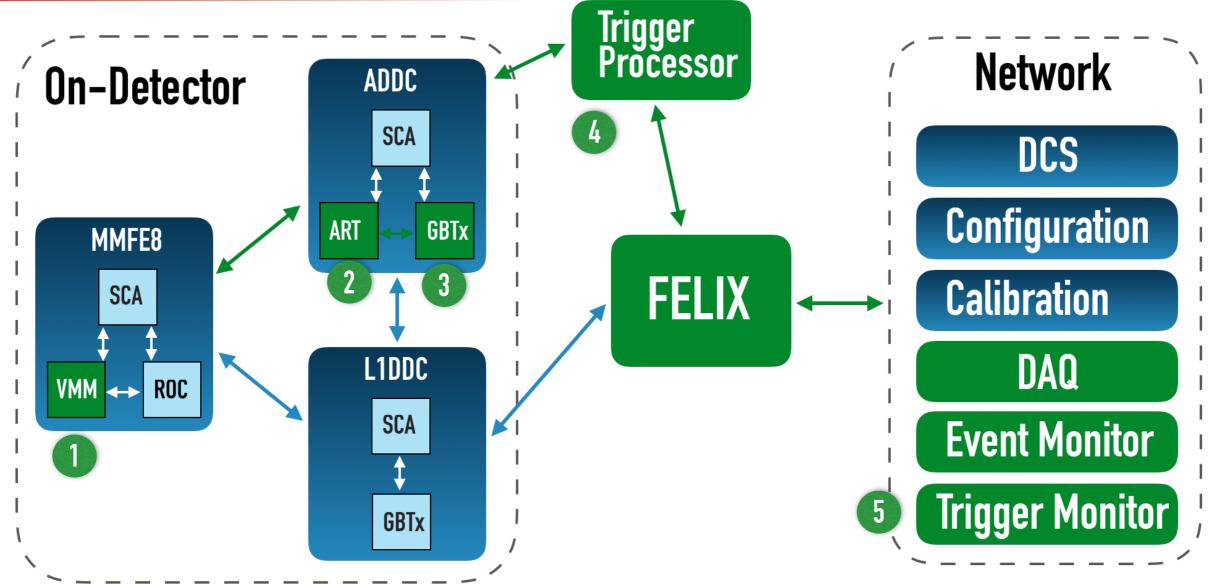
• Large discrepancy could point to electronics issues







### Trigger path



- 1 VMM: digitizes detector signals and send trigger primitives (64 channels)
- 2 ART: packages trigger primitives from 32 VMMs and stamps with bunch crossing ID
- GBTx: packs up trigger data and sends to Trigger Processor
- TP: makes a candidate "track" from trigger primitives
- Trigger and event monitor

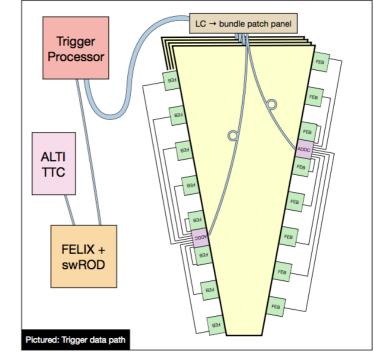


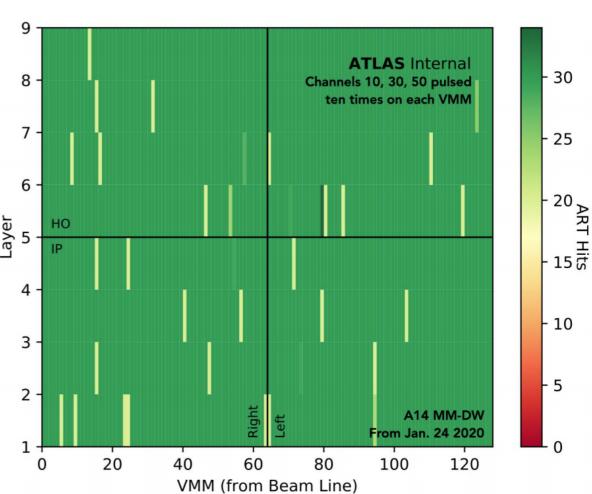


### Trigger tests

Test objective: confirm electrical and optical connectivity by sending test pulses to all VMMs of a double wedge and reading out the ART data from the trigger processor.

- ▶ Trigger data begins with ART hit, essentially the earliest strip of a MM cluster
- ▶ Trigger processor makes "every" BC decide if incoming ART hit make trigger
- Automated ART test run of a DW where all VMM channels are pulsed sequentially and produce a map of the ARTs that are readout out on the TP. 10 pulses sent to 3 different channels on each VMM. If we had perfect performance, then each bin content would be 30.
- ▶ No bins with o content -> sign-off on electrical and optical connectivity throughout chamber
- ▶ Sensitive on dead channels; need to input a dead channel list determined from the SCA/LI readout to be masked
- ▶ Produce a list of the ART-dead channels

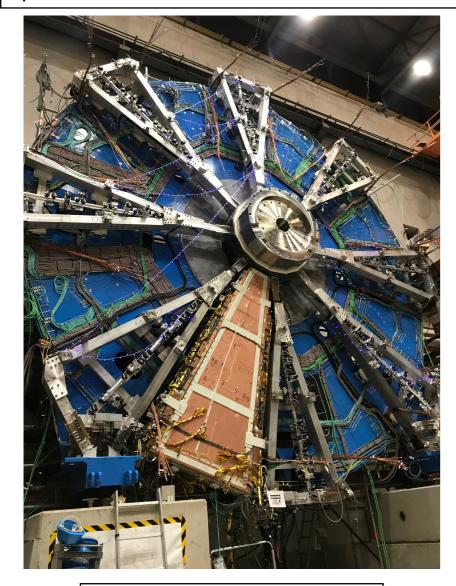






### Summary

NSW Side A @191 1/16, more to come next weeks



Installation in time!

- NSW is a fully redundant trigger and tracking detector system, adequately supported by an advanced electronics scheme and ready to handle the challenges of increased instantaneous luminosity at the High Luminosity LHC
- ▶ Electronics performance in really good shape:
  - Monitoring of all boards though full readout chain
  - Readout and trigger efficiency>90%
  - ▶ Cosmics ray stand test -> Spatial resolution of 100µm
  - Noise and misalignment problems are well defined and solved
- Right now is an exciting time! Integration ongoing with final chambers and electronics
- NSW Side A under progress and aim for the installation at ATLAS cavern until October 2020
- Thanks for all construction, mechanical, integration, electronics teams for this achievement!

## Thanks for your attention!



## Back Up





# 

#### Each MM sector combines:

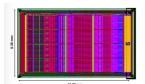
- 128\* MMFE8 [Front-End]
- 16\* LIDDC [ Data-Driver]
- 16\* ADDC [Trigger]
- 16\* LVDB [Power]

#### Micromegas Front-End 8



Houses the VMM chips that convert analog signal of the detector into digital, which includes the ART data.





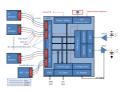
- 130 nm CMOS technology
- ▶ 64 channels per chip
- → ~200 ns dead time per channel
- Timing resolution in the order of ns
- SEU protection

#### Li Data Driver Card



Interface of the MMFE8s and ADDCs to FELIX, passing along configuration data and clock source.





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#### Art Data Driver Card



Collect ART data from eight MMFE8s and relay it to the Trigger Processor.





The ART ASIC on the ADDC deserializes the ART addresses from several VMMs, appends a 5-bit VMM geographical address and a BCID timestamp. It then forms and forwards a data packet to the MM Trigger Processor through optical fiber.

#### Low Voltage Distributor



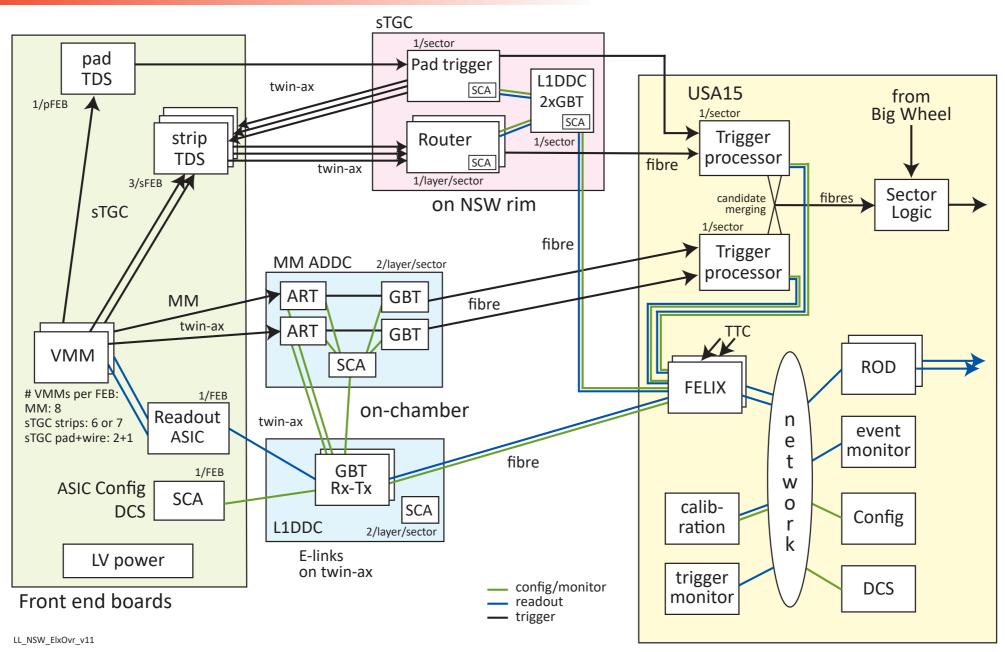
Provides low voltage power to MMFE8, L1DDC and ADDC





FEAST is a Radiation tolerant 10W Synchronous Step-Down Buck DC/DC converter developed to provide an efficient solution for the distribution of power.

### NSW Electronics Trigger & DAQ data flow



- In total 2.4 millions readout channels
- ▶ Separate config/monitor, readout and trigger path
- ▶ 5632 on-detector readout ASICs read out by E-links to GBTx ASICs
- ▶ 1024 on-detector trigger encoders configured by 512 GBT-SCAs
- ▶ All of the above configured and monitored by ~ 6400 GBT-SCA ASICs

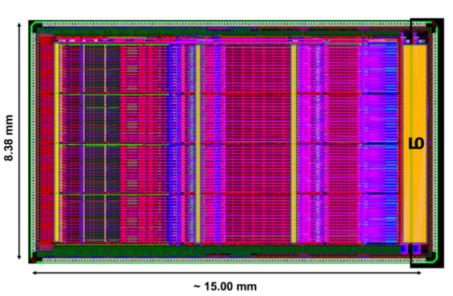
#### E-links used for:

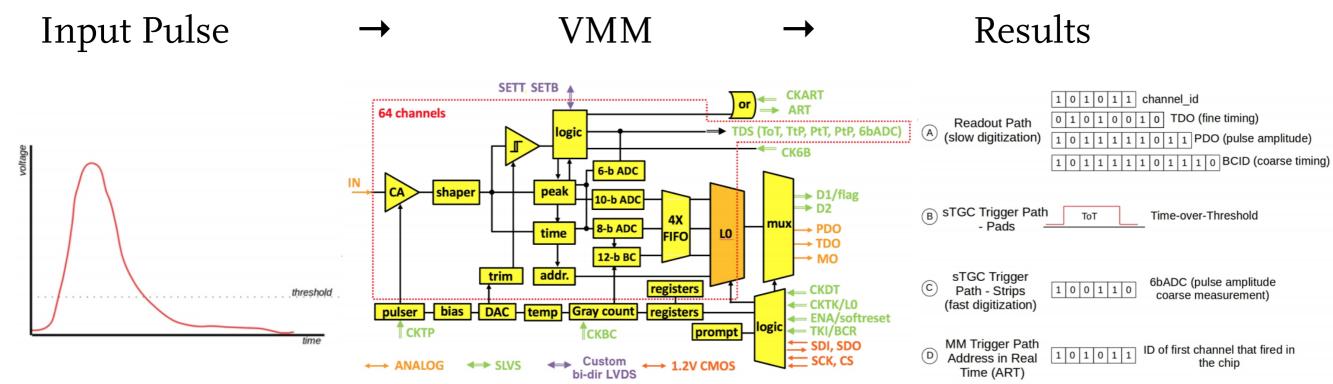
- Li Accept data + Data monitoring
- ▶ BC clock and TTC signals
- ▶ Configuration of ASICs
- Monitoring temperatures and voltages
- ▶ FPGA configuration

### VMM ASIC

- Will be used to readout both sTGC and MM
- Encodes pulse timing info in an 8-bit word (TDO), and pulse height in a 10-bit word (PDO)
- Timestamps the event with the BCID
- Provides trigger primitives from both sTGC and MM

#### 6 million transistors!









### **FELIX**



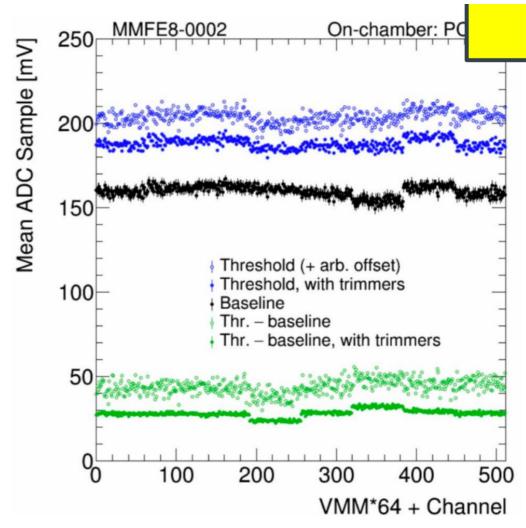
FELIX's FPGA is connected to the PC motherboard by PCIe from which the DAQ and the SC data flow. FELIX also receives TTC commands/clocking and distributes them to the FEs via the GBTx

PC's memory temporarily stores DAQ and SC data and sends/receives these data through the PCIe to the FELIX FPGA. The FELIX PC is connected to a highspeed network for routing the data further upstream

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### **Calibration - Trimmers**

- т. Measure baseline
- 2. Calculate a guessed threshold from baseline and baseline RMS: threshold  $(mV) = RMS \times N + baseline$
- 3. Calculate median effective threshold:
- Threshold eff = threshold baseline (Save value for all channels)
- 4. Adjust trimmers so that all channels achieve the median effective threshold calculated in 3; flatten out effective thresholds





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