LMU LUDWIG-MAXIMILIANS-UNIVERSITÄT MÜNCHEN

Upgrade of the Muon Drift Tube (MDT) electronics for the ATLAS Phase-II upgrade

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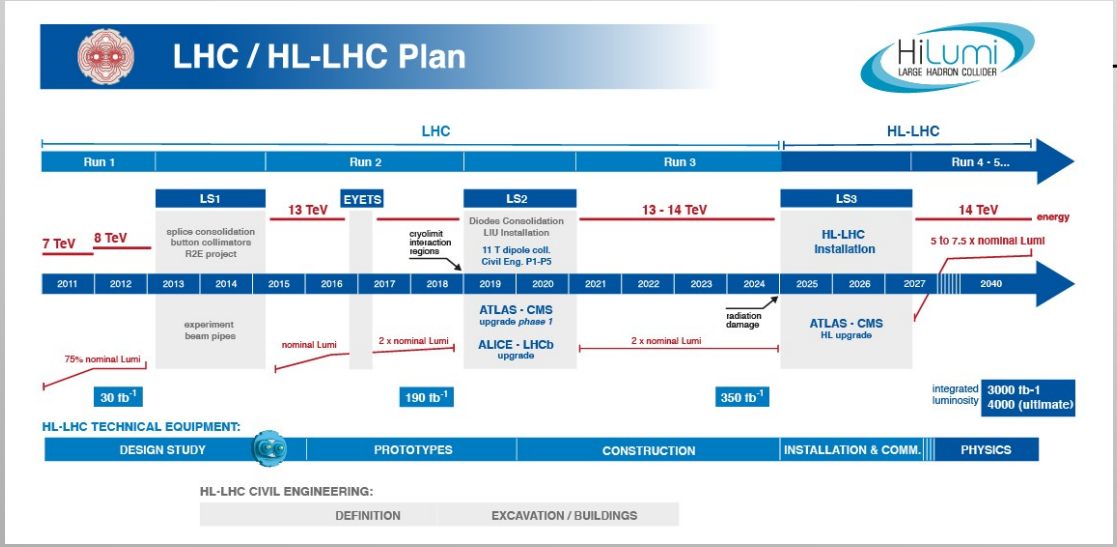
on behalf of the ATLAS Muon Collaboration

ATLAS Phase-II Upgrade

- The upgrades of the ATLAS experiment are in lock-step agreement with the upgrades to the LHC accelerator
- ATLAS Phase-II Upgrade is planned for 2025



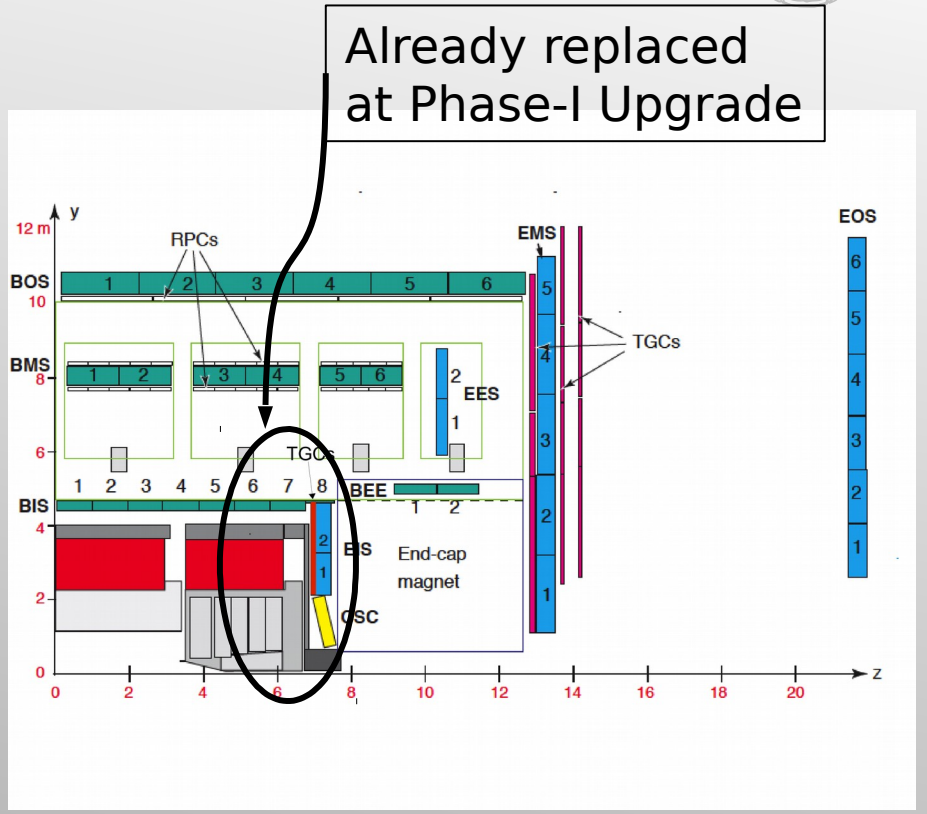
HL-LHC plan

Insta. luminocity $7.5 \times 10^{34} cm^2 s^{-1}$

Integ. luminocity $3000 fb^{-1}$ / 10y

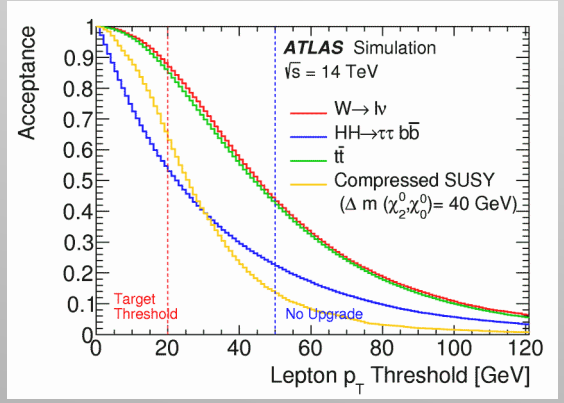
The evolution of the Muon Spectrometer

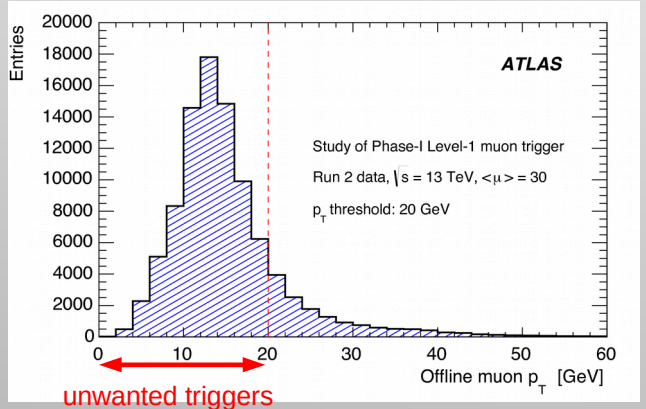
- Stand-alone measurements of muon momentum with a resolution of ~10% @ 1TeV (~60um)
- Phase-0: discrete roles for tracking and trigger detectors (MDT,CSC / RPC, TGC)
- Phase-I: Forward region detectors able to both track & trigger (micromegas, sTGC)
- Phase-II: MDT detectors are also used as trigger device at first level trigger



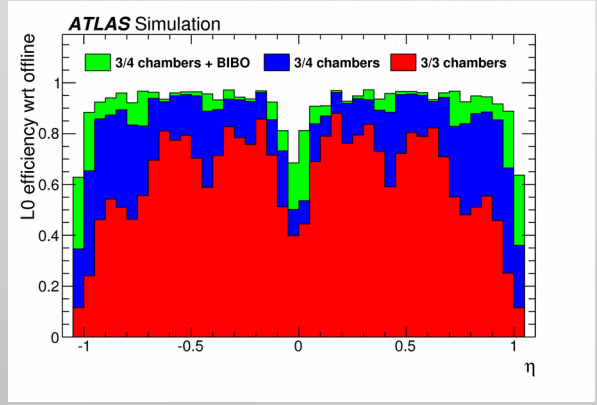
The physics challenges of Muon spectrometer for Phase-II

- Without upgrade, the muon trigger thresholds will have to be raised
- The muon trigger accepts muons with lower than nominal trigger momentum
- We will not even trigger on all the interested muons at Phase-II with the current trigger system





use MDT in at first trigger level



add RPC chambers

The engineering challenges of MDT upgrade for Phase-II

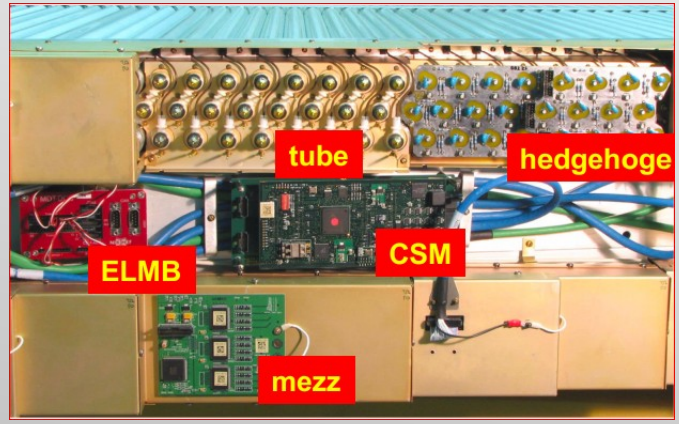
- Since this upgrade has to fit together with the rest of the ATLAS Phase-II upgrades inside the global LHC schedule, it has to be done in situ.
  - The number of electronic cards that has to be upgraded is ~15k mezzanine boards + ~1.5k CSM boards

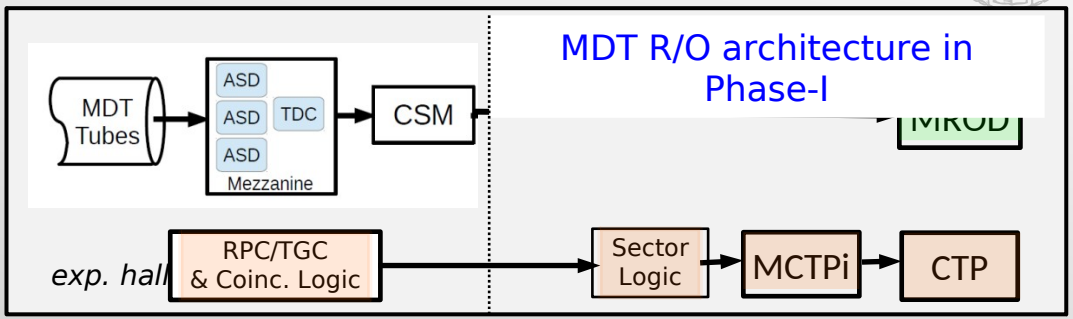
- Expanding the coverage of the muon spectrometer, essentially closes any available physical hole in the spectrometer.Which makes it a challenge to remove the heat produced by the Muon front-end electronics
  - Phase-II electronics try to keep the same heat budget as the original electronics

The solution to the challenges

- Improve the coverage of the muon spectrometer
  - Not part of this talk
- Update the trigger strategy by integrating the precision tracking chambers to the trigger decision
  - Partially part of this talk
- Upgrade the front-end electronics, as they are dependent on the trigger scheme
  - The main part of this talk

Current MDT electronics





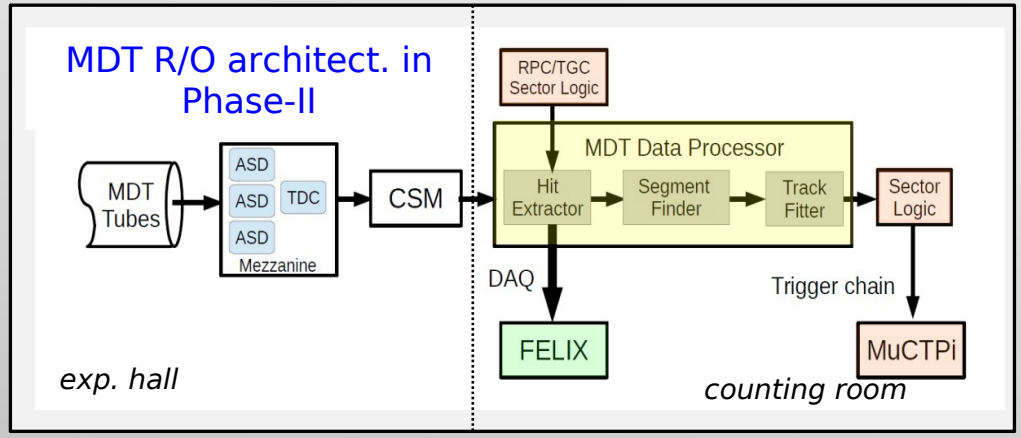
Seperate paths for tracking and triggering

24 Drift Tubes are connected to a hedgehog board to decouple the high voltage

3 8-channel Amplifier – Shaper – Discriminator chips and 1 ATLAS – Muon – TDC exist in each mezzanine card

1 Chamber – Service – Module is collecting the data of up to 18 mezz cards and transmits it to the backend

MDT electronics at Phase-II



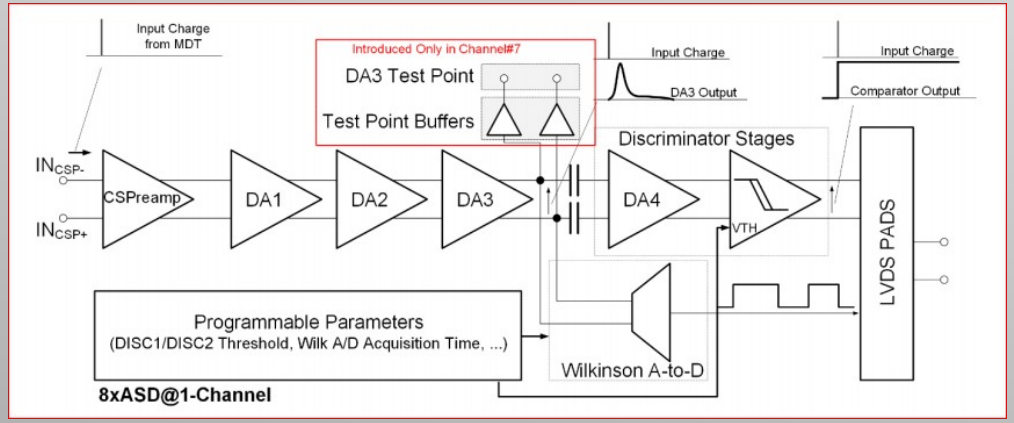
Phase-II MDT data are used to sharpen the trigger decision w.r.t. the muon p_T

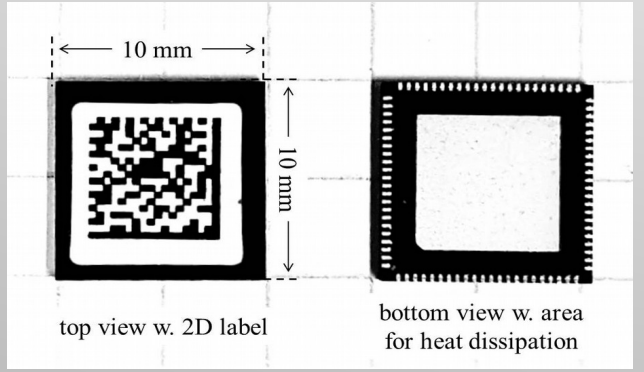
The project to merge the tracking information in the barrel region with the trigger information goes under the name L0MDT and is the other large upgrade project of the Phase-II Muon Spectrometer

ASD upgrade, design

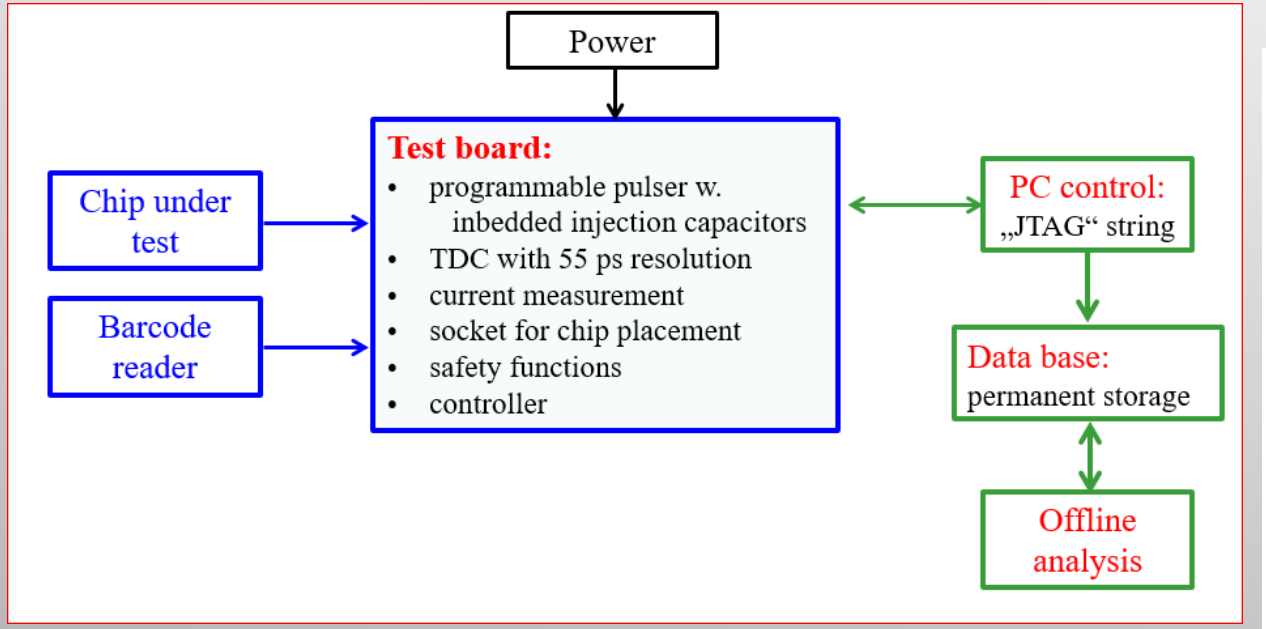
The new ASD chip is a direct evolution of the original ASD chip. Build on the GF 130nm platform. Ability to estimate the charge of the signal. Improvements mainly due to the better technology .

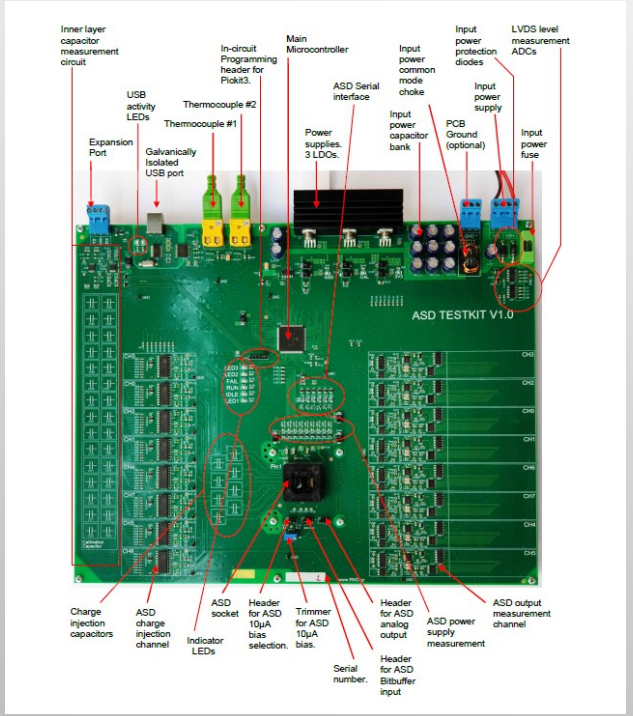
Packaged as an QFN88 with 0.4mm pad pitch





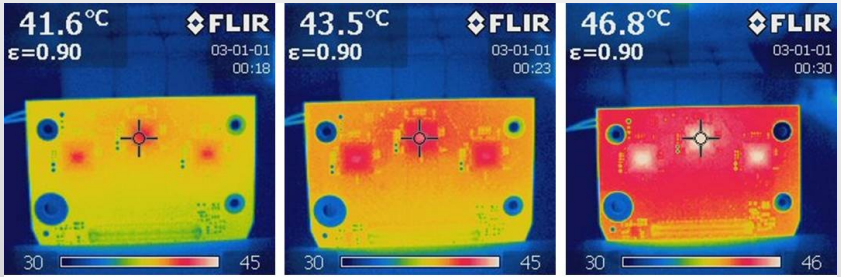
ASD upgrade, tester



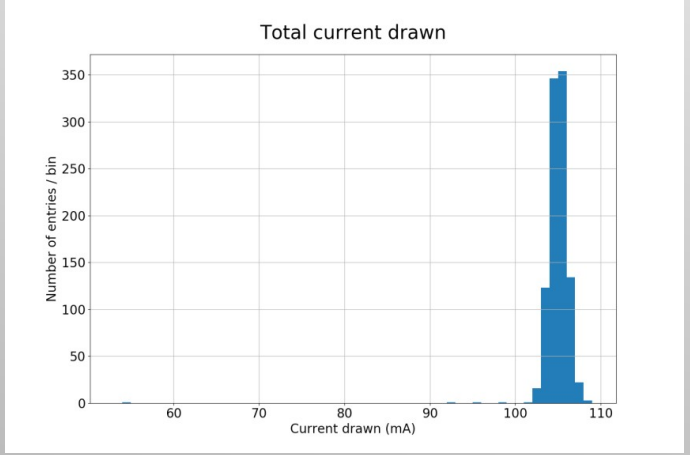


ASD upgrade results

- JTAG read/write cycles
- Power consumption
  - 102+-2mA , 996/1000 ok
  - 92-99mA , 3/1000, functional
  - 55mA , 1/1000 , dead
- Thermal behavior
  - <50°C , including the heat dissipated to the pcb
    Long term reliable operation is expected
    (spec <120°C)



2.7 V 3.0 V 3.3 V

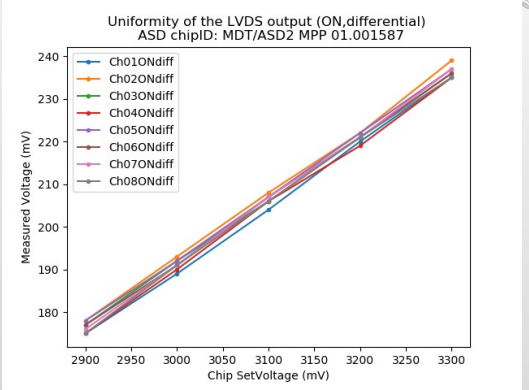


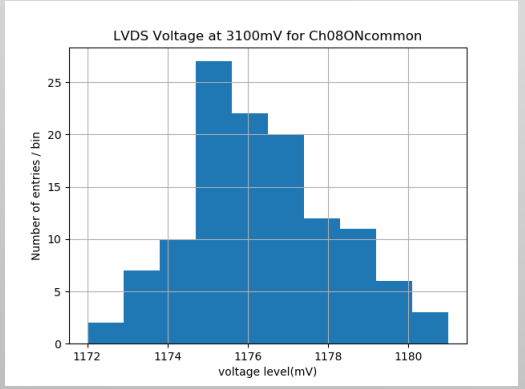
ASD upgrade , test

Check LVDS levels:

- both common and differential modes
- uniformity between channels in the chip
- uniformity between chips
- operating point dependence

No issues found



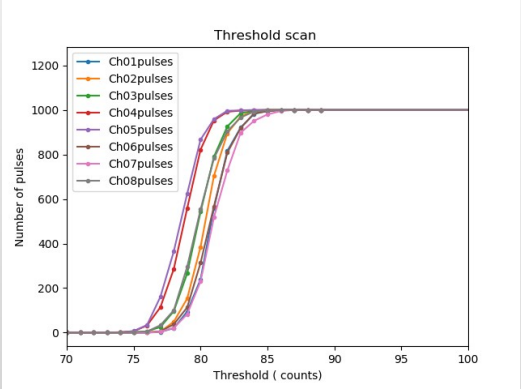


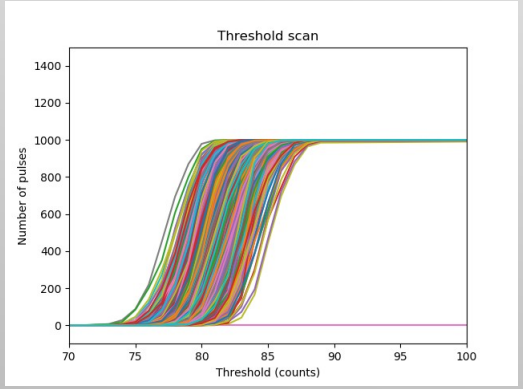
ASD upgrade , test

Threshold scans:
- on a sample of 100 chips
- using 10fC as input charge, 1k pulses per channel
- 2mV/count per chip design

Original chip requirements for ATLAS:
- 16mV channel variation on the same chip

Current chip performance:
- <5mV channel to channel variation
- 16mV variation includes all the chips

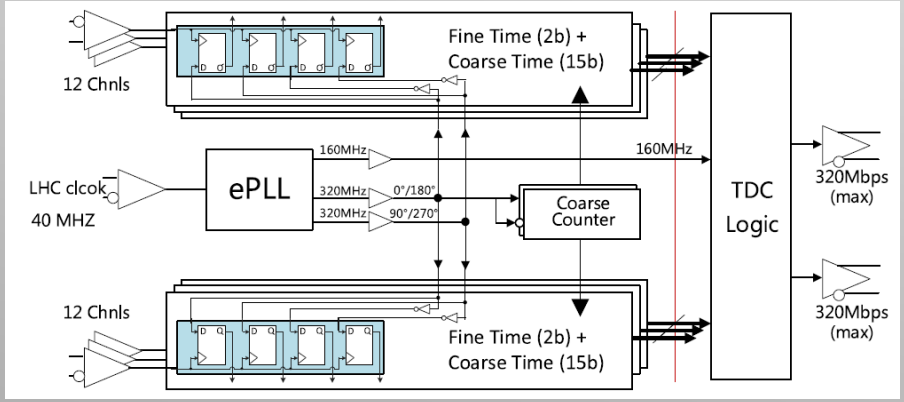


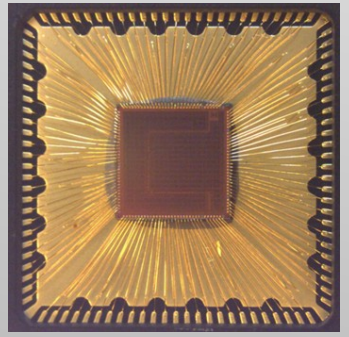


TDC upgrade, design

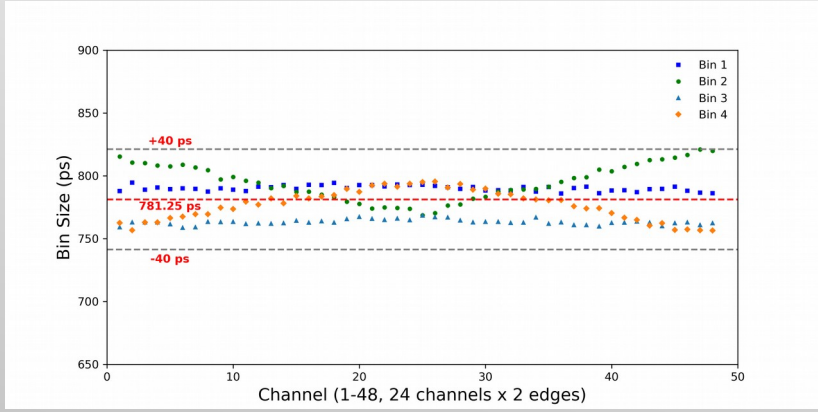
An extension of the available TDC (0.78ns time bin). Keeping the same timing circuit. Updating the logic (to support triggerless operation) and the interface (to 320Mbps), while keeping back compatibility. Reliability, Enlarged buffers. Build on TSCM 130nm platform

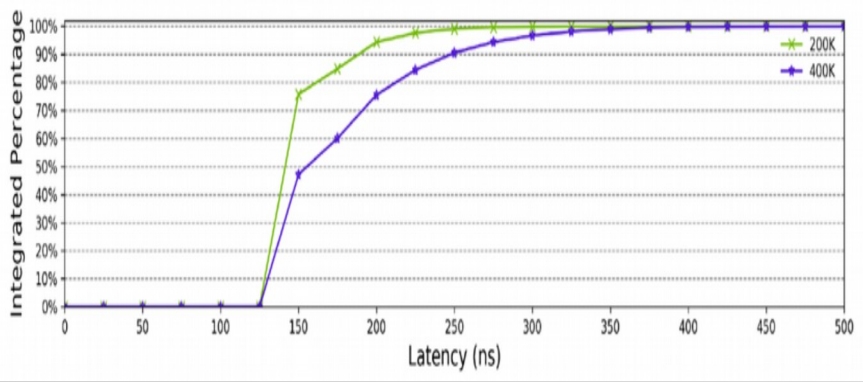
Packaged in a BGA 12x12 (1mm pitch) (First prototype in QFN package)





TDC upgrade, test

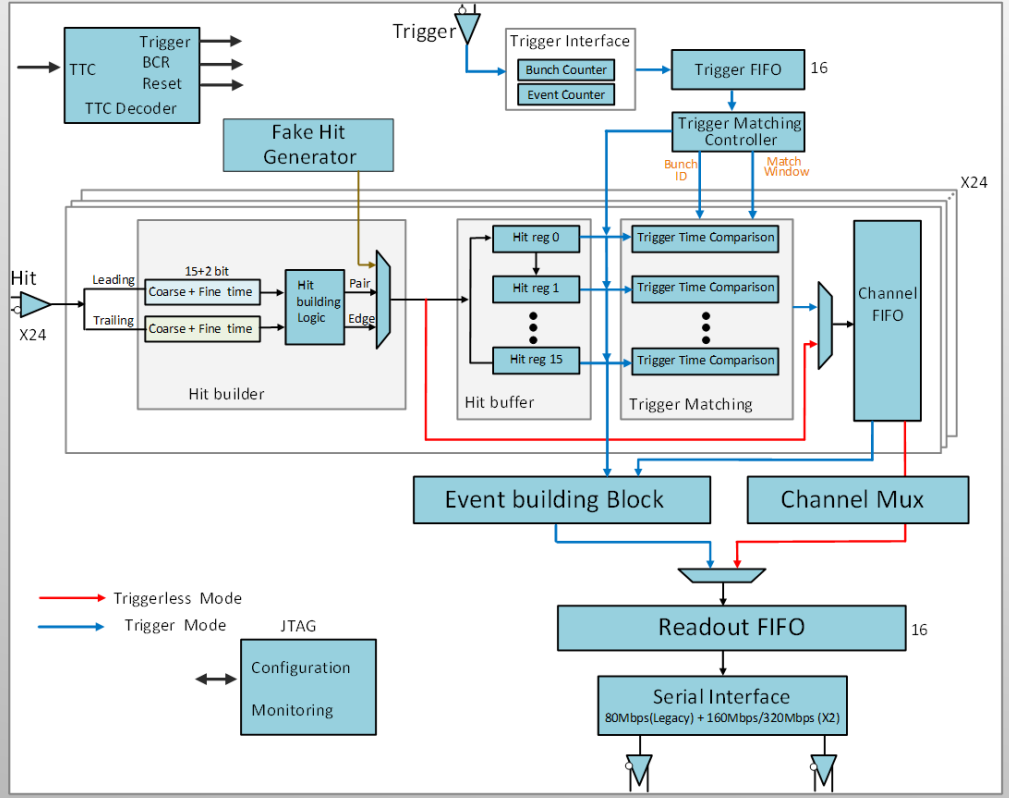




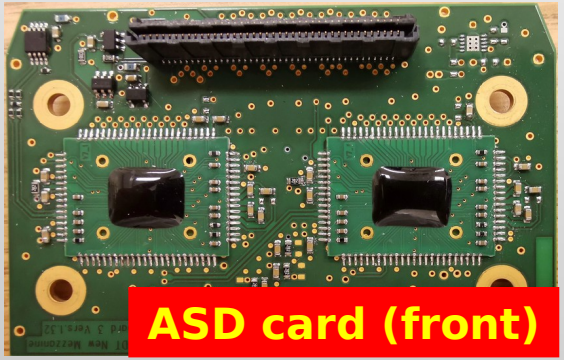
- Uniformity of the bin size 780 ± 40ps
- Latency 350ns at 400KHz hit input
- Power consumption 250mW (from 350mW of the current TDC)

TDC upgrade, test

- **Successful tests for**
  - **Interface, at 80/160/320Mbps**
  - **TTC, legacy and new BCR**
  - **Leading & trailing edge, pair modes**
- **time out for edge paring, TDC ID output, Negative pulse mode, Full Band width with Idle packet inserting**



ASD and TDC integration



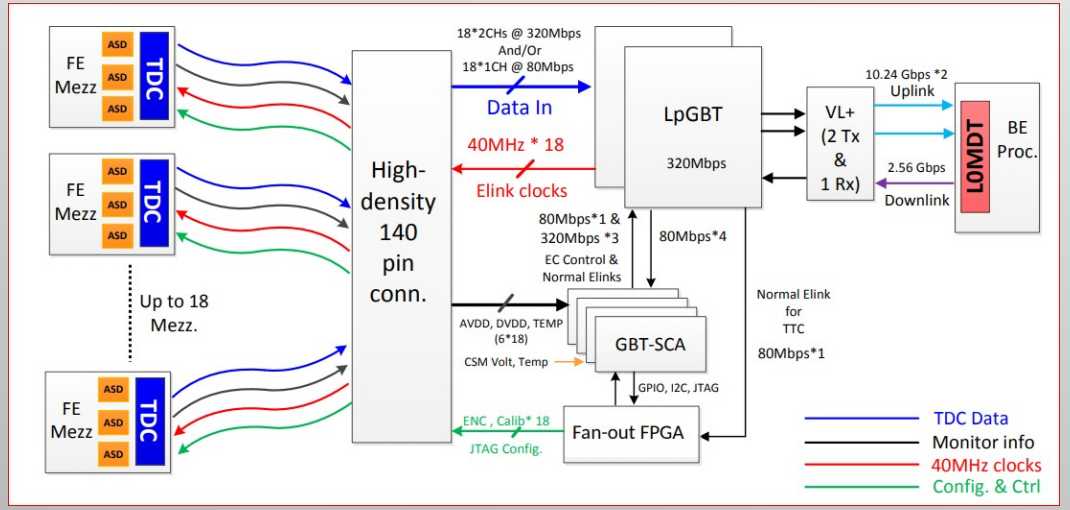
- Interface between ASD and TDC studied with prototype chips, on a prototype mezzanine
  - No problems found

CSM upgrade, design

- 18 mezz cards @320Mpbs as input bandwidth.
- Output bandwidth > 10Gpbs.
- Lower power consumption ~5W/board
- Readout old mezzanine cards in asynchronous protocol
- Multiplex a mixture of old &new cards

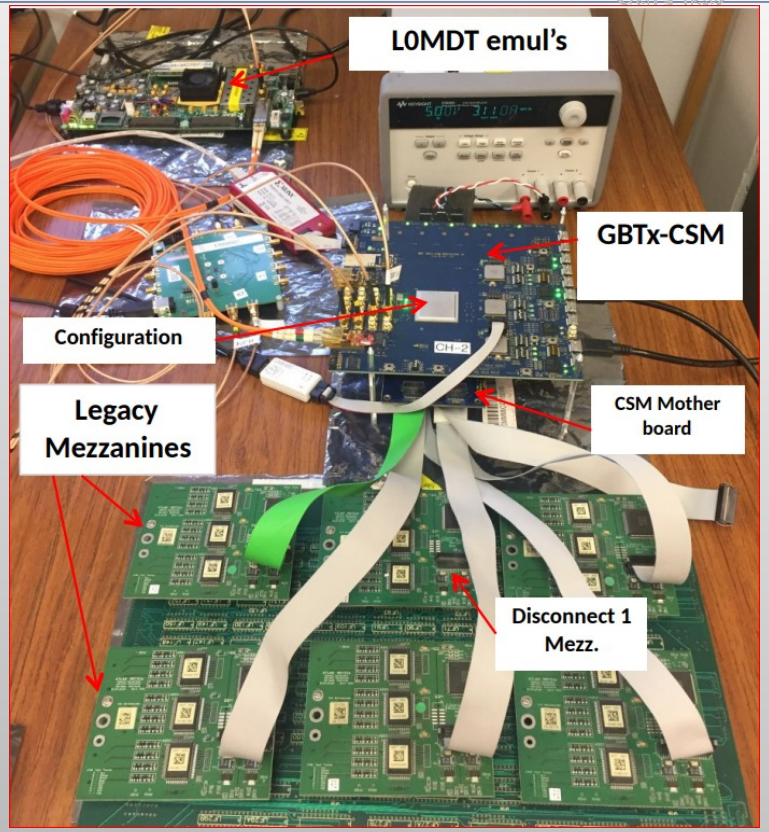
CSM upgrade, from prototype v1 to prototype v2

- Move to the CERN platform for data transmission, monitoring and control.
- Change power scheme from FEAST to radiation hard LDOs
- Schematic design, layout, power scheme: done
- Submitted this month
- Using the prototype lpGBT, with known issues
  - To be fixed in the next version



CSM upgrade, prototype v1 test results

- Tester concept developed in parallel to the first prototype. Evaluate
  - FEAST Power
  - GBTx configuration
  - Clock distribution
- Integrate with new TDC
  - Data link, SCA control, JTAG fanout
- Integrate with legacy mezz cards
  - ASD & TDC configuration
  - GBTx configured 80/160/320Mbps



MDT Upgrade electronics, schedule

- ASD chip has passed all the internal ATLAS reviews in the last two years. The final results of the preproduction run are going to be used as input to the Production Readiness Review.
    - At the end of 2020 all the chips will be available in packaged form.
- TDC engineering samples (~40 chips) are available.
    - Standalone testing and first integrations with the ASD chip.
    - Preproduction submission (~2k chips) planned for the end of 2020.
- CSM design for second prototype is available
    - Moving to preproduction by 2021

Summary

- MDT electronics are being updated for Phase-II to match the trigger requirements of the ATLAS experiment.
  - Progress on semiconductor processes, optoelectronics and fpgas are actively helping in this target
- All projects are on track to their schedule.
- Moving to integrating the different chips to their boards