The Front End Electronics for the Drift Chamber readout in MEG experiment upgrade

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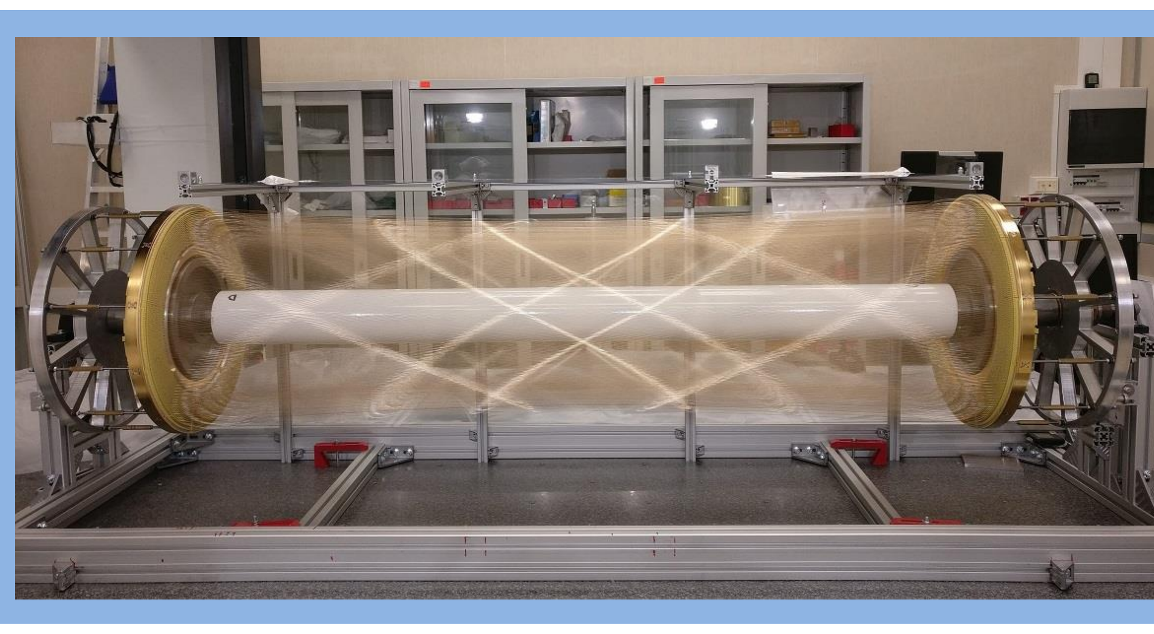
ABSTRACT

Front End electronics plays an essential role in drift chambers for time resolution and, therefore, spatial resolution. The use of cluster timing techniques, by measuring the arriving times of all the individual ionization clusters after the first one, may enable to reach resolutions even below 100 µm in the measurement of the impact parameter. A high performance Front End electronics, characterized by low distortion, low noise and a wide bandwidth has been developed with the purpose to implement cluster timing techniques in the new drift chamber for the upgrade of the MEG experiment at Paul Sherrer Institut (CH) [1].

THE MEG II DRIFT CHAMBER

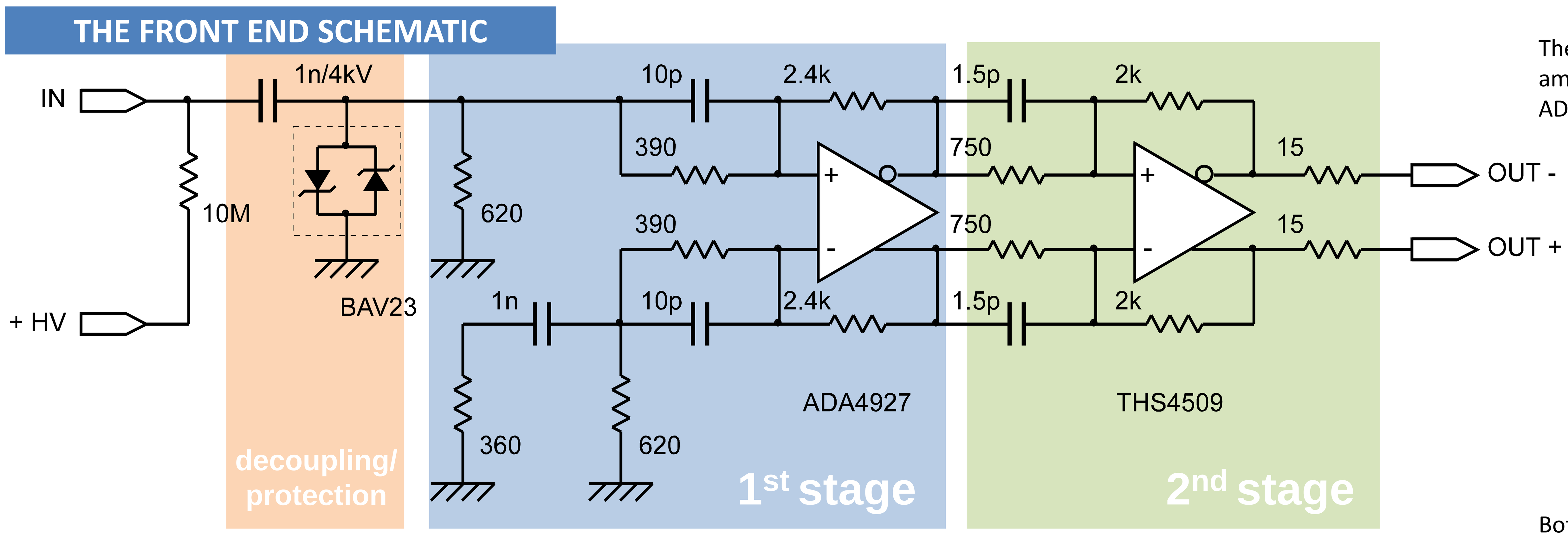
The MEG II Cylindrical Drift Chamber (CDCH) is a single volume detector, whose design was optimized to satisfy the fundamental requirements of high transparency and low multiple scattering contribution for 50 MeV positrons, sustainable occupancy (at $7{\times}10^7$ μ^+/s stopped on target) and fast electronics for cluster timing capabilities [2, 3].



In order to permit the detection of single ionization clusters, the electronic read-out interface has to process high speed signals. For this purpose, a specific high performance 8-channels front-end electronics (FE) has been designed with commercial devices such as fast operational amplifiers [4].

The FE was designed for a gain which must produce a suitable read-out signal for further processing, low power consumption, a bandwidth adequate to the expected signal spectral density and a fast pulse rise time response, to exploit the cluster timing technique [5, 6].

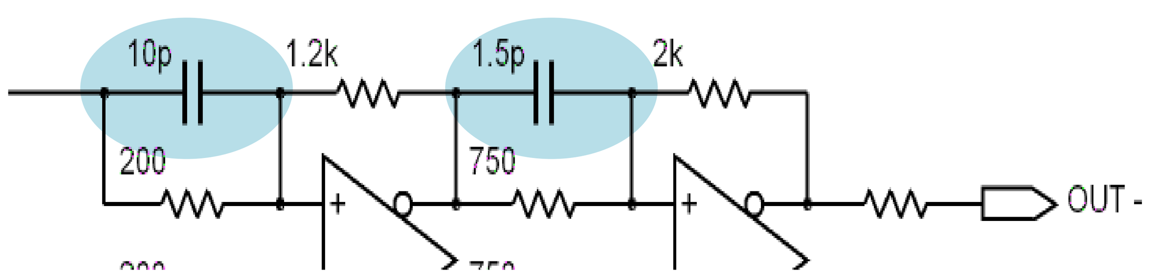
THE FRONT END SCHEMATIC

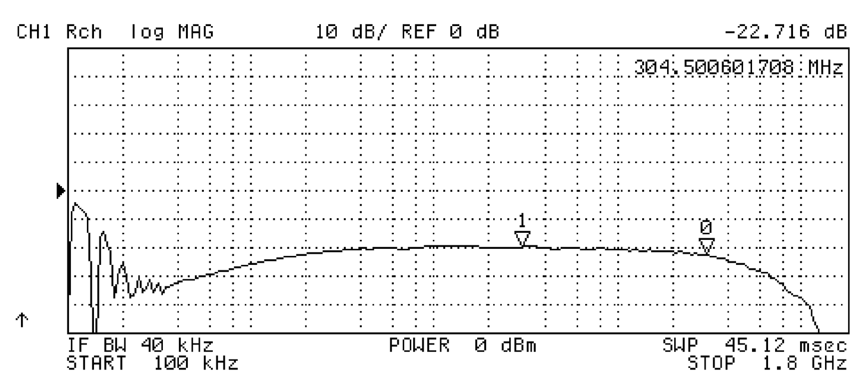


The input network provides decoupling and protection, while signal amplification is realized with a double gain stage made from ADA4927 and THS4509:

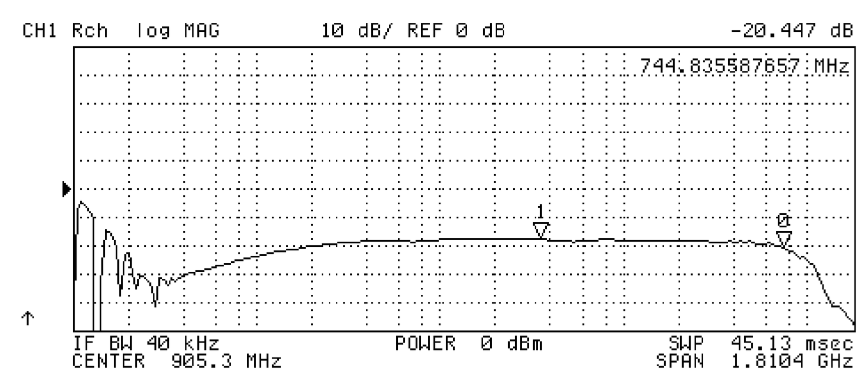
- Analog Device's op-amp ADA4927 works as a first gain stage. The current feedback architecture provides a loop gain that is nearly independent of the closed-loop gain, achieving wide bandwidth, low distortion, and low noise (input voltage noise of only 1.3 nV/√Hz at higher gains) and lower power consumption than comparable voltage feedback amplifiers [7].
- The THS4509 by Texas Instruments is used as a second gain stage and output driver. It is a wide-band, fully differential operational amplifier with a very low noise (1.9 nV/√Hz), and low harmonic distortion (-75 dBc HD_2 and -80 dBc HD_3 at 100 MHz). The slew-rate is 6600 V/s with a settling time of 2 ns to 1% for a 2 V step; it is ideal for pulsed applications [8].

Both the devices are ideal for pulsed applications.





AFTER 5m LONG OUTPUT CABLE WIHTOUT PRE-EMPHASIS

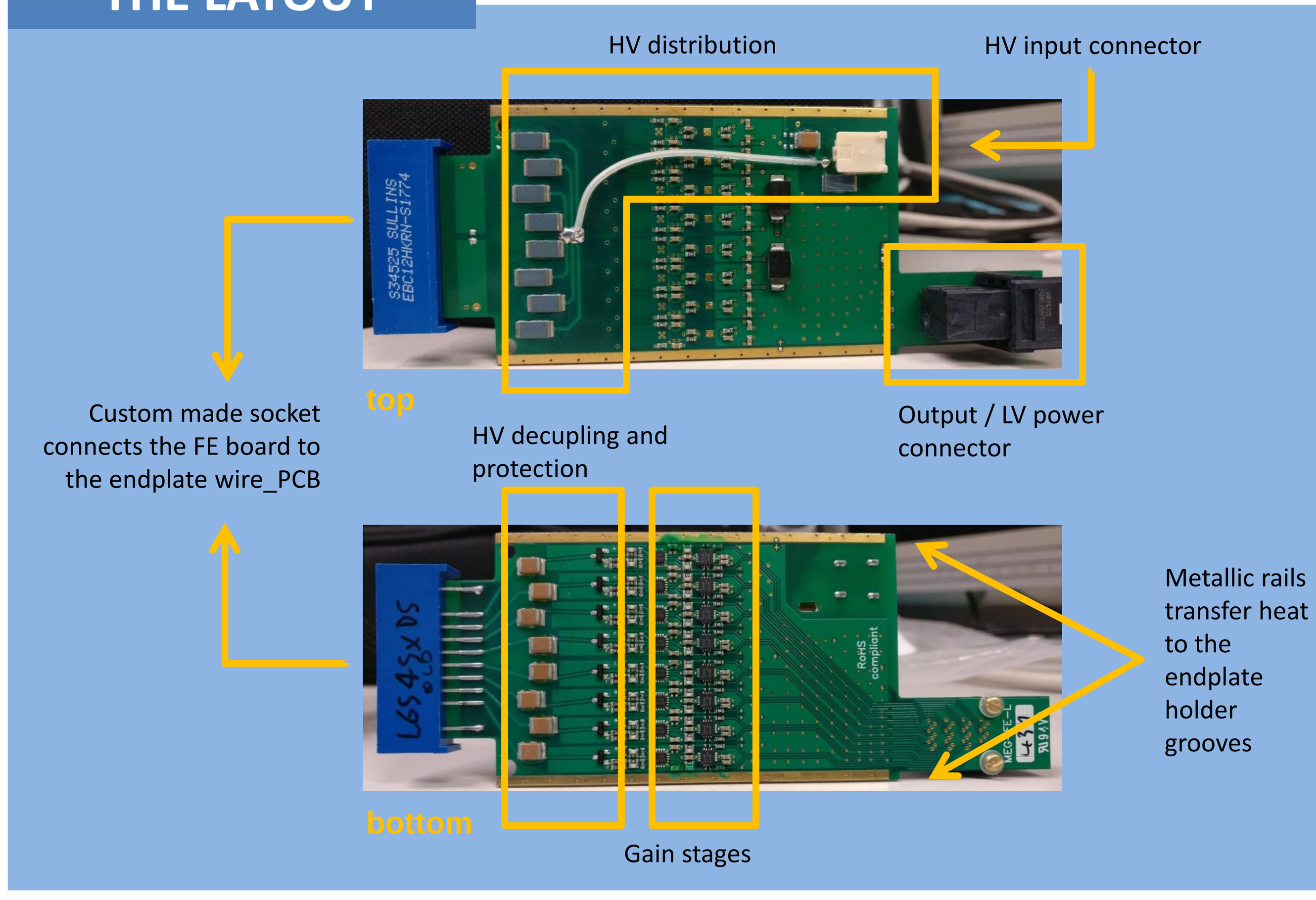


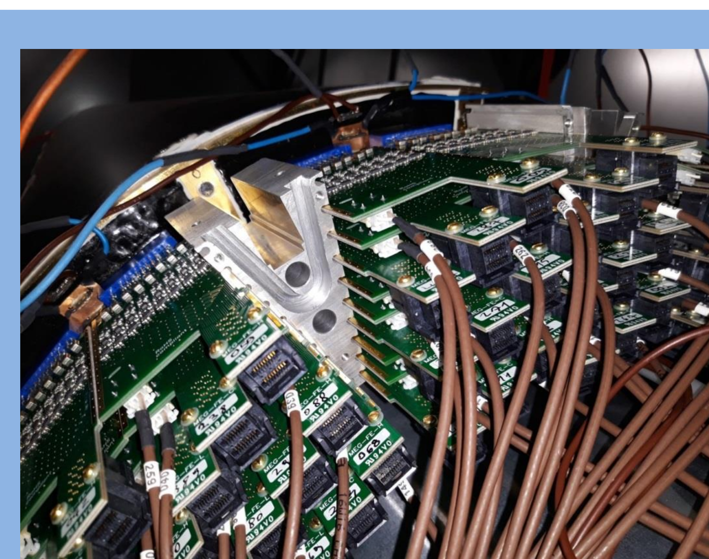
AFTER 5m LONG OUTPUT CABLE WITH PRE-EMPHASIS

In order to balance the attenuation of the output cable, a pre-emphasis on both gain stages has been implemented. The pre-emphasis introduces a high frequency peak that compensates the output cable losses, resulting in a total bandwidth of nearly 1GHz.

The current consumption for each channel is 60 mA at a voltage supply of ±2.5 V; this correspond to a total power dissipation per end-plate of about 300 W, therefore an appropriate cooling system made both with recirculation of coolant fluid and with forced air is used.

THE LAYOUT





Due to the area of the FE output connector socket and considering the available space between the CDCH layers, three different board versions have been designed, one with the output connector on the right, one in the center and one on the left.

The output of the FE is connected to the WDB through a custom made cable 5m long, designed to have a stable, flat frequency response, made by shielded parallel pairs, each pair being individually shielded, (Amphenol Spectra Strip SkewClear®).

Some pairs of the output cable are used for powering the FE board.

HV bias to the CDCH sense wires is provided through the FE board via a dedicated connector.

Pre-amplified differential signals are successively digitized by the WaveDREAM board at a (programmable) speed of 2 GSPs with an analogue bandwidth of 1GHz [9].

PERFORMANCES

Linearity for each channel of the FE board was measured:

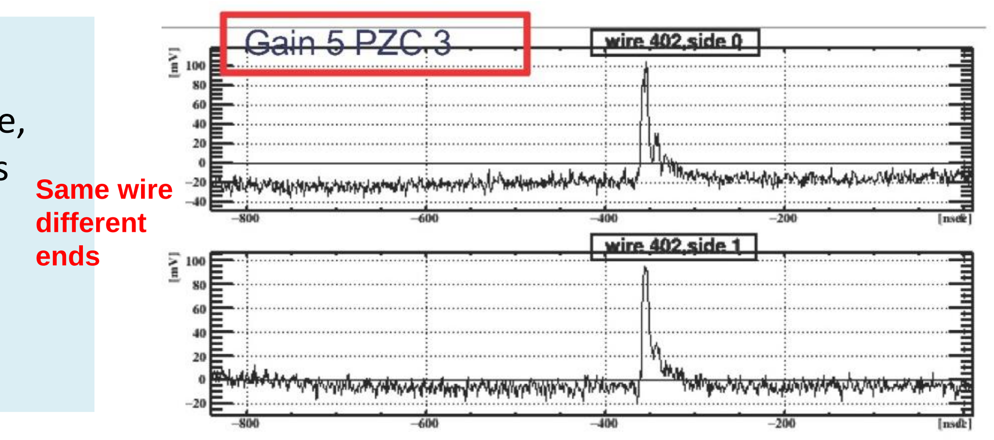
- Gain (V_{out}/V_{in}) is 20dB (middle bandwidth) on 120 Ω load
- Mean non-linearity is less then 0.1 % (V_{in}: 15mV ÷ 75mV)

Cross talk between adjacent channels (Ch+1) is ~1%, cross talk to next channel (Ch+2) is negligible (<0.5%).

Noise level measured (in the experimental area) is less then 2mV, after 5m long cable, on a 120 Ω resistive load.

Despite a low frequency interference, a residual noise of ~2mV (sigma) has observed.

The source of the interference has been later identified and removed.



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