Design and first performance results of waveform sampling readout electronics for Large Area Picosecond Photodetector

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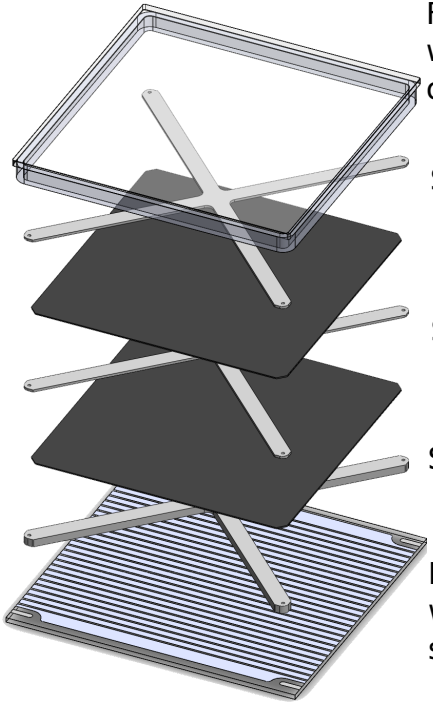
Large Area Picosecond Photodetectors (LAPPD)

INCOM
BRIGHT IDEAS

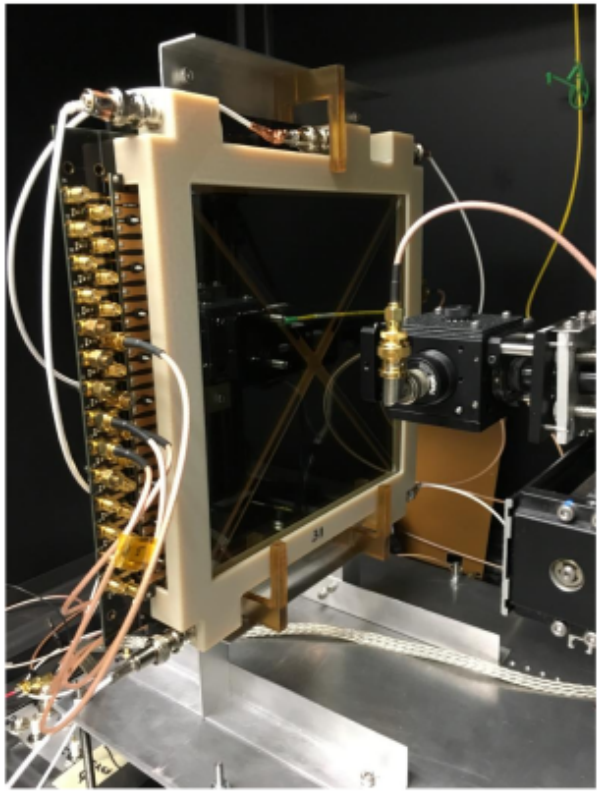
- MCP based photodetector
- Large sensitive area of 200×200 mm
- Quantum efficiency $> 20\%$
- Gain $> 10^7$
- Dozen of picoseconds temporal resolution
- About 1 mm spatial resolution
- Strips anode structure



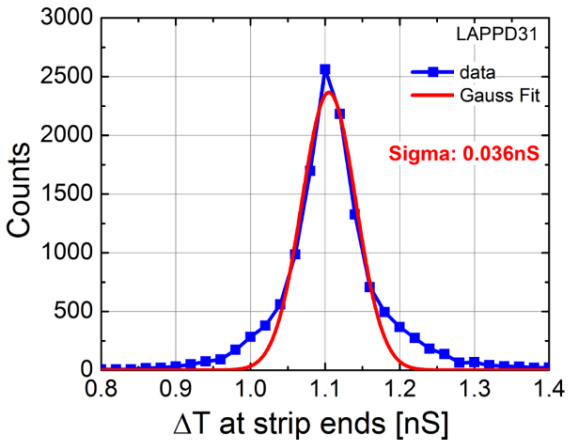
www.incomusa.com/lappd/

Stripline anode structure allows to significantly decrease number of readout channels keeping spatial resolution still high

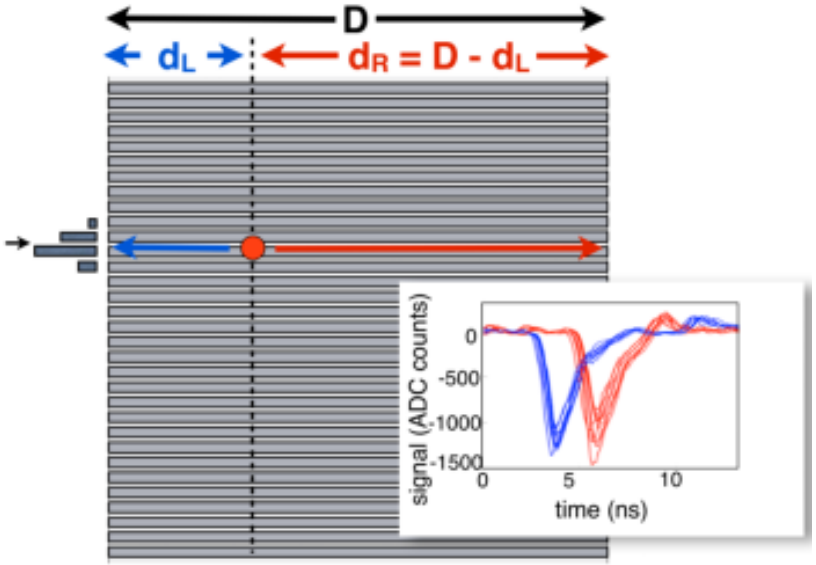
LAPPD anode structure



A. Lyashenko, VCI2019 Proceedings



- Currently available stripline LAPPDs have 28 anode strips. Total 56 pins.
- Strip number – coarse vertical position. Strip pitch is ∼6.5 mm. Centroiding can improve resolution to ∼ mm
- Time difference between two ends – position along strip (observed ∼3 mm)



G. Jocher *et al.*, NIM A822, 25 (2016).

Motivation for electronics development

Motivation

- LAPPD devices are now commercially available
- A readout card capable for work with LAPPD out of the box may be of interest for both LAPPD R&D itself and for groups who intend to use such devices for small experiments

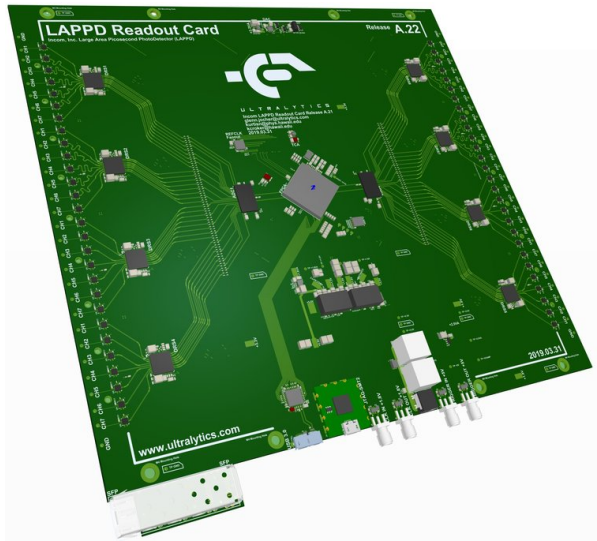
Goals

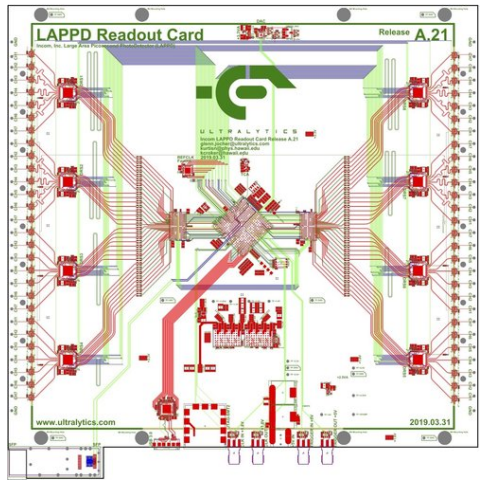
- Integrated readout solution for LAPPD photodetectors which may be easily incorporated to different experimental needs
- Parallel read out of all 56 channels of the device
- High sampling rate consistent with the LAPPD time resolution
- High speed readout
- Flexible triggering
- **Open-source** firmware/software which provides full control of the device and data taking process

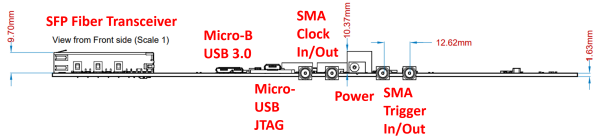
LAPPD readout electronics

- General concept and design – cooperation of **University of Hawaii**, **Incom**, and **Ultralytics LLC**
- Hardware – **Ultralytics LLC**, Clarksburg, USA
  www.ultralytics.com/lappd
- Firmware and software – **University of Hawaii**

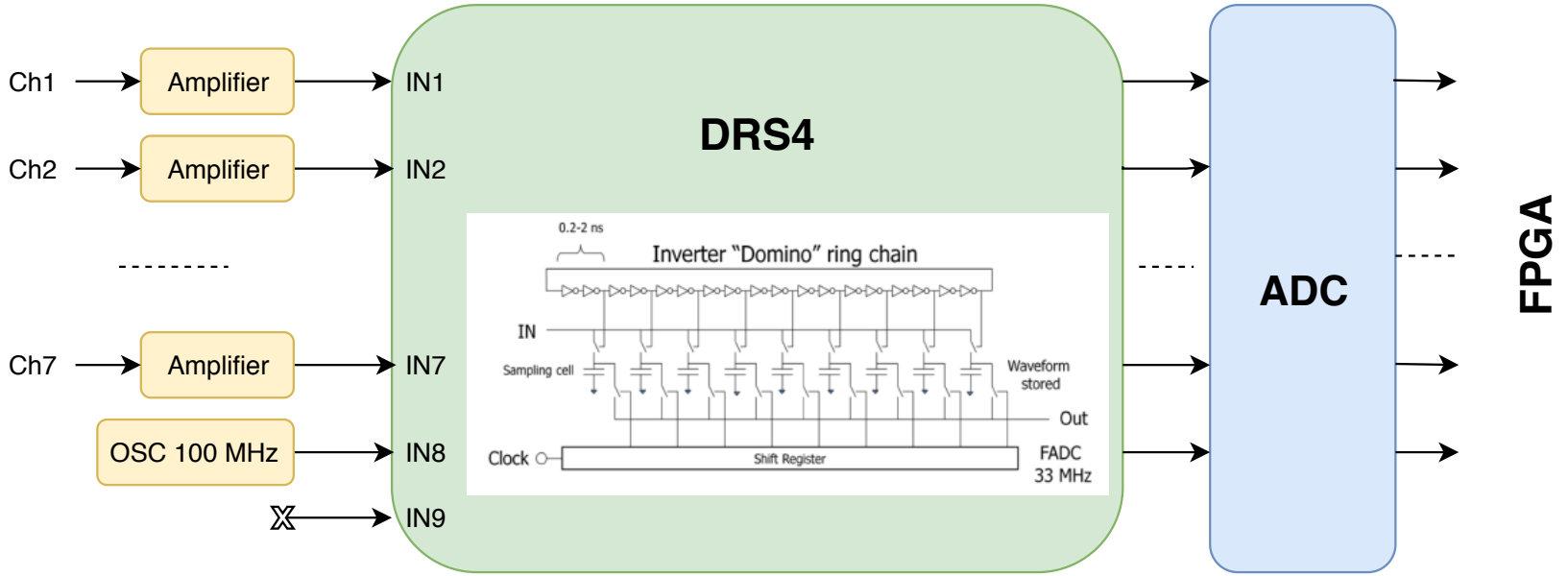
- Xilinx Artix-7 FPGA
- 8×DRS4 (www.psi.ch/drs)
- 2×32-channel ADS52J90 ADC for full parallel readout
- SFP fiberoptic transceiver
- USB 3.0, JTAG
- 4×SMA connectors for clock/trigger in/out for synchronisation among multiple boards







DRS4 for waveform sampling

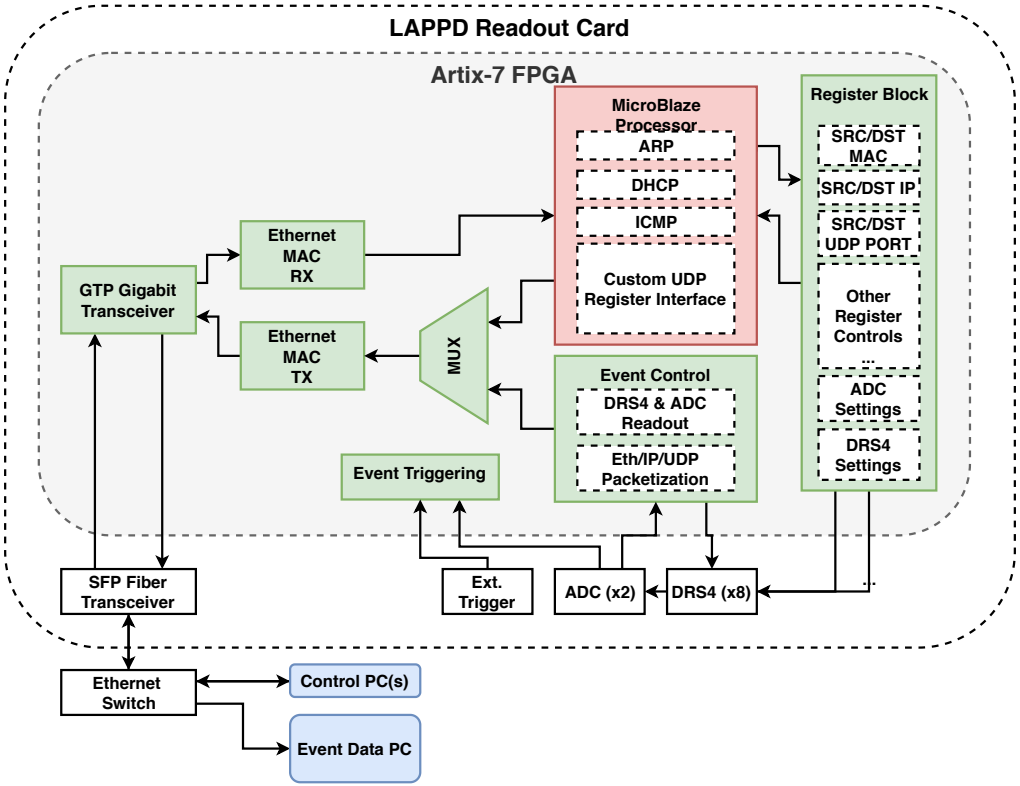


- Sampling with switched capacitor array of 1024 samples
- Sampling rate up to 5 GSPS
- Parallel read out of all channels
- Transparent mode for self triggering
- Region of interest readout mode which may significantly decrease readout time
- One channel in each DRS4 is connected to 100 MHz oscillator for time calibration

Firmware

- Control over DRS4 readout sequence
- Building of the event data and sending it to readout PC

- Ethernet MAC implemented in firmware
- Microblaze soft-core CPU allows implementation of ARP, DHCP and ICMP
- Asymmetric data flow: slow data channel for registers access and fast downstream at near full link bandwidth



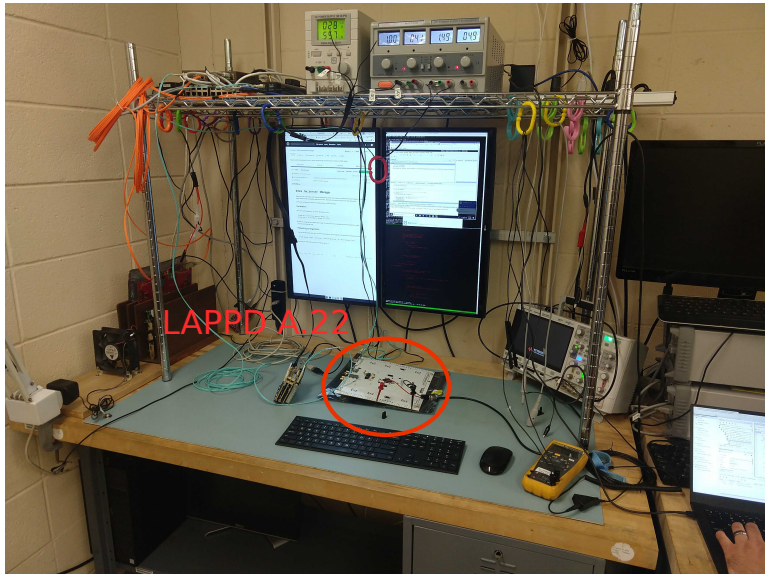
To be implemented

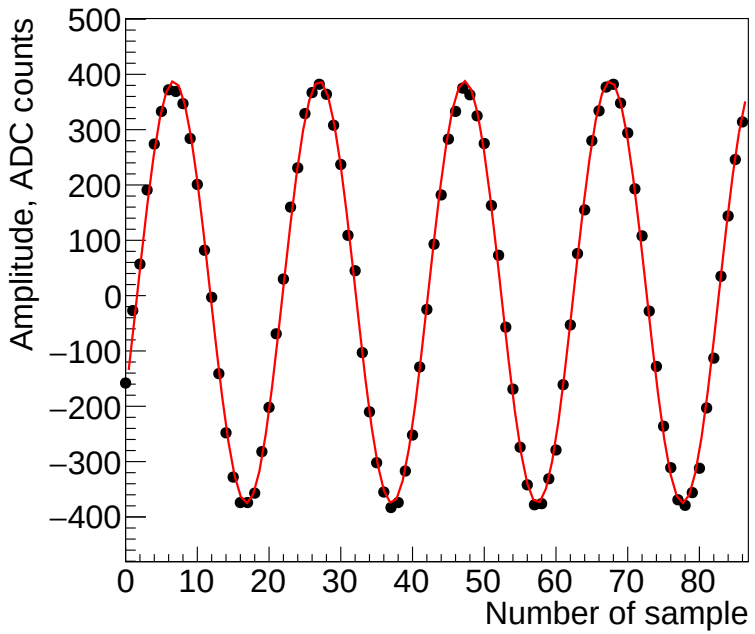
- On-line pedestals subtraction
- Zero suppression
- On-line (A, t) extraction
- Self-triggering with DRS transparent mode

- UDP-based protocol for registers reads and writes
- Data stream from FPGA is multiplexed with slow data channel in fabric and goes directly to Ethernet MAC TX

Firmware/hardware status – A.21 prototype

- First fully exercised PCB
- Two A.21 boards produced
- 2 instrumented DRS-4 chips : 14 channels (7 strips)
- 0.7 mV nominal noise (on-site)
- DRS4 control, full, and ROI readout sequence implemented
- Full waveform of 1024 samples takes about 120 μs. May be improved to 60 μs
- Calibrations: pedestal, timing, and precision gain (TCAL only)
- Issues : amps and DRS4 offsets mismatch (amps removed), grounding issues



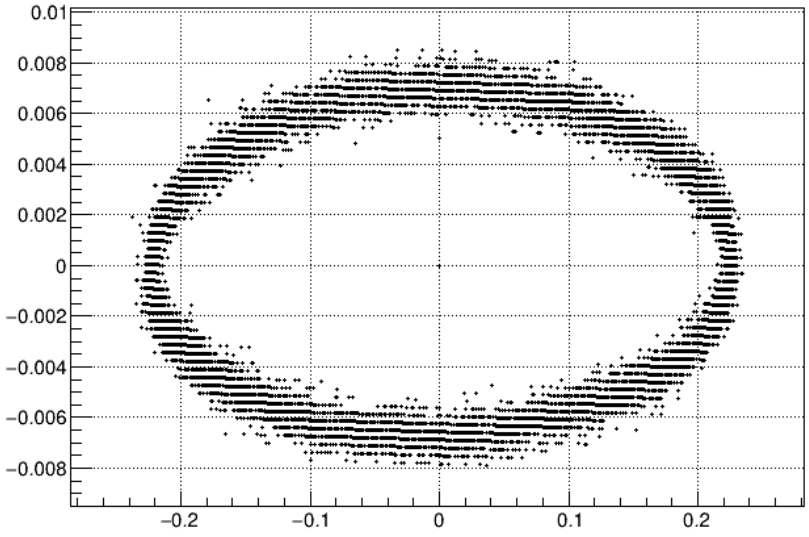


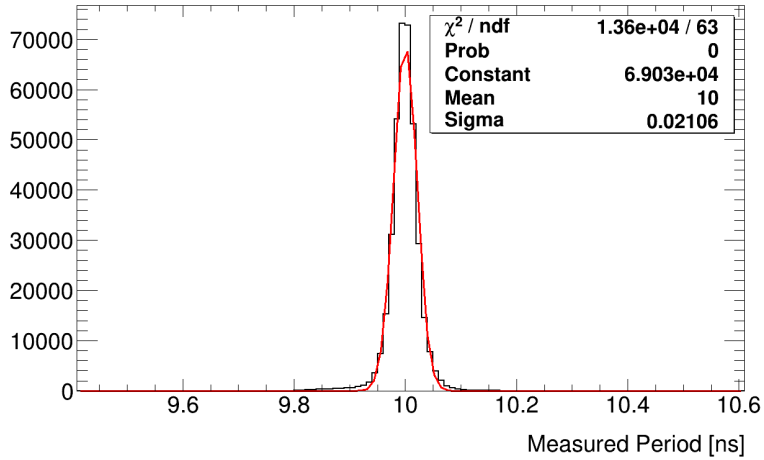
Pulse tests

- 2 ns rise, 100 mV pulses
- ≈26 ps intra-DRS4 resolution
- $\lesssim$57 ps inter DRS-4 resolution

Time-offsets calibration

- Individual timing offsets for sampling cells
- Procedure derived from *K. Nishimura, et al., Physics Procedia 37 (2012)*
  $V_i = A \cdot sin(2\pi f t_i + \phi) + P_i$
  $x = V_i + V_j = 2A \cdot sin(\pi f \Delta t_{ij}) + x_0$
  $y = V_i - V_j = 2A \cdot cos(\pi f \Delta t_{ij}) + y_0$
- x vs y – ellipse from which shape one can extract Δt_{ij}
- Simplified procedure : ellipse fitting -> moment calculation
- Expect improvements with : *B. Cheng, et al., Nucl. Instrum. Methods A 916(2019)* time offsets calibration along with calibration of the sampling cell gains





Evolvable Embedded Vechicle for Execution of Experiments

EEVEE is currently leveraged on 3 separate hardware platforms, using Xilinx Generation 6 and Generation 7 FPGAs

- Extensively documented, embedded C, open-source UDP/IP stack: DHCP and "headless" configuration, automatic discovery, Python library.
- Extendible via "stones": Demo telemetry module written, FPGA pedestal subtraction planned, OTA firmware update could be implemented

LAPPDDigest: rapid prototyping Python 3.5 readout on commodity platforms

- Small, multiprocess, tools: common command-line interface
- 4 core PC with SSD: 3kHz, 6 channels, 1024 samples (raw)
- On the fly or offline: pedestal subtraction and timing calibration
- Python pickled data, easily converted into Incom existing toolchain

Software

EEVEE
The Evolvable Embedded Vehicle for Execution of Experiments

Microblaze side: ARP, IP, DHCP, access to FPGA registers
PC side : basic functions library to communicate with the board

LAPPD control
LAPPD specific functions to set operational parameters of the board

LAPPD digest
receive data stream, event unpacking and reconstruction

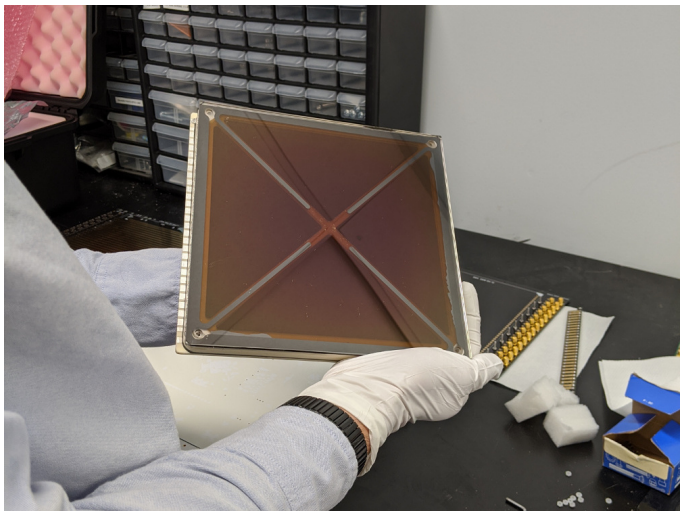
Visualization and control GUI

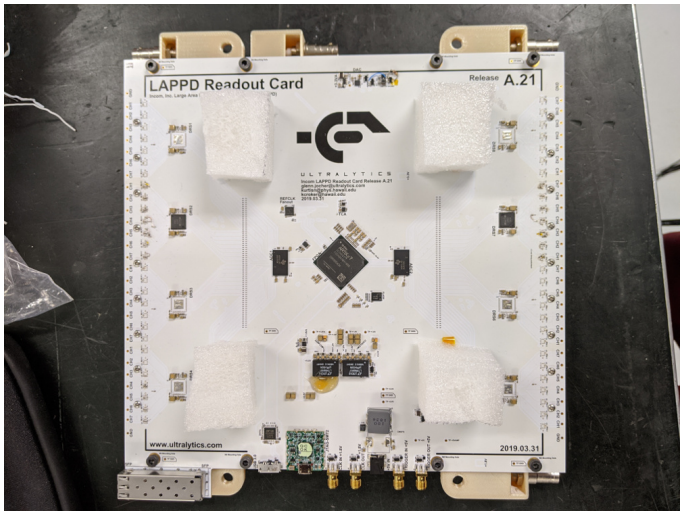
Open-source and extremely flexible software package is being developed.

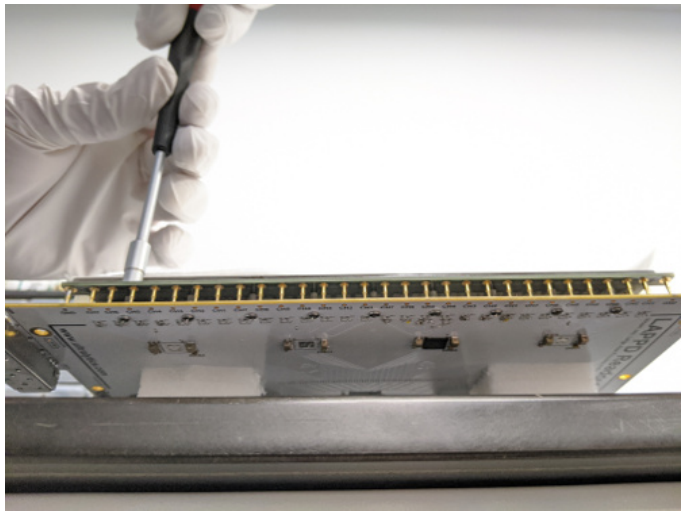
https://github.com/kcroker/eevee

Tests @ Incom

- A.21 prototype readout board shipped to Incom in Dec. 2019





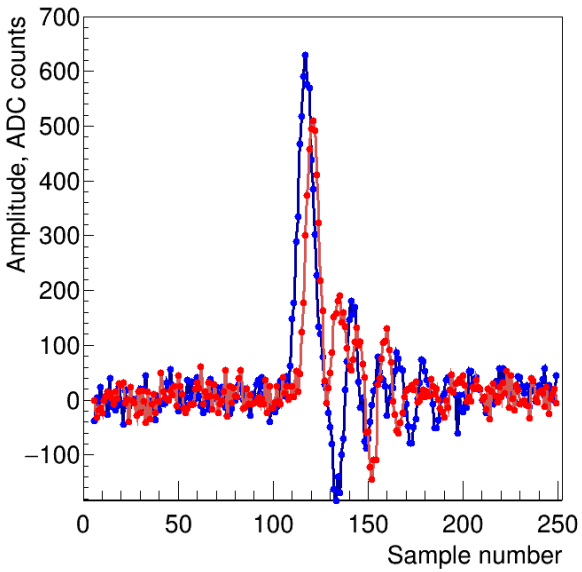


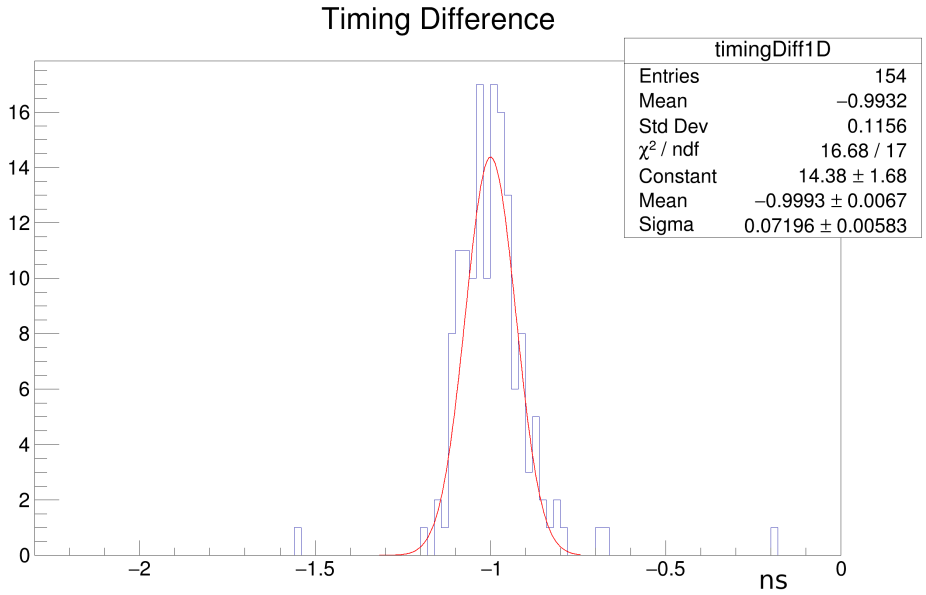
Tests @ Incom : first results

- Tests with laser pulse
- ≈72 ps time resolution for time difference between two ends of the same strip

Limiting factors :

- Hardware noise issues mostly related to grounding
- Very preliminary timing calibration of the DRS-4 samples. A lot of room to improve.





Conclusion

- Development of the universal highly integrated readout card for LAPPD has reached fully functional prototype stage.
- Required functionality implemented in the both firmware and software.
- $> 10\times$ faster than chained DRS4 eval board
- All performance specs are lower-bound: all aspects can be improved
- A.21 shipped to Incom. First tests with LAPPD tile performed.
- A.22 (next hardware version) PCB expected end of Q2 2020
- MK2 data protocol and C readout expected to deliver 10 $\times$ speed improvements (at least)

Thank you for your attention!