The GEM-based detector for tracking the Compton-scattered photons in the Laser Polarimeter facility at VEPP4-M collider.

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Abstract: *The Laser Polarimeter is being developed at VEPP-4M collider for beam energy calibration by Resonant depolarization technique. The essential part of this facility is a photon-tracking detector measuring trajectories of back-scattered gammas.*

The Laser Polarimeter facility

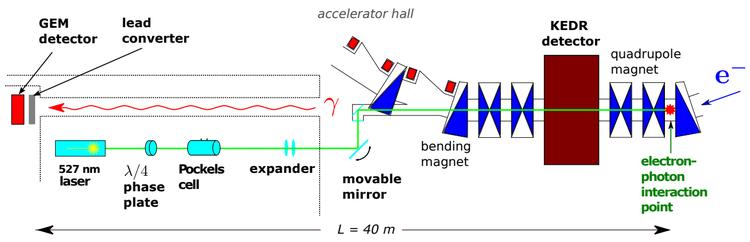

Figure. 1: *The Laser polarimeter layout at VEPP-4M.*

The VEPP4-M collider has a unique system for energy measurement based on Resonance Depolarization technique. The existing system is working well using the Touschek effect for measurement of polarization at the energies below 2 GeV. Unfortunately, at higher energies the efficiency of the Touschek polarimeter is rather small. For higher energies it was proposed to develop Laser polarimeter [1] which is based on the effect of up-down asymmetry of Compton back-scattering of circularly polarized photons by vertically polarized electrons.

The general view of the laser polarimeter at VEPP-4M is shown in Figure 1. The difference of an average vertical scattered angle for left and right circular polarization depends on the beam polarization in this scheme.

The very first energy measurement using this scheme was done in 2017 (fig. 2), while in this experiment for registering particles converted from back-scattered photons the tracking detector of the DEUTERON facility was used [2].

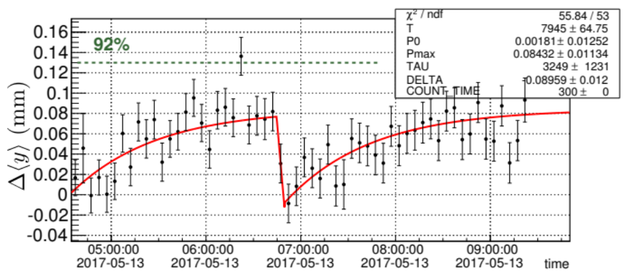

Figure 2: *Radiative polarization process and depolarization jump observed at the energy of 4.1 GeV.*

The GEM Detector

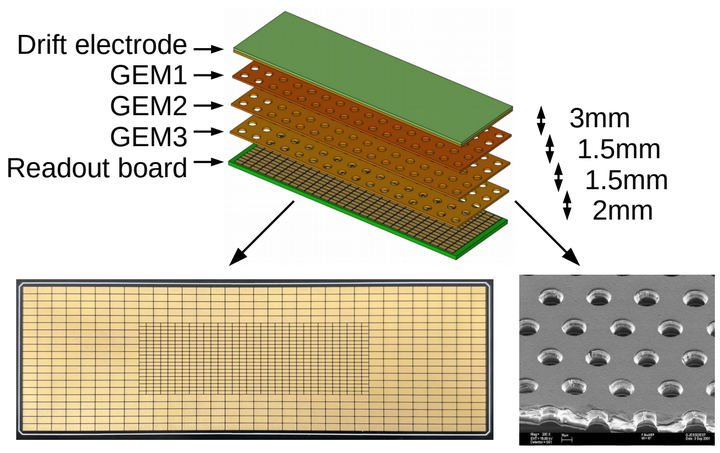

Figure 3: *Schematic view of the detector's sensitive area*

The development of the detector's design was started in 2015 and during 2018 the detector was finally assembled.

The sensitive area of the detector is 128x40 mm^2 and consists of three cascades of gaseous electron multiplier (GEM) with the pad readout structure (fig. 3). The readout structure is a rectangular grid of 1120 pads, which are 2x1 mm sized in center and 4x2 mm on the edge, where bigger pads are used for a rough alignment of the detector.

Detector has a modular design and encompasses several boards (fig. 4, 5):

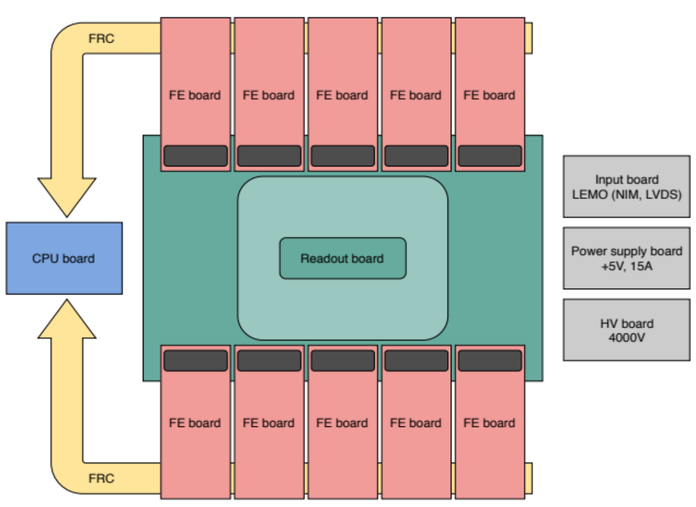

Figure 4: *Overview of the detector electronics and data acquisition system*

- readout board with GEMs and readout structure;
- ten FE-boards with DMXG64 ASICs [3] and ADCs;
- CPU board (DE10-Nano) with FPGA/SoC and gigabit ethernet;
- trigger-polarity input board with LEMO connectors (NIM);
- Power supply board (low voltages for all boards);
- High Voltage board providing up to 4kV for the detector.

FE-boards are inserted into FMC sockets on the readout board, to which the pads of readout structure are connected. FE-boards are grouped into pack of five for top and bottom regions. Each pack is connected in parallel via flat ribbon cable to 40-pin IDC connectors of the CPU board. The trigger-polarity input board is inserted into Arduino socket of CPU board.

The modular design allows one to replace some parts, for example the readout board can be replaced by the PCB with different readout structure, because sensitive area can be disassembled and reassembled again without much efforts.

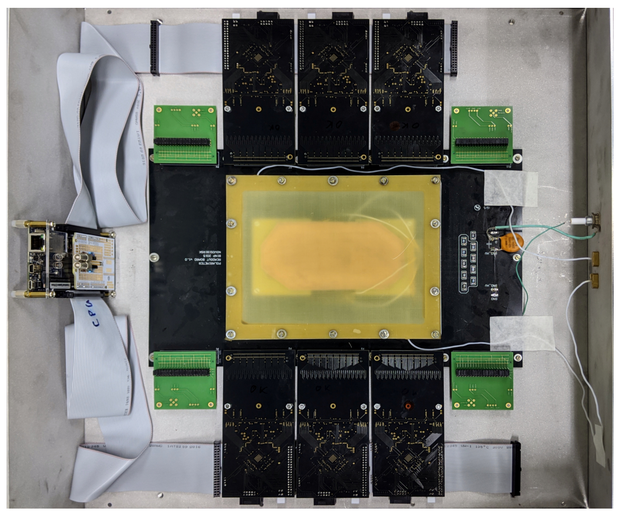

Figure 5: *Essential components of the detector assembled.*

FE electronics

Front-end electronics of the detector is based on the DMXG64 ASIC (64 channels, 100 frames of analog memory), twenty of these chips are required to cover 1120 channels in total. Thus it was divided into ten FE boards.

Each FE board (fig. 6) contains protection circuits against high voltage discharge, two DMXG64 ASICs (with dedicated 14bit ADC each) and Altera MAX10 FPGA to generate the sequence signals for the FE chips, readout and put the digitized data onto the parallel bus. Also, the FE board has a miniUSB connector and FT230X USB-UART IC onboard, thus it can work standalone without CPU board.

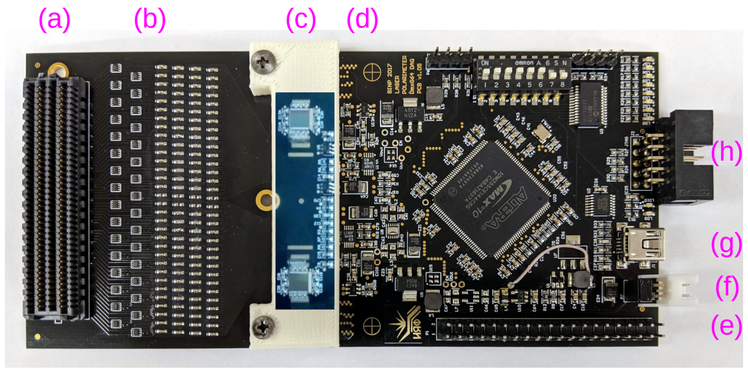

Figure 6: *FE board elements: (a) SAMTEC FMC connector, (b) ESD protection circuits, (c) DMXG64 ASICs, (d) 14bit ADC, (e) CPU board interface connector, (f) +5V power connector, (g) miniUSB UART interface, (h) JTAG*

The signal from the pads of the readout structure comes through the FMC connector passing by protection circuits into DMXG64 ASIC, after that digitized data from the dedicated ADCs go into FPGA and are transferred to the CPU board or PC by UART.

As the CPU board the Terasic DE10-Nano development kit is used (fig. 7). This kit features Cyclone V FPGA with two hardware ARM cores running Linux and many peripherals in compact enclosure.

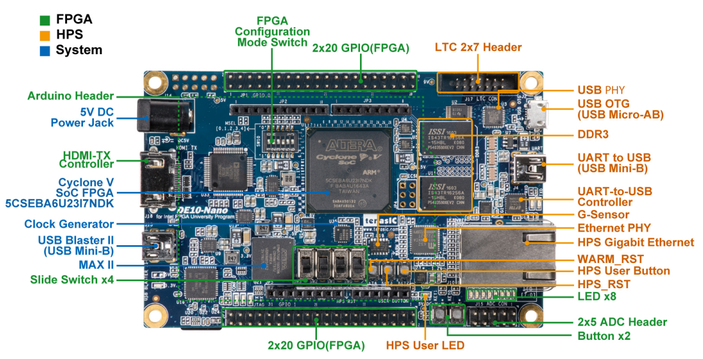

Figure 7: *Terasic DE10-Nano development kit used as CPU board.*

DMXG64 ASIC

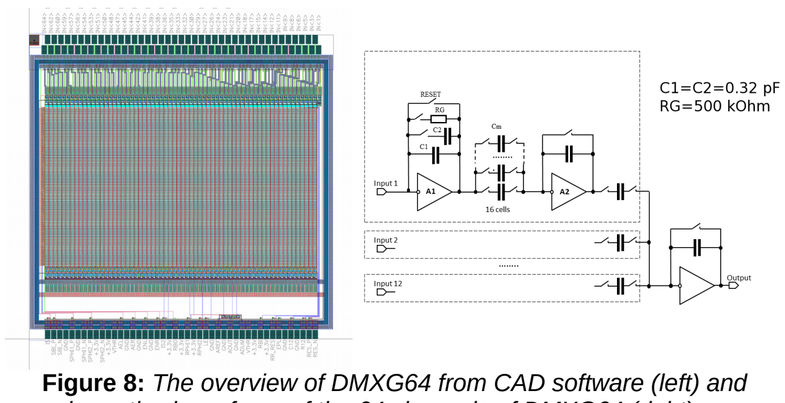

Figure 8: *The overview of DMXG64 from CAD software (left) and schematic view of one of the 64 channels of DMXG64 (right).*

The DMXG64 ASIC was developed in BINP for various GEM-based detectors. It has 64 input channels, while each channel has low-noise charge sensitive amplifier and dedicated analog memory for 100 samples. Figure 8 shows the chip design from the engineering CAD software and the schematic of one channel.

The electronic calibration of the FE board channel was made and results complied to the previous study of the DMXG64 ASIC (fig. 9).

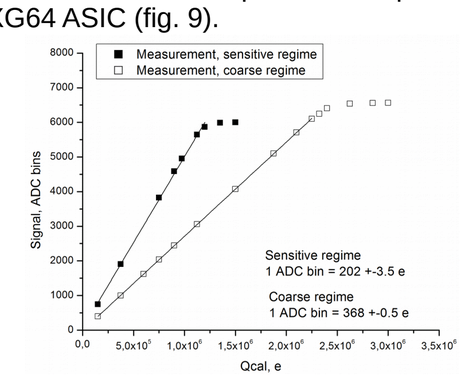

Figure 9: *Electronic calibration results in two modes.*

The measurements with Sr^{90}

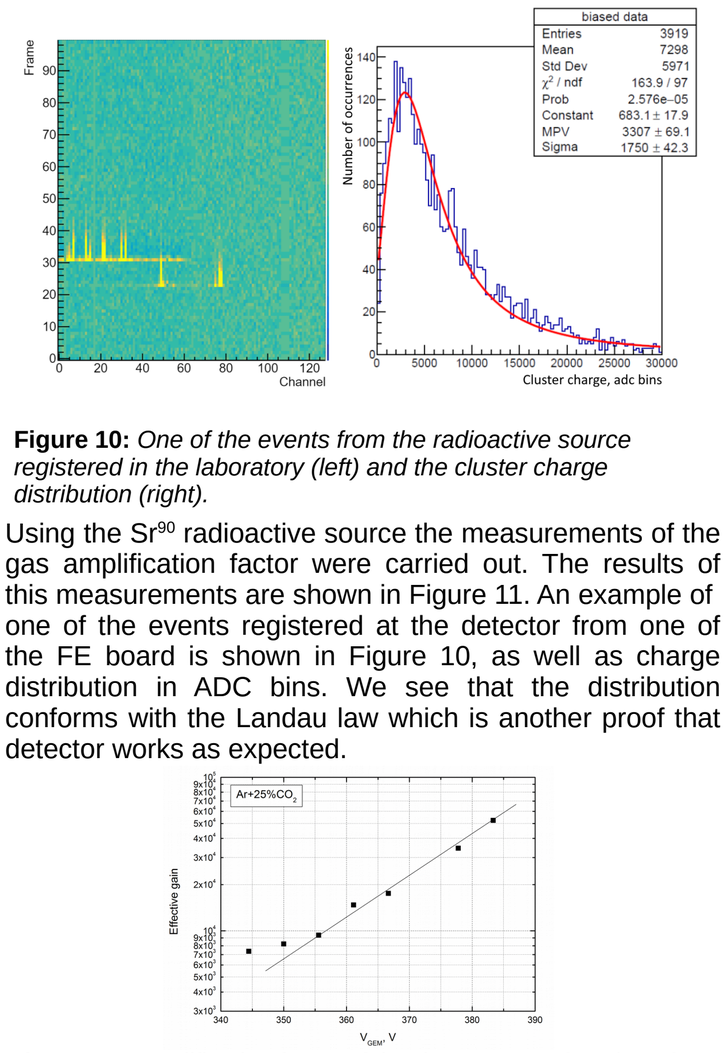

Figure 10: *One of the events from the radioactive source registered in the laboratory (left) and the cluster charge distribution (right).*

Using the Sr^{90} radioactive source the measurements of the gas amplification factor were carried out. The results of this measurements are shown in Figure 11. An example of one of the events registered at the detector from one of the FE board is shown in Figure 10, as well as charge distribution in ADC bins. We see that the distribution conforms with the Landau law which is another proof that detector works as expected.

Figure 11: *Amplification factor of the detector as a function of voltage for the single GEM.*

Conclusion

The Laser Polarimeter facility is under active development. The principle of operation was proved, and the core components of the detector were manufactured and work well.

The detector is scheduled to be put into operation at the Laser Polarimeter facility starting from March 2020.

References

[1] V.E. Blinov et al. / **Laser Polarimeter at VEPP-4M** // JINST, 2017, 12_C08020

[2] V.N. Kudryavtsev et al. / **The development of high resolution coordinate detectors for the DEUTERON facility** // JINST, 2014, 9_C09024

[3] V.M. Aulchenko et al. / **A 64-channel integrated circuit for signal readout from coordinate detectors** // JINST, 2017, 12_C05004