Current and Future FPGA-TDC Developments at GSI

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Outline

Motivation for building TDCs with an FPGA

- flexibility, all-in-one chip (discriminator, TDC, DAQ), FPGA needed anyhow
- channel price "automatically" drops with new FPGA generations
  - factor of 5 in performance/price increase in 5 years
  - game-changer: FPGA/TDC/DAC/Discriminator are not the price determining part of the system anymore!
  - enables the use of FPGAs "everywhere" in the front-end
- new processes (in consumer electronics) can improve radiation tolerance by a factor of ~100 (e.g. FD-SOI - STMicroelectronics)

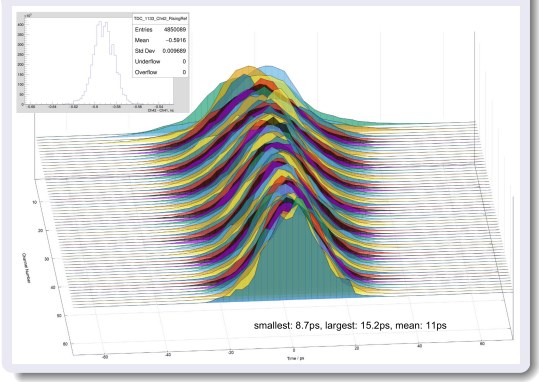
Radiation		Experimental radiation test data	FDSOI28 SER gain w.r.t. BULK 28nm
Atmospheric neutrons (<800MeV)	Sea-level	Neutron-SER < 10FIT/Mb	100×
Alpha particles (@0.001cph/cm2)	Sea-level	Alpha-SER < 1 FIT/Mb	1000×
	Sea-level	RHBD microprocessor immunity	100×
	Sea-level	Ultra low alpha wafer counting	~
Thermal neutron (<25meV)	Sea-level	Thermal-SER < 2 FIT/Mb	20×
Muons	Sea-level	Peak error rate 10x lower than Bulk	>10×
Heavy ions (≤60MeV/(mg/cm²))	space	Asymptotic error X-section=10^{-10} cm²/bit	100×
Low energy protons (<10MeV)	space	Error cross-section < 10^{-14} cm²/bit	1000×
Gamma rays (10KeV)	space	VTH shift <1mV/krad (till 100krad)	~

ST, Central CAD and Design Solutions, SER FDSOI28, P.Roche et al.

Features of FPGA-TDCs

- FPGA TDCs can be very precise and affordable time measurement devices
- trade-off between time precision and used resources
- FPGA TDCs are flexible
  - implemented features (not core TDC!) can be easily changed (trigger, windows, scalers, splitters, etc.)
  - new ideas pop up quite often
- Downsides of FPGA TDCs
  - Going to the full potential of the FPGAs (optimization), the development of the TDC-core is very time consuming (same methods as ASIC design)

64 channel time precision distribution for the EraΣor-TDC



Future of FPGA TDCs

Who takes care?

GSI Experiment Electronics Department is committed to continue the development and maintenance of this technology:

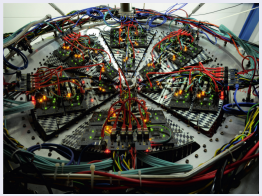
- further improve the performance
  - number of channels, hit rate (dead time), readout speed
  - not focused on time precision as
    - ~10ps sufficient for many applications
    - higher precision easy to get if less channels/FPGA are acceptable
- well documented designs for long term usability

Applications

How can we use it?

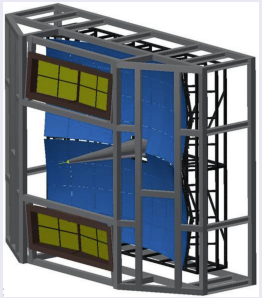
Team for a total of 100k channels and more...

HADES-RICH



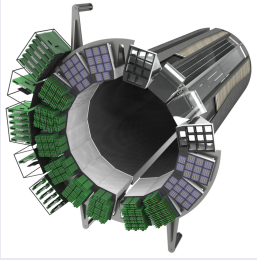
- 27k channels MA-PMT
- existing detector
- production beam time in March 2019

CBM-RICH



- ~56k channels MA-PMT

PANDA-Barrel-DIRC



- ~11k channels MCP-PMT
- smaller signals

TRB Collaboration

Team of ∼8 developers (hard and software)

FPGA-TDCs: New Developments at GSI

EraΣor-TDC: Main Features

- Second generation of TDL-based FPGA-TDC
- Project status: design finished, implementation in progress, partially simulated – preliminary specs!
- Lowest-cost platform: Lattice ECP5 (150k LUTs), less than 20€ per chip
- 48+1 Channels: 11ps RMS time precision
- Parallel operation of channels: reduce deadtime or increase time precision
- Additional sampling-TDC with ~1.2GSamples/s
- Additional trace buffer (48-Channel logic analyzer)
- Fast 32-bit pulse counter per channel
- 40-bit Timestamps
- speed optimized readout

A Selection of Design Principles

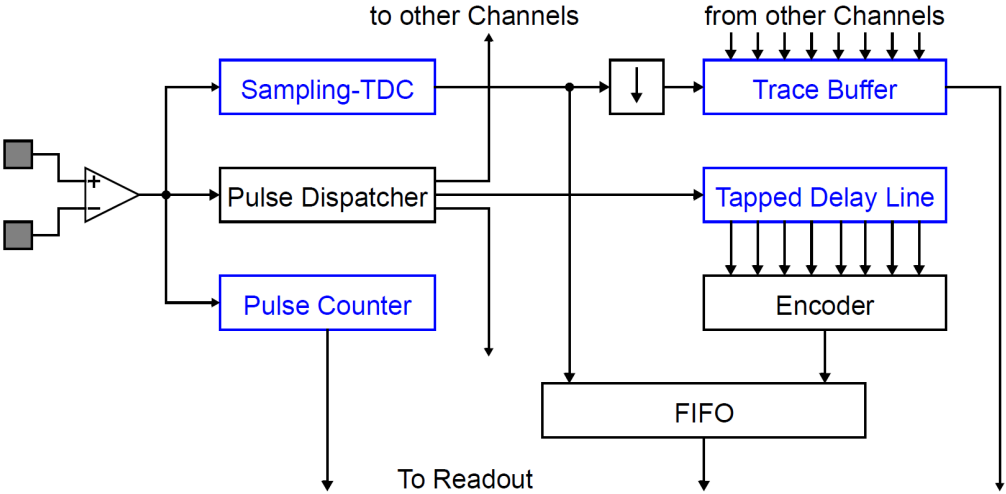
- Sampling-TDC and trace buffer
- Pulse dispatcher
- Encoder based on population count
- On-the-fly obsolete hit elimination
- On-the-fly fine time calibration

Versatile Measurement Instrument (I)

Four Measurement Units

- TDL-based TDC
- Sampling-TDC
- Trace buffer
- Pulse counter

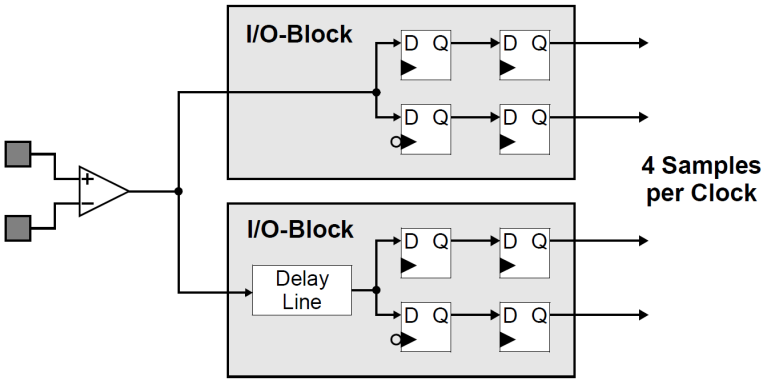
Versatile Measurement Instrument (II)

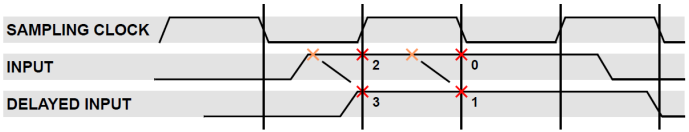


Sampling TDC (I)

- Use fast DDR-FFs and Delay Lines in IO-Blocks (usually used for DDR memory interfaces)
- Basically for free: uses very little fabric resources
- By shifting the input signals, high effective sampling rates can be achieved at low system clock rates
- 1.2GSamples/s (could be increased to 2.4GSamples/s with different board layout) @300MHz
- Continuous sampling, storage only when hit detected
- Deadtime-free TDC
- Usage: detect transitions during TDL deadtime; fall-back when TDL is used by sibling channel to compensate channel loss (always 48 Channels)

Sampling TDC (II)

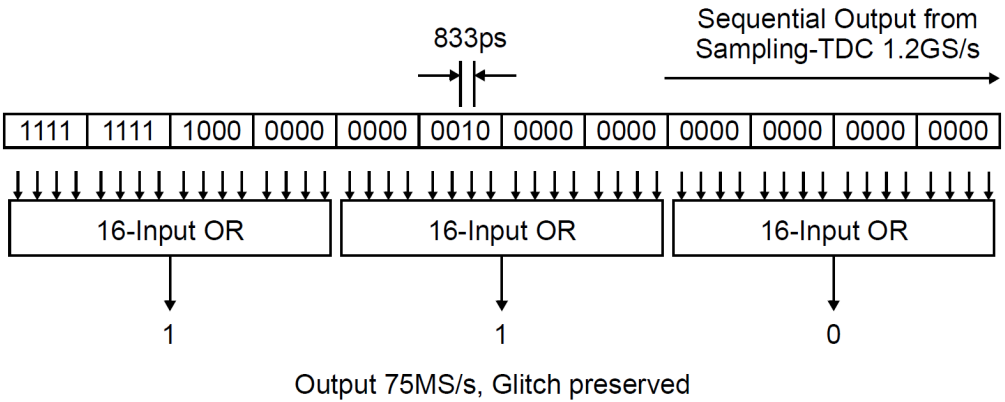




Trace Buffer (I)

- Continuously stores the samples from the sampling-TDC of all channels
- Stops when reference time signal arrives
- Think of it as a logic analyzer (only external trigger)
- Downsampling factor of 4, 8, 16 or 32
- Logical OR as downsampling filter will catch short pulses
- Buffer depth: 1k samples
- Maximum record length: 29μ
- example: for the HADES experiment: Logic Analyzer with 27,000 channels
- Usage: Detector and FEE debugging without DAQ software

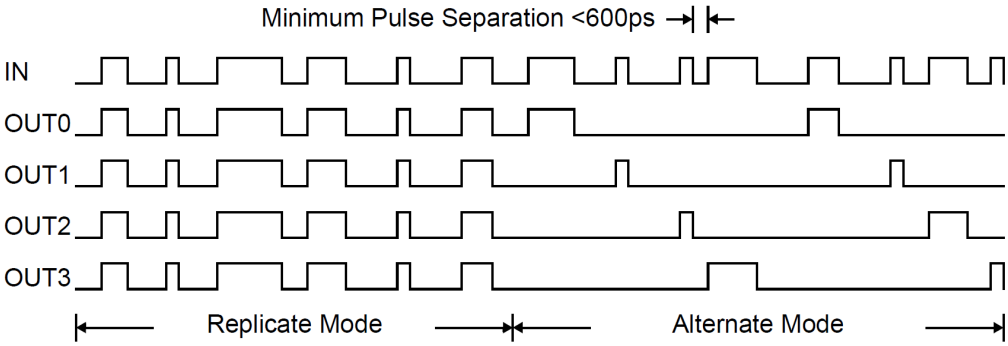
Trace Buffer (II)



Pulse Dispatcher (I)

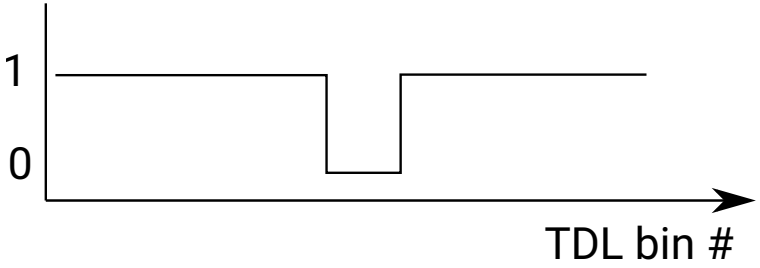
- Can either replicate the signal or send pulses alternatingly to 2 or 4 channels
- Can easily be extended to a higher number of channels
- Minimum required pulse separation: <600ps (from simulations)
- Usage: reduce deadtime or separate glitches from true pulses

Pulse Dispatcher (II)



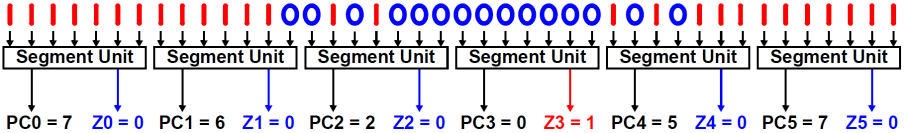
TDL and Encoder (I)

- TDL: standard carry-chain of 224 full adders
- Wave Union for higher precision: one travelling low-pulse (two transitions)
- population count encoder for elimination of bubble degradation
- problem: wave union and population count encoder cannot be combined so easily
  - population count is constant in first approximation



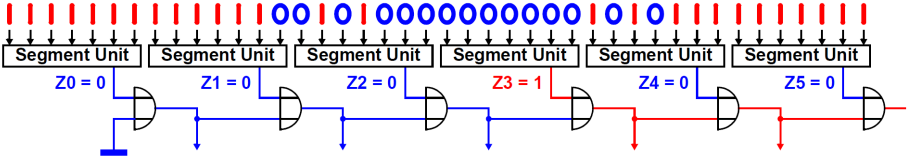
TDL and Encoder (II)

- Solution: divide TDL in segments, compute individual population count and set a flag if segment is entirely zero.



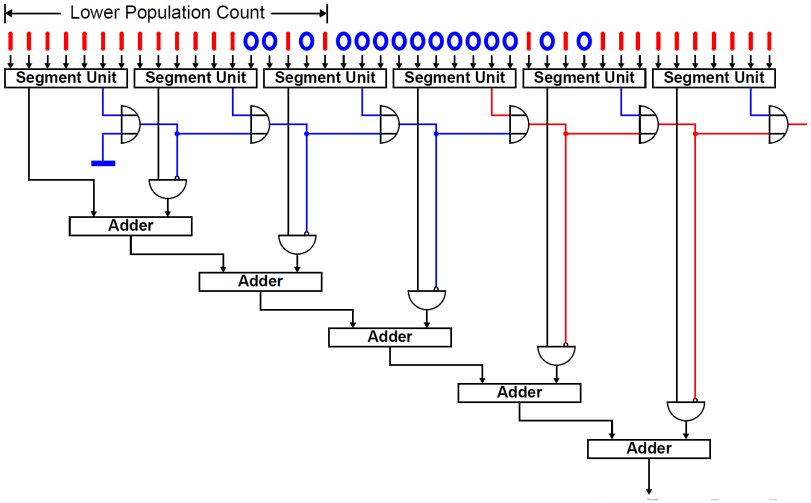
TDL and Encoder (III)

- Use this flag in a combinational chain to mark all upper bits as invalid.



TDL and Encoder (IV)

- Build a conditional adder tree to compute the population count only up to the pulse.

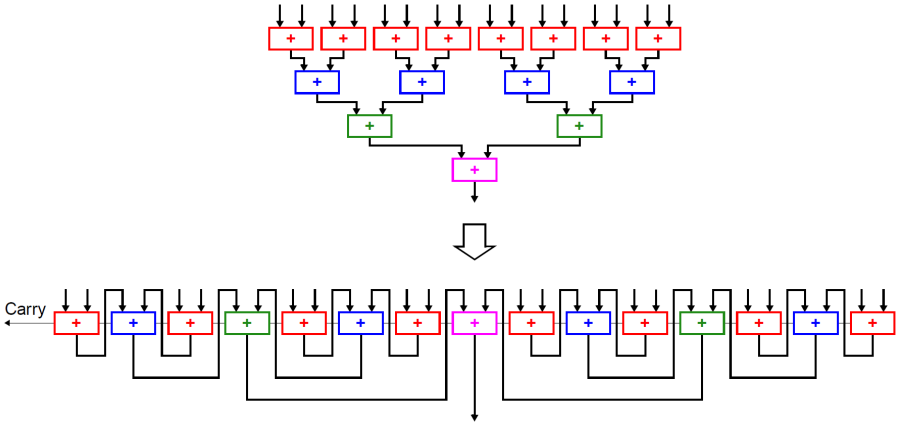


TDL and Encoder (V)

- Build a second adder tree to unconditionally count the number of zeros across the TDL bits.
- The fine time is then 2 * „Lower Population Count“ + „Zero Population Count“.
- Two pipelined adder trees can perform one measurement per clock.

TDL and Encoder (VI)

- An adder tree can be transformed into a large ripple carry adder.



TDL and Encoder (VII)

- The entire encoder has been implemented as 3 ultra-wide ripple carry adders.
- Together with the TDL, these are 4 ultra-wide carry chains which allow a very compact implementation.
- The floorplan of the TDL-Encoder-Combo occupies 104 PFUs with 832 LUTs. Of these, 832 are used.
- 100% Utilization

On-the-Fly Obsolete Hit Elimination

- Applies to triggered systems that use a trigger window.
- When a trigger is received, the timestamp of each hit must be compared to the trigger window boundaries.
- For performance reasons, each channel has its own trigger window comparator.
- IDEA: use this comparator permanently and discard hits that drop out of the trigger window (idea contributed by Jan Michel, Frankfurt University)
- When a subsequent trigger arrives, overhead is reduced because all hits behind the trigger window have already been read from the FIFO and discarded.

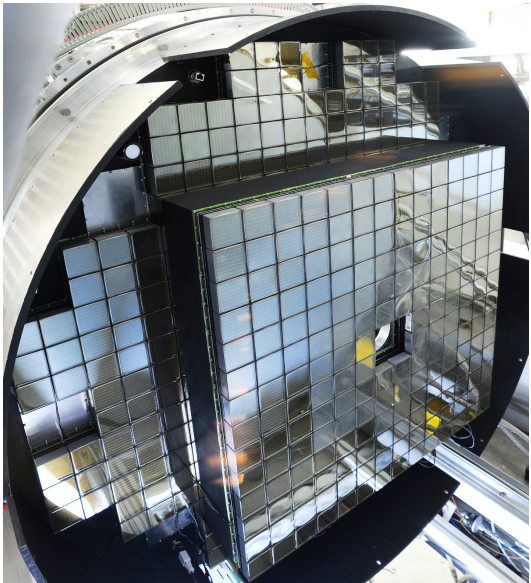
On-the-Fly Fine Time Calibration

- calibration in software: huge number (for many channels) of table look-ups can present a performance problem (LVL1 cache)
- Therefore calibration (Bin Number $\rightarrow$ Fine Time) is done in hardware using BlockRAMs
- When done centralized (at DAQ interface), tables can be efficiently packed in BlockRAMs
- 4 tables per BlockRAM, 48 channels require only 12 BlockRAMs
- Calibration is done at full readout-speed, no performance reduction
- Tables are computed externally in software to limit hardware costs

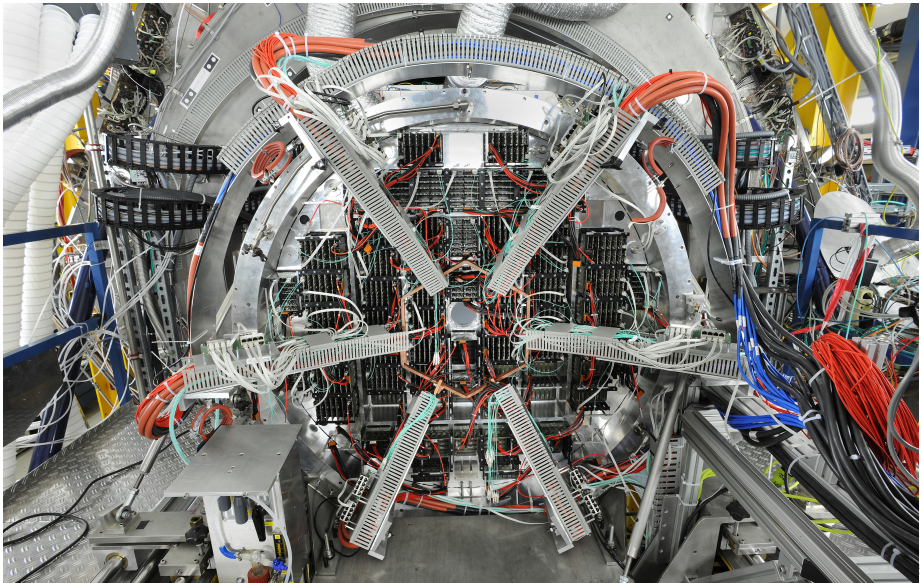
EraΣer TDC Summary

- We presented our current TDC Project called EraΣer
- A selection of design principles and tricks have been dicussed that enable a fully-featured second generation measurement system to be integrated on a lowest-cost FPGA
- Where can we apply it?

HADES RICH Detector: 428 PMTS, each 64 channels



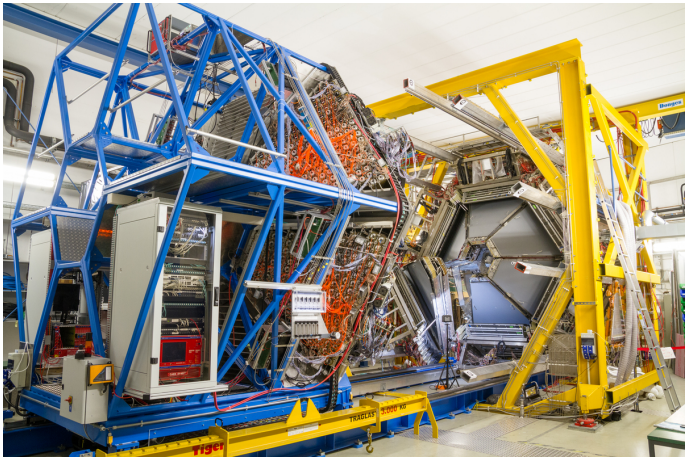
HADES RICH Detector: DiRICH Electronics for 27k channels



Summary I

- The FPGA-TDCs (with its associated TRBNet + DAQ) is a mature platform (hardware and software) useful for many applications
  - Collaboration takes care of constant development and maintenance
- based on the "come-and-kiss" principle
  - avoid hard to acquire ASICs
  - due to modern commercial components (small, cheap, low-power) now closer to the ASIC domain
- DiRICH-system proved to work very well in production beam time
- MA-PMT and MCP-PMT applications (and beyond that) are quite common and we can share the achievements and effort to develop and maintain it
- 60k channels for CBM-RICH will be built starting this year
- many more applications: PANDA barrel DIRC, PANDA F-RICH, etc.

Summary II



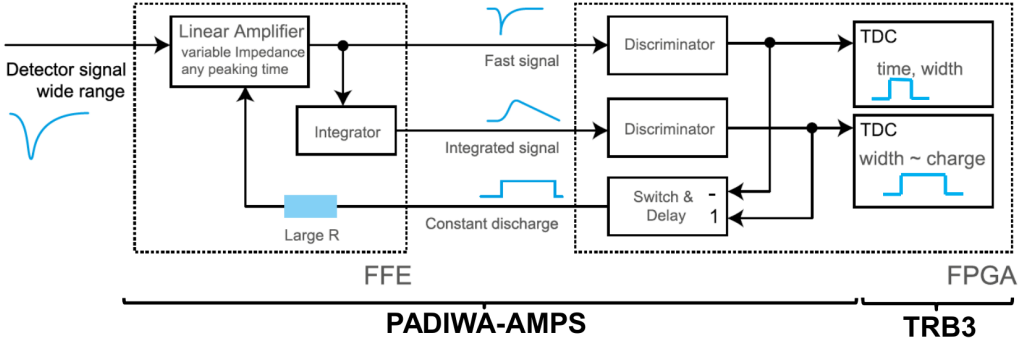
- The HADES detector-system uses only TDCs for analog to digital conversion, including the Electromagnetic Calorimeter.

Summary

- Thank you for your attention!

Backup

FPGA-TDC: Charge Measurement



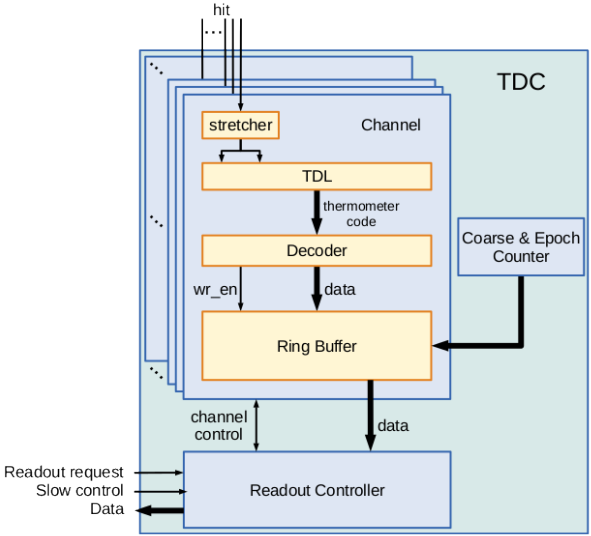
Modified Wilkinson ADC:

- "Come-and-Kiss"-principe: Commercial of the shelf and keep it small and simple.
- Input signal is integrated with a capacitor
- Capacitor is discharged using a constant current source triggered by the input signal

Basic Operation of an FPGA-TDC

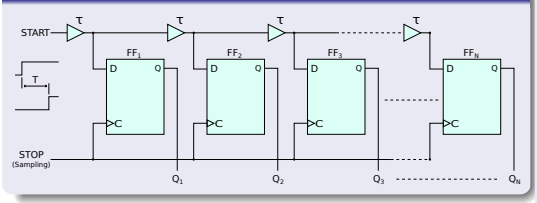
features

- Coarse & Epoch counters for long measurement range
- Tapped Delay Line for fine time interpolator
- Stretcher for measuring the traling edge in the same channel
- Decoder: thermocode $\rightarrow$ binary
- Ring buffer for the latest hit signals

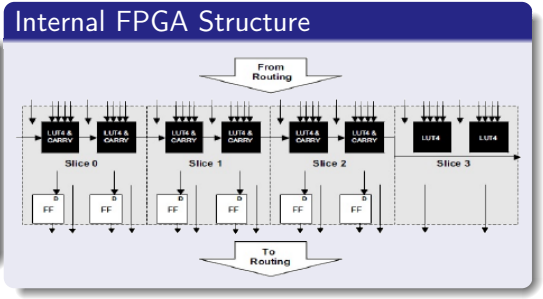


Fine Time Interpolation

Tapped Delay Line



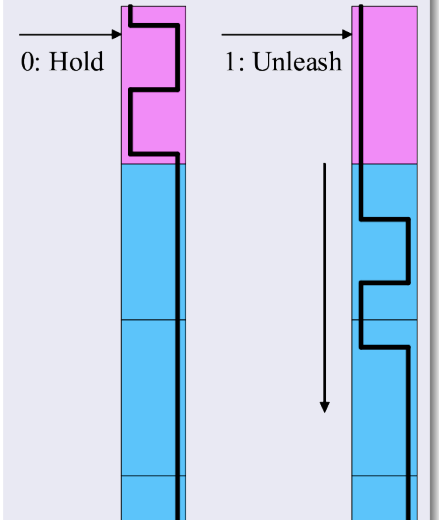
Internal FPGA Structure



- Propagation of the start signal is sampled with the stop signal
- Suits well with the FPGA architecture
- Carry chain for delay line $\rightarrow$ small bin width
- Clock signal as common stop signal $\rightarrow$ minimal skew
- Coarse & Epoch counters $\rightarrow$ $\sim$45 minutes measurement range

FPGA-TDC: Further improvements

Wave Union Launcher



- Non-uniform intrinsic delays → Ultra wide bins
- the precision of the TDC is reduced
- Wave Union Launcher [Jinyuan Wu]:
  - send many transitions to the delay line, when a hit signal arrives, thereby increase the number of measurements on the delay line and even out ultra wide bins (UWB)

FPGA-TDCs: Bin Width (DNL)

- Non-linearities caused by non-uniform intrinsic delays
- UWBs increase non-linearities
- WUL averages the locations of the transition on the delay line, thus dividing the UWBs
- Max bw: 45ps $\rightarrow$ 35ps
- Avg bw: 20ps $\rightarrow$ 10ps
- Calibration of the TDC further decreases the non-linearity