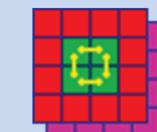
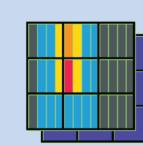


The phase-1 upgrade of the ATLAS **Level-1 Calorimeter Trigger** On behalf of the ATLAS collaboration

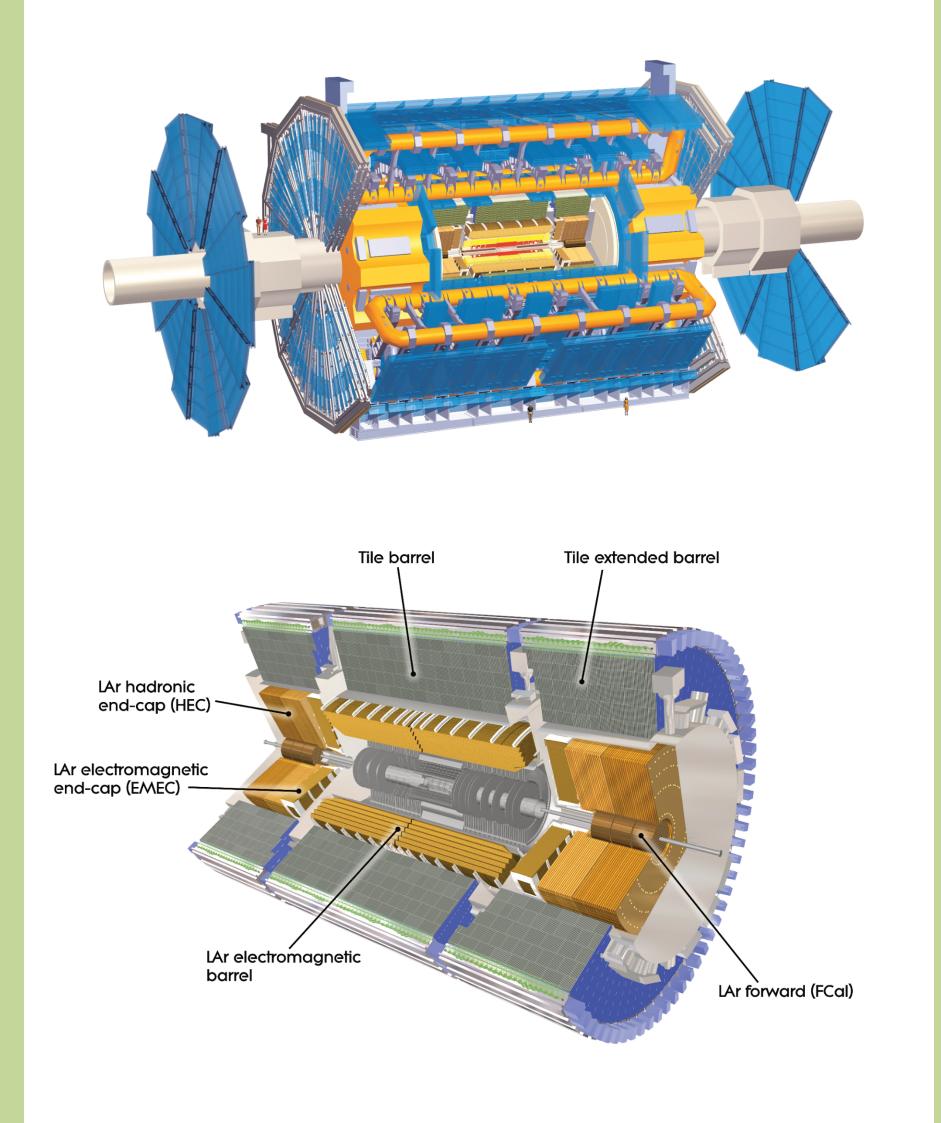


Yuri ERMOLINE Michigan State University



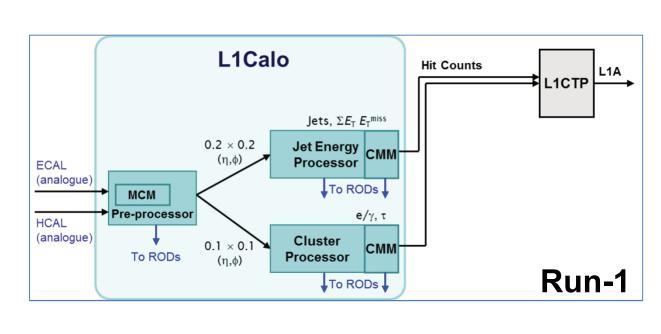
Abstract

The ATLAS Level-1 Calorimeter Trigger (L1Calo) is a hardware-based system that identifies events containing calorimeter-based physics objects, including electrons, photons, taus, jets, and missing transverse energy. In preparation for Run 3, when the LHC will run at higher energy and instantaneous luminosity, L1Calo is currently implementing a significant programme of planned upgrades. The existing hardware will be replaced by a new system of feature extractor (FEX) modules, which will process finer-granularity information from the calorimeters and execute more sophisticated algorithms to identify physics objects; these upgrades will permit better performance in a challenging high-luminosity and high-pileup environment.

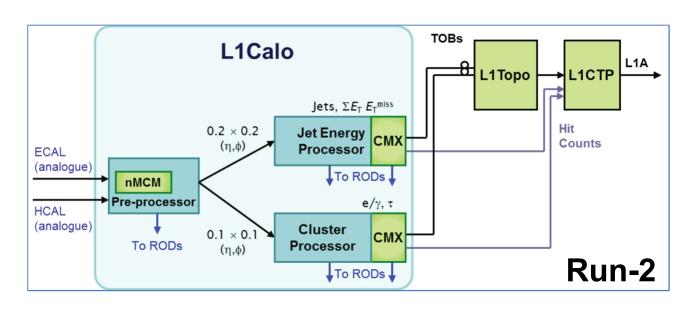


ATLAS Level-1 Calorimeter Trigger system evolution

L1Calo is a pipe-lined system processing signals from the liquid-argon and tile calorimeters and provides trigger signals to the Central Trigger Processor (CTP). Since the start of the ATLAS operation, the initial L1Calo system underwent several important upgrades.



- Multi-Chip Module (MCM) with preprocessing ASIC replaced by new, FPGAbased version (nMCM).
- Cluster Processor (CP) and Jet Energy Processor (JEP) calculate and send trigger objects in addition to simple counts
- New L1Topo module for topology-based decisions uses trigger objects and forwards the result to the CTP.



<u>Y26</u>

48 x 48w

eFEX

Crate 0

48 x 48w

eFEX

Crate 1

132 x 48w

12.0m + 0.5m

4.0m + 0.5m

Y27

6 x 48w

gFEX

Crate

30 x 48w

iFEX

Crate

LArFOX B

LArFOX D TileFOX F

TileFOX E

LArFOX A

LArFOX C

<u>Y28</u>

40 x 48w

Crate1

DPS

Crate 2

Crate 3

116 x 48w

24 x 48w

<u>Y29</u>

40 x 48w

36 x 48w

PC (FE-Felix)

PC (FE-Felix)

PC (FE-Felix)

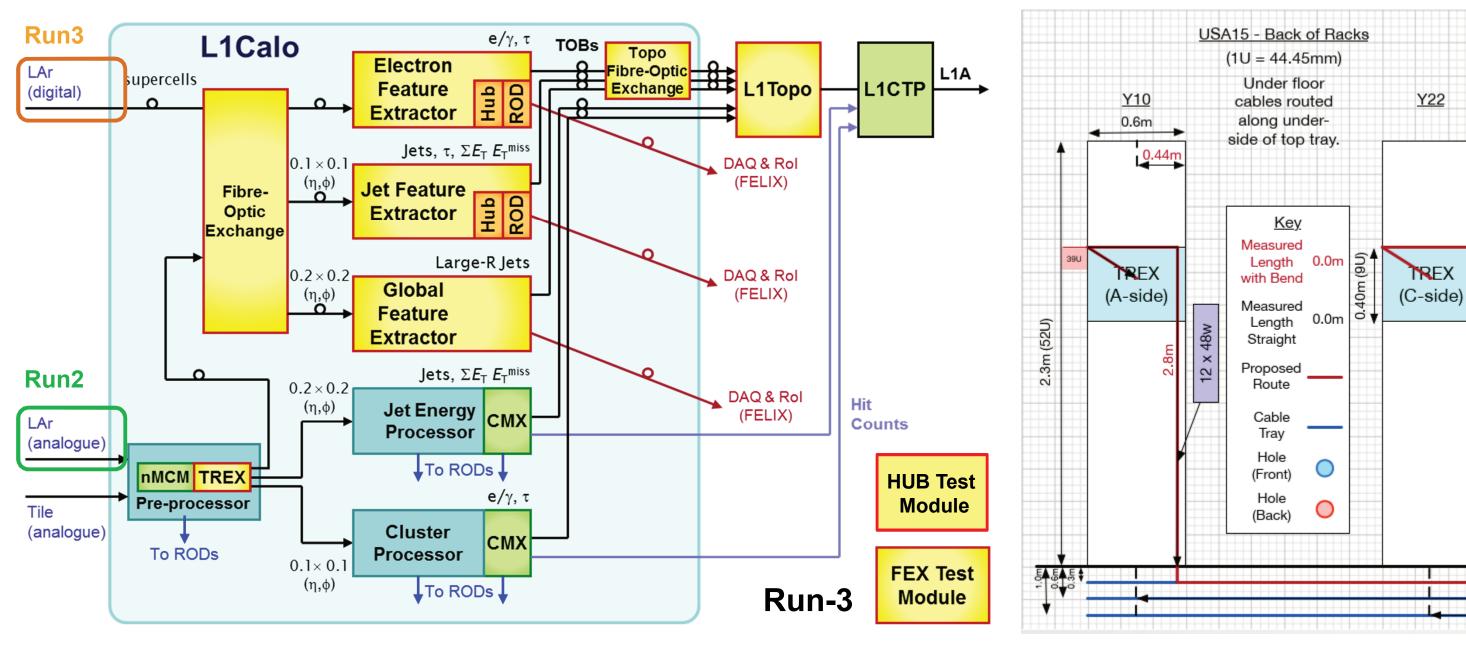
PC (FE-Felix)

PC (FE-Felix)

PC (FE-Felix)

PC (FF-Felix

The ATLAS experiment is planning an upgrade to the TDAQ system for the Phase-I period (Run-3, from 2021 to 2024) to address the new challenging accelerator machine conditions, namely an increase in luminosity to ~2.5E34/cm²s and to maintain the sensitivity to electroweak physics without being affected by the increased number of pile-up events. The upgraded system makes use of higher granularity and runs better-performing trigger algorithms than currently employed.



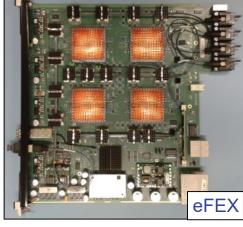
- Three new Feature EXtractor (FEX) systems: electron FEX, jet FEX and global FEX (identifies large jets).
- The digitised data will be distributed by a new Fibre Optical eXchange plant (FOX).
- New Tile Rear EXtension (TREX), provides the Tile digitised results to the FEX processors as well as to CP and JEP.
- The current legacy system will initially run in parallel and will be decommissioned after the performance of the FEX processors has been validated.

Preparation in progress: from drawing to cable installation...



Input data and algorithm (*jFEX* example)

Firmware development (eFEX example)



eFEX: isolated $e/\gamma \& \tau$ candidates **jFEX**: jets (& large τ), Σ ET, ETmiss gFEX: large radius jets, ETmiss, centrality, etc.

Feature Extractors (FEX)

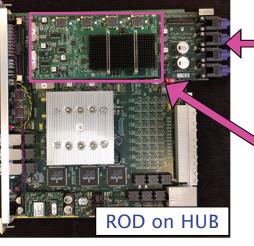
Systems with similar characteristics:

- ATCA modules with FPGAs
- Large optical input bandwidth
- Large processing capacity

eFEXjFEXgFEXNo. ATCA modules2461Processing FPGAs per module4 Virtex74 Ultrascale+3 Virtex Ultrascale+Control EPGA/SoCVirtex7Zynq Ultrascale+ (UltraZed)Zynq Ultrascale+				
modules4 Virtex74 Ultrascale+3 Virtex Ultrascale+Processing FPGAs per module4 Virtex72ynq Ultrascale+2ynq Ultrascale+ControlVirtex7Zynq Ultrascale+Zynq Ultrascale+		eFEX	jFEX	gFEX
FPGAs per module Ultrascale+ Control Virtex7 Zynq Ultrascale+		24	6	1
	FPGAs per	4 Virtex7	4 Ultrascale+	
(Ontrazed)	Control FPGA/SoC	Virtex7	Zynq Ultrascale+ (UltraZed)	Zynq Ultrascale+
MiniPods 17 24 35	MiniPods	17	24	35
No. Links at 11.2 424 536 492 Gb/s		424	536	492
PCB 22 layer 24 layer 30 layer	РСВ	22 layer	24 layer	30 layer

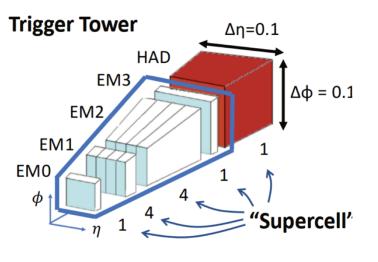


TREX: VME rear transition module in Pre-Processor Module (PPM) provides the Tile digitised results to the FEX processors and maintain the legacy trigger path to CP and JEP systems.



IUB: Control and clock hub in e/jFEX and L1Topo ATCA shelves

The inputs to the L1Calo in Run-2 are Trigger Towers (TT) that are formed by analogue summation of calorimeter cells across the longitudinal layers in a region of $\Delta \eta \times \Delta \phi = 0.1 \times 0.1$. The Phase-1 upgrade increases the granularity of the LAr trigger inputs to ten Super Cells per trigger tower as shown:

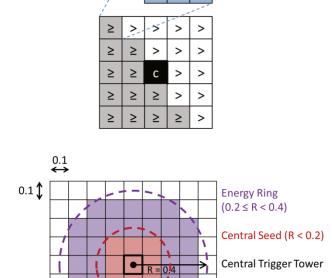


Super Cells allow These L1Calo improvements of algorithms in eFEX and jFEX. Coarse granularity also available for gFEX to enable the processing of the full calorimeter in a single ATCA module.

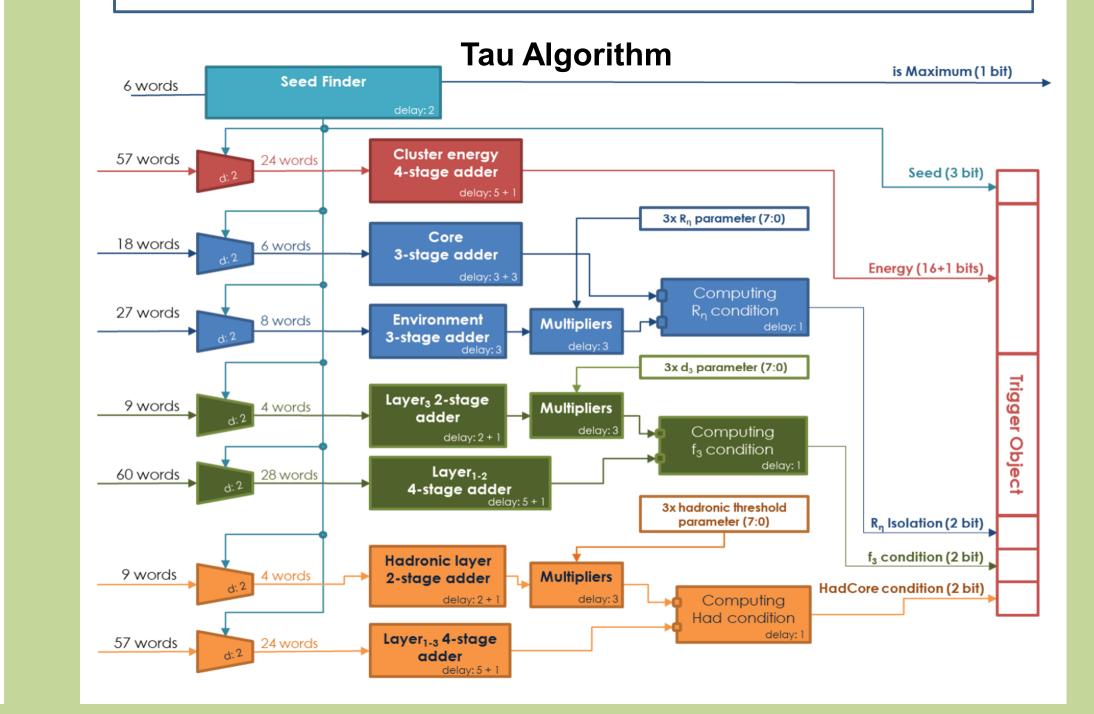
Seed:

Small-R jets on jFEX (sliding window):

- Seeding jets: seeds from 3x3 jets, energy sum from nine TT with a configurable threshold
- One local maximum in 5x5 window
- Building "round" jets within a radius of 0.4 around central TT in the seed

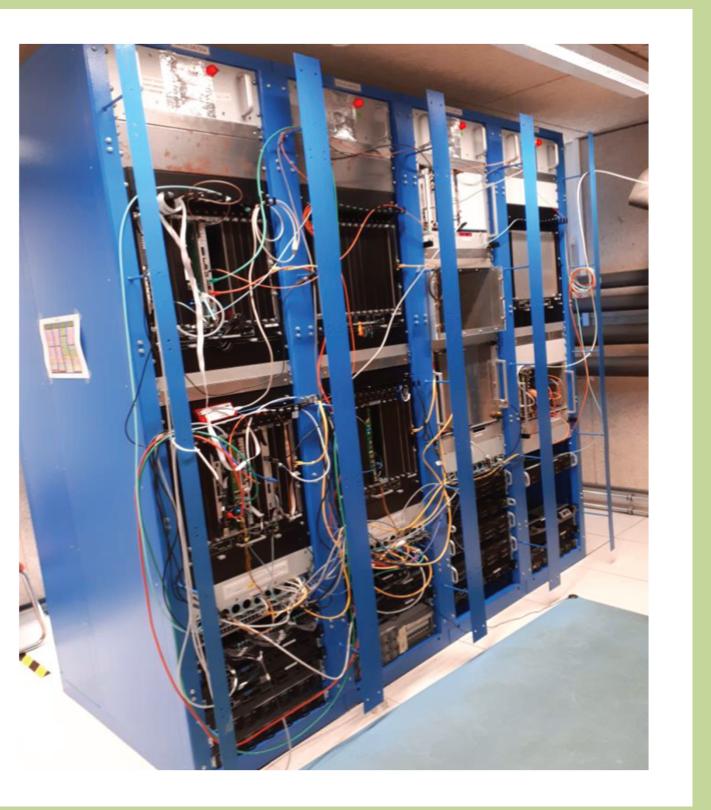


From LAr e/γ Algo😳 Dynamic MGT Local sorting Mappin Tau Alg 😐 threshold Real-time data path _ _ _ _ _ _ _ _ _ _ _ _ _ To L1Topo Playback TOB Tx Global Output Protoc sorting RAM 💽 monitorin

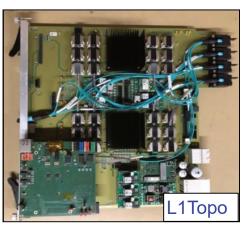


TDAQ Surface Test Facility (STF)

Aimed to perform as many tests as possible for each module before final commissioning: full functionality demonstrated within system

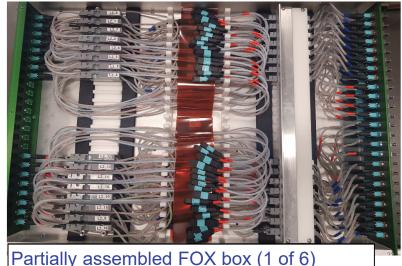


ROD: ReadOut Driver, collects & buffers data across shelves and transmits them to DAQ system

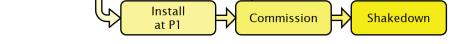


L1Topo: Re-design of Run-1 Topo based on jFEX hardware: 3 ATCA modules with 2 Xilinx Ultrascale+ FPGAs per module. x3 processing power of current Topo

FOX & TopoFOX: Fibre mapping



	FOX	ТороFOX
Mapping from/to	Calorimeters to FEXs	FEX & Muon trigger to L1Topo
No. fibres	~7500	~1500
Housing	6 x 2U boxes	1 x 2U box
No. assemblies	206	57
Assembly types	31	5



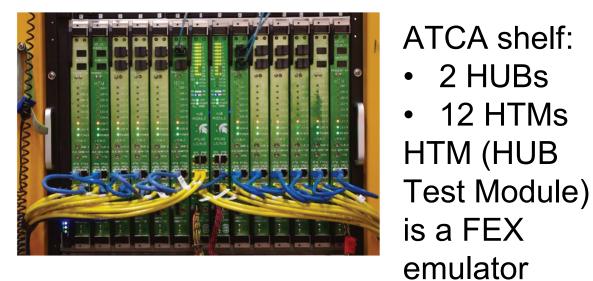
Individual module test example:

Individual Module Tests

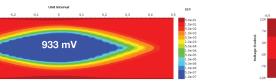
University of Birmingham

L1Calo commissioning

System tests at STF



MGT link stability as a function of drive voltage (max ~933 mV, min ~191 mV).



Margin of ~5 in voltage attenuation

- Build vertical slice through system
- Internal L1Calo system-level tests
- Integrate with neighbouring systems
- Soak tests with bit-wise simulation
- 4 CERN standard ATCA shelves for jFEX, eFEX/gFEX, Topo, LAr, Muon trigger
- VME Crate for PPM (TREX, 9U) and TTC (Timing and Trigger Control, 6U)
- DAQ (FELIX + SW ROD)
- Legacy DCS for PPMs (TREX)
- DCS machine from Central DCS for ATCA

BROCKHAVEN NATIONAL LABORATORY NATIONAL LABORATORY University of Cambridge University of Chicago University of Chicago

• In use for tests since Feb'19

International Conference on Instrumentation for Colliding Beam Physics (INSTR20), 24 - 28 February, 2020, BINP, Novosibirsk, Russia