Design of Prototype Front-End Electronics for the Gamma-Gamma Collider

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1. Introduction

The Gamma-Gamma collider proposed by Institute of High Energy Physics (IHEP) is under discussion in China. The high-energy electron beams (~200 MeV) generated by a linear electron accelerator are divided into two arcs, and then brought into a head-on collision at the interaction point (IP). A high-intensity laser beam is illuminated to the electron beams at the conversion points (CP) shortly before they cross the IP, and the procedure can generate target gamma beams (1-2 MeV) based on Compton back-scattering. Finally, the γ beams collide at the IP. The planned structure of the $\gamma\gamma$ collider facility is shown in Fig. 1.

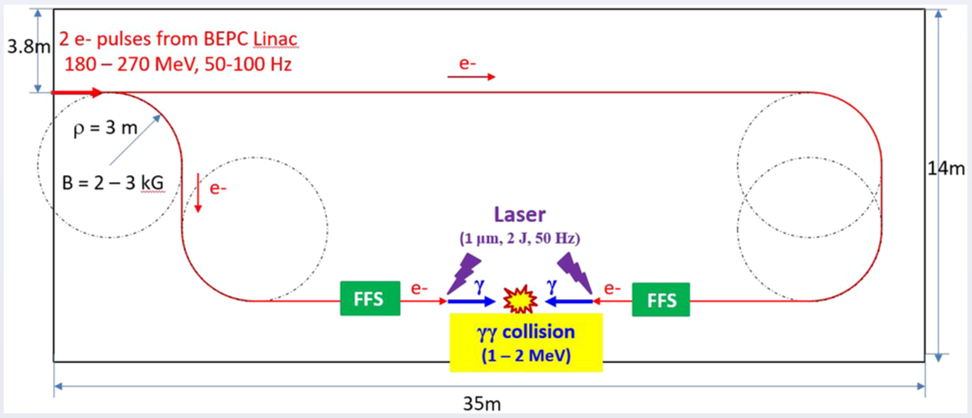

Fig. 1. A planned structure of the Gamma-Gamma collider facility.

The unique experiments on the gamma-gamma collision of 1-2 MeV cross section include $\gamma\gamma$ scattering and Breit–Wheeler pair production. These physical interactions are predicted but still not observed in laboratory, thus the development of the low-energy Gamma-Gamma collider is of great significance. The collision products and background particles are photon, electron and positron, and they are all collected by CsI(Na) scintillators and plastic scintillators, and then converted into electric signals by silicon photomultiplier (SiPM). To measure the output electric signals of the detectors, an electronics system is in progress.

2. Readout Requirements

In the $\gamma\gamma$ collider, all the detectors are placed in the vacuum chamber around the collision area for light signals collection. Due to technical limitation of wall perforation and the compact space in the vacuum chamber, the front-end electronics requires high integration inside the chamber, which results that each board with size of 50 cm×25 cm processes 180-channel analog signals from detectors. The power consumption of the front-end electronics is as low as possible to reduce the heat dissipation in vacuum.

Besides, the remaining requirements of the experiment is as following:

- Pulse width: 30 ns to 2 μs
- Rising edge: 10 ns to 600 ns
- Time resolution: 70 ps (RMS)
- Analog bandwidth : better than 50 MHz
- Sampling rate:1 GSPS

In order to distinguish types of particles, the waveform digitizing technology is applied on the readout electronics. Therefore, it is a good challenge to achieve the design of low noise, high sampling rate and low power consumption.

A readout electronics system composed of front-end electronics and back-end electronics has been put forward for the Gamma-Gamma collider, as shown in Fig. 2. The front-end electronics is comprised of several Front-End Electronics cards (FEEs) with 180 channels on each board. The back-end electronics is one Data Acquisition board (DAQ) to collect all the data from the FEEs.

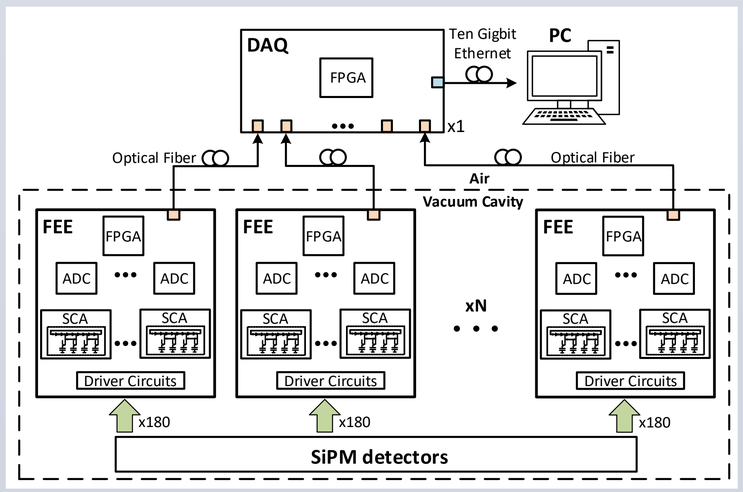

Fig. 2. Architecture of readout electronics system for the Gamma-Gamma collider.

3. Design of the FEE

To reach the design of low power consumption, the FEE uses low-power switch capacitor array (SCA, DRS4) chips and Analog-to-digital converters (ADC) to realize the waveform digitization, as shown in Fig. 3. The DRS4 chip has 8 input channels but only consumes around 110 mW at 1 GSPS sampling rate.

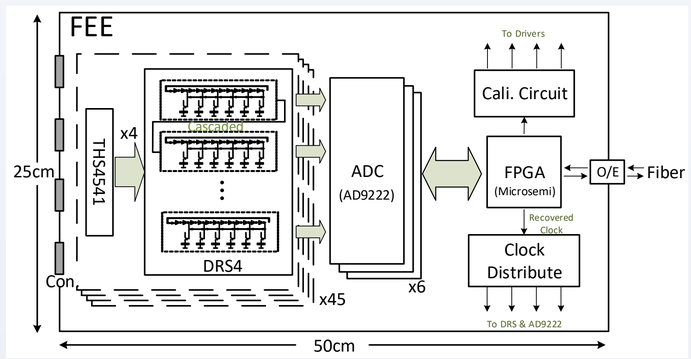

Fig. 3 The diagram of the FEE.

There are 180 differential driver (THS4541) circuits on the FEE serving all signals from SiPMs. 45 DRS4 chips are applied to store analog waveforms at cascading mode and read out the signals at one MUXOUT channel. Then six 12-bit, serial, ADCs (AD9222) with 8 input channels per chip are applied for waveform digitization. Finally, the low-power FPGA IGLOO2 series is used to record digital data and reduce the instantaneous power consumption of the FEE by controlling time-sharing operation of the chips. All the data from the FEE are sent to the DAQ through serial optical links. Fig. 4 shows the photograph of the FEE version 1, and the board with 8 input channels is used to verify the type selection and performance of the chips.

Fig. 4. Photograph of DAQ.

4. Performance

To study the performance of the FEE, the noise and the ENOB were tested in the lab at first. Each sampling cell in the DRS4 chip has a constant offset error, so the calibration waveform was obtained when precision voltage signals were injected into the analog channel. And the noise was sampled with the input floating. After offset correction, the RMS noise of the channels is less than 3 mV, as shown in Fig. 5.

The sine signals provided by the SMA100A generator were sent into the FEE through a low-pass filter. After the analysis of four-parameter sine wave curve-fitting, time interval of the SCA was calculated, as shown in Fig. 6. The ENOB of the channels is better than 6.7 bit when the frequency of input signals is less than 70 MHz.

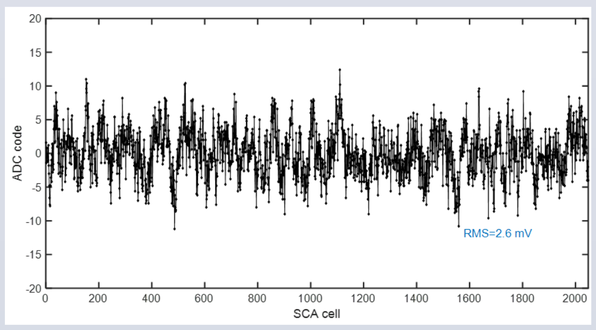

Fig. 5. Noise waveform of one channel on the FEE v1 after offset correction.

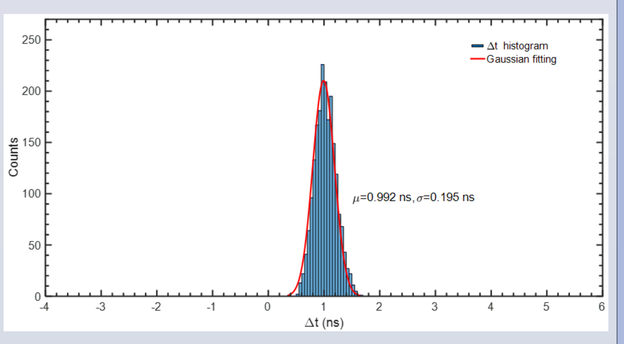

Fig. 6. Time interval histogram of the DRS4 SCA.

To evaluate the performance of the FEE v1 for the experiment, joint-test with the plastic scintillator and SiPM detectors has been conducted. Fig. 8 shows typical plots of the signals deposited by cosmic rays in the detector.

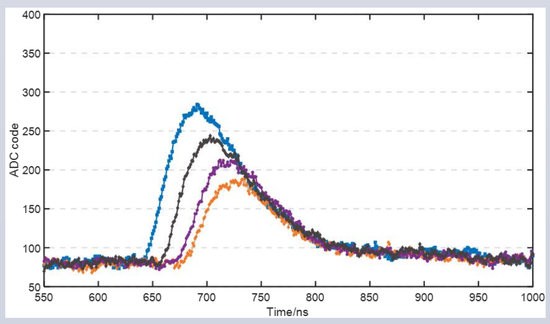

Fig. 8. Typical waveforms of the detector signal in one plastic scintillator strip.

5. Conclusion

The design of the Front-End electronics and the performance of the FEE v1 for the Gamma-Gamma collider are presented in this poster. And the performance of the FEE v1 validated that the design of the front-end electronics meets the requirement of the Gamma-Gamma collider.

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