Signals in the Well Electron Multiplier with the DLC anode (part II)

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Design details

- Dielectric substrate with Copper on one side
- 1st electrode (cathode)
- Well-like hole
- DLC layer (anode)
- 5 Dielectric substrate with Copper on both sides
- 2nd electrode (Copper mesh)
- 7 3rd electrode (strip/pixel readout)

Equivalent diagrams for DLC layer as RC-system

- 2nd electrode (3rd electrode similar). Capacitors normalized to RC-cell (per one hole)
- τ = RC

Input Signal Reconstruction delivered with amplifier Tp=150 ns

- Signals were inverted by amp. in these measurements: 1st electrode (blue) 2nd electrode (green) 3rd electrode (red)
- Reconstruction of the signal in the input done using convolution y(t)=x(t)*h(t) where x(t)=input, h(t)=amp. impulse response (red), y(t) - output (blue), Y(t) - reconstruction (green).
- Assuming that y(t) is composed of h(t) (width 10 ns) and step-function (amplitude 1%) and assuming that T is the end of the input signal we obtain an agreement Y(t) and y(t) within ~10% (green), a. The rise time of Y(t) becomes too large (green), if the h(t) is missing on the input, b.

Five characteristic time intervals

- Below we show 5 characteristic times which define the rate capability of the detector:
  1. 5 mV/div. 200 mV/div
  2. 10 mV/div t=7 ns
  3. 10 mV/div t=10 ns
  4. 5 mV/div t=20 ns
  5. 10 mV/div t=50 ns

Possible application at LHCb M2R1 and M3R1 upgrade (project)

- The LHCb (Large Hadron Collider beauty) experiment is one of eight particle physics detectors experimenting data at the Large Hadron Collider at CERN.
- Rates extrapolated to luminosity $2\times10^{30} \text{cm}^{-2}\text{s}^{-1}$ in the inner-most regions of the LHCb muon detector (Run 4, Run 5)
- 3300 kHz/cm² in M2R1 chambers 1900 kHz/cm² in M3R1 chambers
- In order to minimize efficiency losses at high particle fluxes due to the dead time we propose a solution for M2R1 and M3R1 based on the WELL Electron Multiplier with the DLC anode – a key element of the robust and fast 2D-position sensitive MPG.
- 8-layer M2R1 or M3R1 chamber with narrow gaps (1 mm each).
- Architecture: two 4-layer chambers with digital signals combined by logical OR.
- Within each 4-layer chamber signals are combined by wire OR.
- As foreseen, the existing front-end electronics with Tp=10 ns (CARMAc) has to be saved.

Acknowledgements

The authors would like to thank C. Chicherin and S. Klishkar for mechanical design (PSPI). S.Brabec and SOL Instruments, Minsk, Belarus for the drift-tube measurements the Raman spectral facility (PhTI), Institute of Physics, Acad. Sci. of Belarus, Gatchina for the spectrometric measurements of the WELL detector presented in this work. A.Kashchuk and O.Levitskaya acknowledge the financial support of Russian Ministry of Science, agreement NS-55-2019-1991 then 11.05.2019, unique identification number of project RFBR19-0711300200.