GDL and trigger data readout

TRG/DAQWS@BINP

20160906

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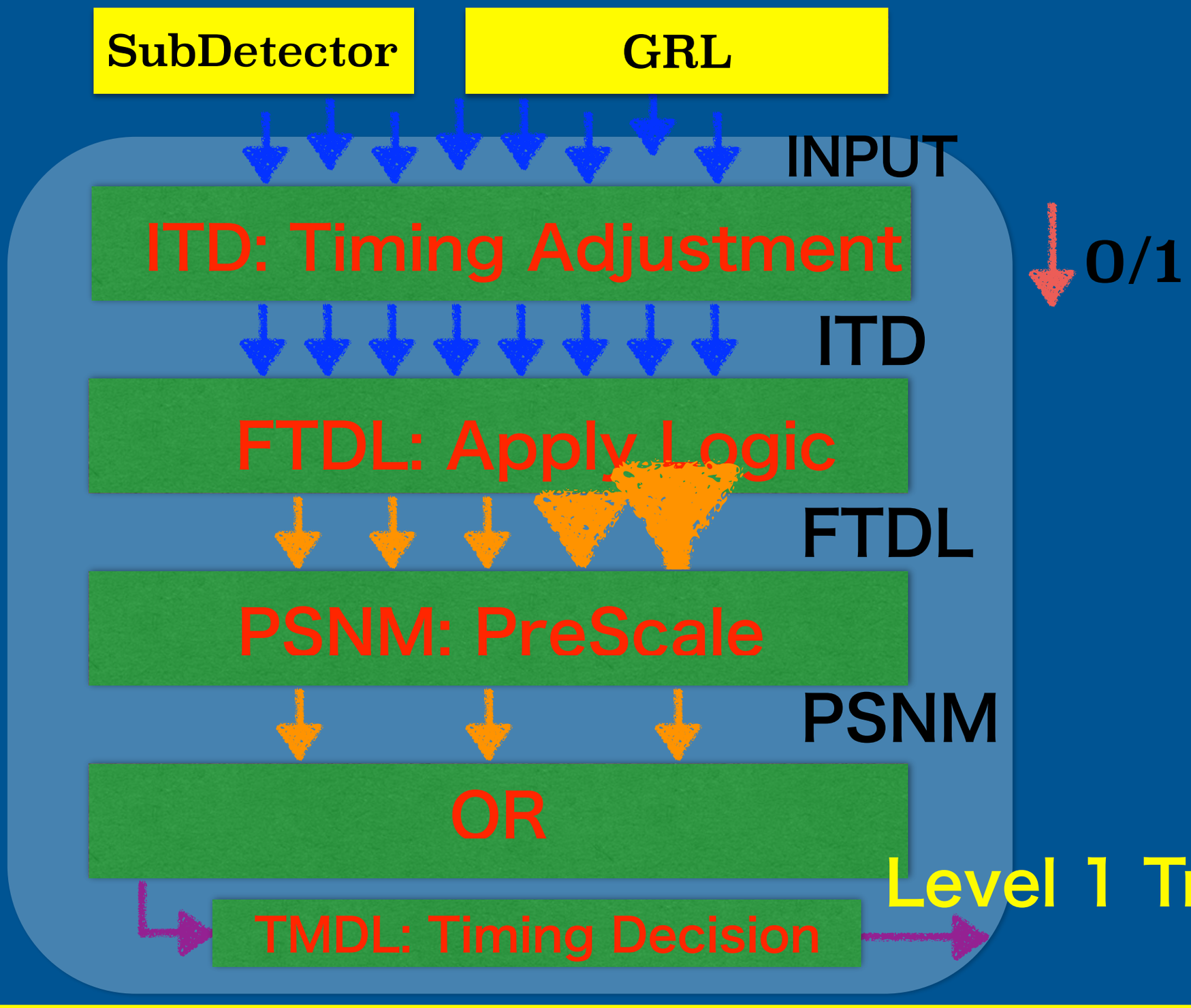
GDL (Global Decision Logic)

- Implemented on UT3 in Ehut, accessible with vmetrg18



ut bits from subtrigger 1

	nbits	name	
CDC	3	n_t3_full	#of 3D full tracks
	3	n_t3_short	#of 3D short tracks
	3	n_t2_full	#of 2D full tracks
	3	n_t2_shoft	#of 2D short tracks
	1	cdc_bb	back-to-back topology
	1	cdc_open45	45 deg opening angle
	3	cdc_timing	timing signal
ECL	1	e_high	1 GeV or more
	1	e_low	0.5 GeV or more
	1	e_lum	3 GeV or more
	1	ecl_bha	Bhabha
	11	bha_type	Identified as Bhabha
	4	n_clus	# of cluster
	1	ecl_timing	timing signal

ut bits from subtrigger 1

	nbits	name	
TOP	3	n_hits	# of top hits
	1	top_bb	back-to-back topology
	1	top_active	Top Timing active
	3	top_timing	Top Timing
KLM	3	n_klm	# of klm hits
Random	1	revo	
	2	rand	
	3	bhabha_delay	

Logic (FTDL and PSNM bits)

v0.02

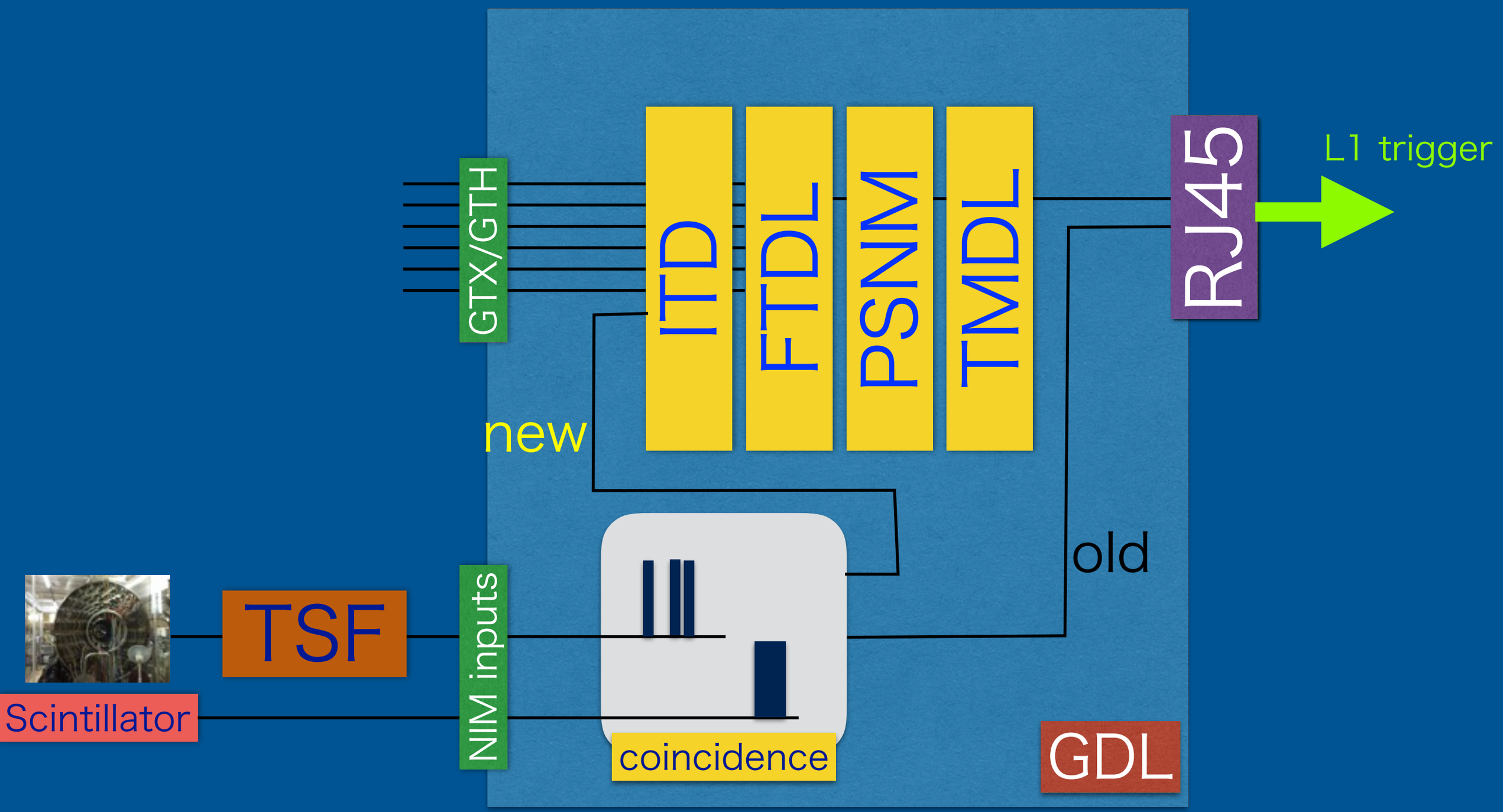
	PS	Logic = algorithm
3 3D tracks	1	zzx = (n_t3_full >= 2) & (n_t3_short >= 3)
3 2D tracks	1	ffs = (n_t2_fu ll >= 2) & (n_t2_short >= 3)
1 GeV or more	1	hie = e_high & (! bhabha)
4 clusters	1	c4 = n_clus >= 4
LowMult	1	zx = (n_t3_full >= 1) & (n_t3_short >= 2) & (! bhabha)
	1	fs = (n_t2_full >= 1) & (n_t2_short >= 2) & (! bhabha)
Bhabha	50	bha = bhabha
	50	bhatrk = e_lum & (n_t2_short == 2)
ee → $\gamma\gamma$	10	gg = bhabha & (n_t2_short == 0)
mu pair	1	mupair = (n_t2_short == 2) & (n_klm == 2)
random	1	revolution = revo
	1	random = rand
	1	bg = bhabha_delay

PS = prescale
FTDL = Final Trigger Decision Logic
PSNM = FTDL after prescale

GDL Firmware updates

- ✓ ITD
  - ✓ Function to extend input signal length added
    - ✓ Needed to take coincidence in FTD
      - ✓ GDL receives rising edge timing only
    - ✓ Different valid signal widths for each input
    - ✓ Controlled via VME
- ✓ TMDL
  - ✓ BUSY signal length changeable via VME
    - ✓ 200 nsec requirement by DAQ
    - ✓ ~500 nsec maximum variation of TSF signal

CDC Cosmic Ray Test



GDL Monitor

trgadmin@vmetrg18:~/n — ssh -XY bdaq.local.kek.jp — 151×18

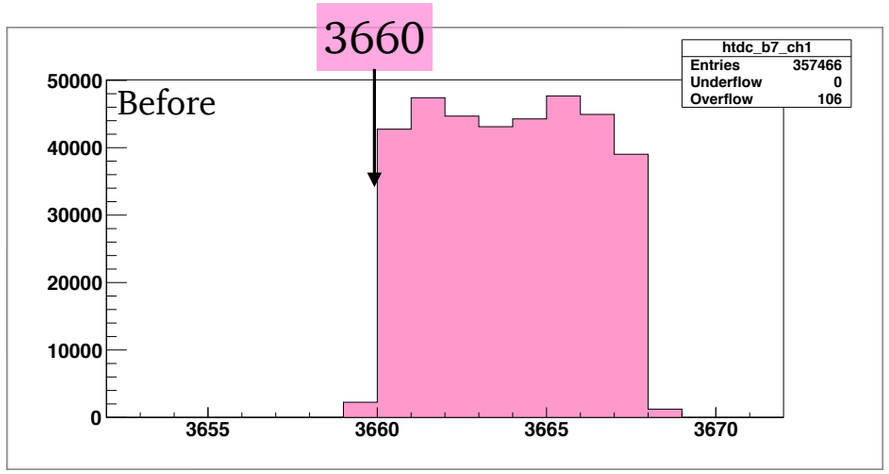
trgadmin@vmetrg18:~/n — ssh -XY bdaq.local.kek.jp

```
Clock counter: 0x00002749-a219cbd4, running about 3 day 22 hrs 28 min 55 sec

FTD    3
GDL    2016_0829_1255_08
ITD    ftd/data/itd_0001.dat
PSNM   ftd/data/psn_0003.dat
DAS    ftd/data/das_0001.dat
RANDOM ftd/data/rnd_0001.dat


 0 zzx                0,        0,        0  |  6 bhabha            0,        0,        0  | 12 bg                0,        0,        0
 1 ffs                0,        0,        0  |  7 bhabha_trk        0,        0,        0  | 13 nim0              0,        0,        0
 2 zx                 0,        0,        0  |  8 gg                0,        0,        0  | 14 nim1              0,        0,        0
 3 fs                 0,        0,        0  |  9 mu_pair           0,        0,        0  | 15 nim2              0,        0,        0
 4 hie                0,       70,        0  | 10 revolution        0,      110,        0  | 16 crtout            1,   970318,        0
 5 c4                 0,        0,        0  | 11 random            0,        0,        0  |
```

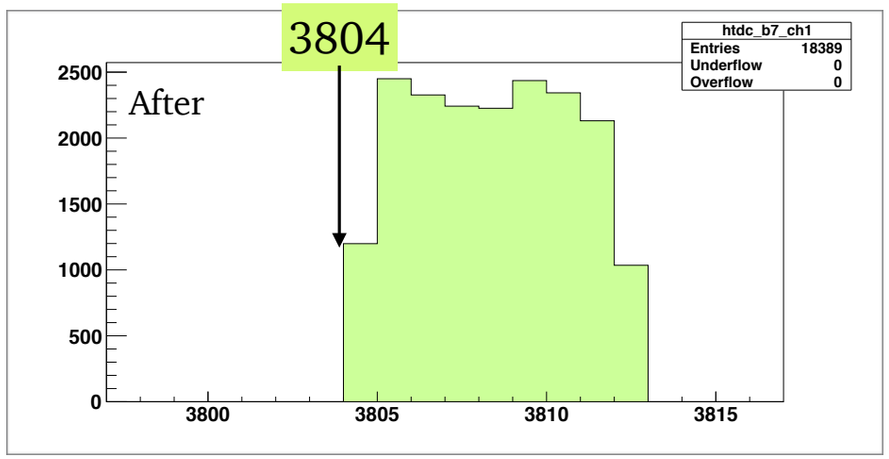
PSNM

CDC CRT; GDL Latency

Nanae Taniguchi (160829)



additional delay = 144 count ~ 144 nsec



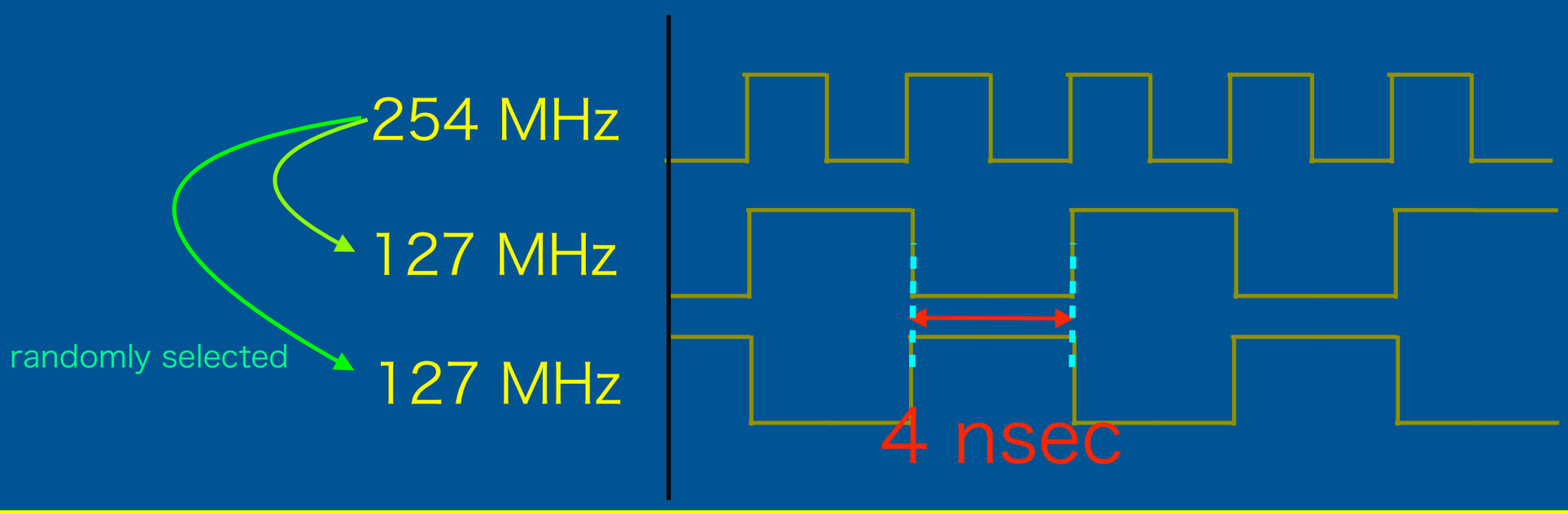
1st "real data" taken with L1 from GDL components

- ✓ **96 nsec for TMDL time window**
- ✓ **Study needed to select proper time window length**

CDC CRT; Timing Shift Problem

Y. Iwasaki/N. Taniguchi

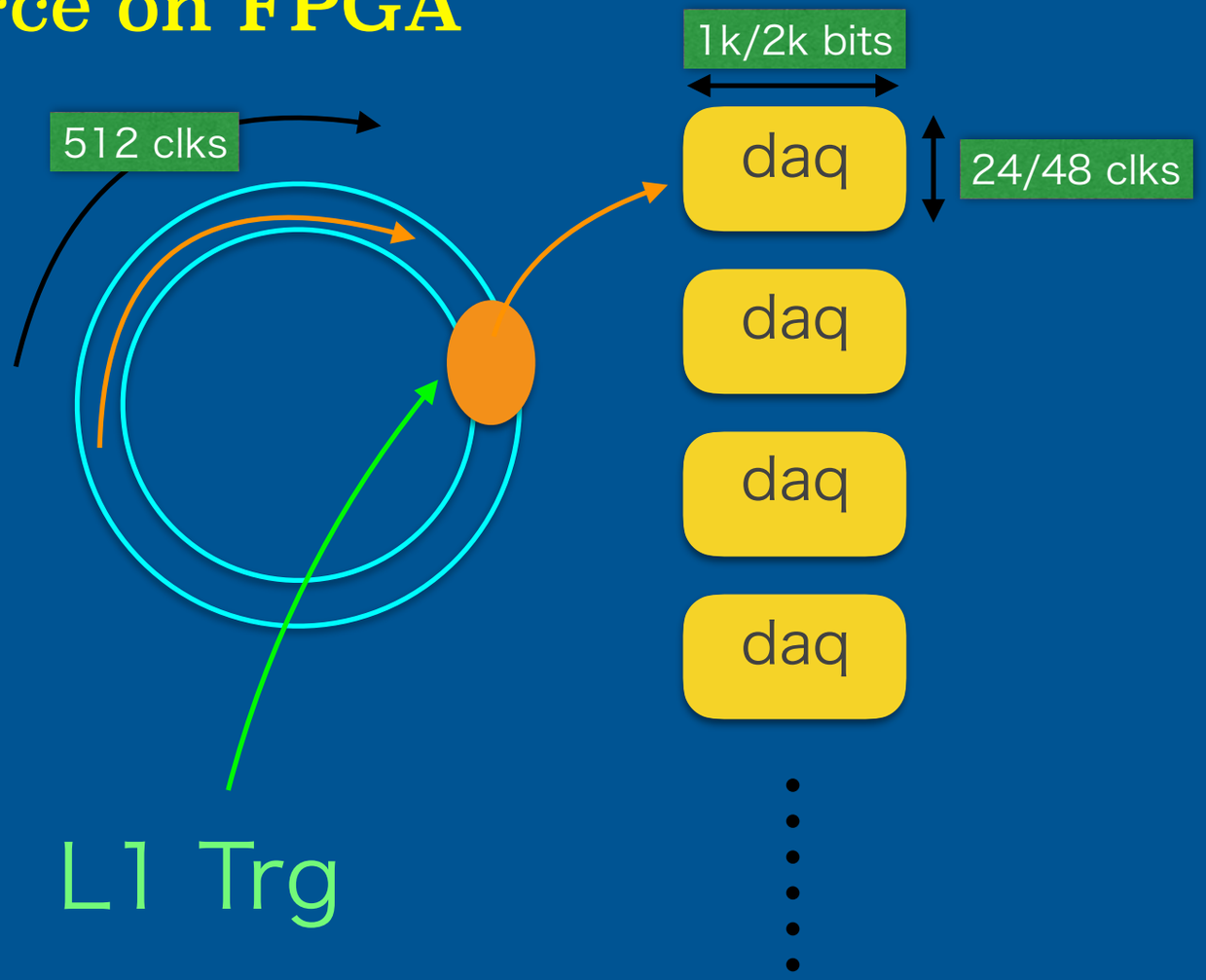
- ✓ 4 nsec timing shift observed after rebooting crate
- ✓ 127 MHz was generated using 254 MHz
  - ✓ 254 MHz for GTH
  - ✓ Two 127-MHz clocks with different phase generated randomly
- ✓ (Seems to be) solved by changing clock source



Event Buffer for b2l on UT3

- ✓ Hyunki's version
- ✓ Modified for different configurations (bit size, number of DAQ buffer, BRAM depth, address size, data clock, 380t/565t)
  - ✓ Depends on available resource on FPGA

bit size	#daq buf	daq buf depth	UT3	Module
1k	4	24	380t/ 565t	2D
2k	16	48	380t/ 565t	GDL



2D(CDCTRG) data taking through b2l

- ✓ For debugging 2D Firmware
- ✓ Merger play mode; Simulation data given to Merger
  - ✓ Merger -> TSF -> 2D
- ✓ Event buffer
  - ✓ outputs have 8 clock width
    - ✓ 1k bit, 4 DAQ buffer, 24 clock depth
- ✓ Dedicated trigger using TSF
  - ✓ GDL -> FTSW228 -> 2D
    - ✓ Delay for this cycle adjustable through VME
- ✓ Dummy data test ok, will under go this week.

b2l + b2tt unified interface

- ✓ b2l + b2tt + Event buffer
- ✓ To clean up top.vhd
  - ✓ Signals to connect b2tt and b2l hidden
- ✓ To increase b2l easily if necessary
  - ✓ Without increasing Event buffer size
  - ✓ UT3 has 40 GTX lanes (4 RJ45)
- ✓ Any reason to have separate component?

```
map_b2l : entity work.myb2l
  generic map (
    B2LIN_DATA_WIDTH => B2LIN_DATA_WIDTH,
    DBUF_ADDRESS_WIDTH => 6, -- 5/6 for 565t/380t
    DBUF_DEPTH => 48, -- 24/48 for 565t/380t
    IDATACLK => 128 -- 32 or 128
    )
  port map (
    RESET_X => RESET_X,
    CLK125M_P => CLK125M_3P, -- in
    CLK125M_N => CLK125M_3N, -- in
    dataclk => CLK125M,
    sysclk => CLK125M,
    clk250m => CLK250M,
    data_b2l => data_b2l, -- in
    revo_r => revo_r, -- out
    trgCntr => trgCntr,
    trgL1 => commonL1,
    delay => b2l_buffer_delay,
    RJ_CLKP => RJ_CLKP(0),
    RJ_CLKN => RJ_CLKN(0),
    RJ_TRGP => RJ_TRGP(0),
    RJ_TRGN => RJ_TRGN(0),
    RJ_ACKP => RJ_ACKP(0),
    RJ_ACKN => RJ_ACKN(0),
    RJ_RSVP => RJ_RSVP(0),
    RJ_RSVN => RJ_RSVN(0),
    TXN_B2L => TXN_B2L,
    TXP_B2L => TXP_B2L,
    RXN_B2L => RXN_B2L,
    RXP_B2L => RXP_B2L,
    debug => debug_b2l
    );
```

GDL data

- ✓ 96 inputs (input, inputDelayed)
- ✓ 192 outputs (ftd, psnm)
- ✓ TMDL outputs
  - ✓ timing source 3 bit + α
- ✓ Raw mode
  - ✓ Record everything within time window
  - ✓ Except for “inputs” due to large timing variation ~ 2usec
  - ✓ 476 + α bits, 48 clocks ~ 3 kB/event
- ✓ Suppress mode
  - ✓ bit number + rising timing for only fired bit in 32bit word
  - ✓ 100 fired * 32bit < 0.5 kB/event

Trigger Data

		#UT3	B/ev	MB/sec	
GDL		1	500	15	
GRL		1			
ECLTRG		1	400	11	
KLMTRG		1	7/muon	0.2/muon	Sent to GRL
TOPTRG		2			No b2l? To GRL?
CDC	TSF	9			
CDC	2D	4			
CDC	3D	4			
CDC	NN	4			
CDC	ETF	1			No b2l?
Total					

Summary

✓ **GDL is ready to debug using real data.**