SVD DAQ

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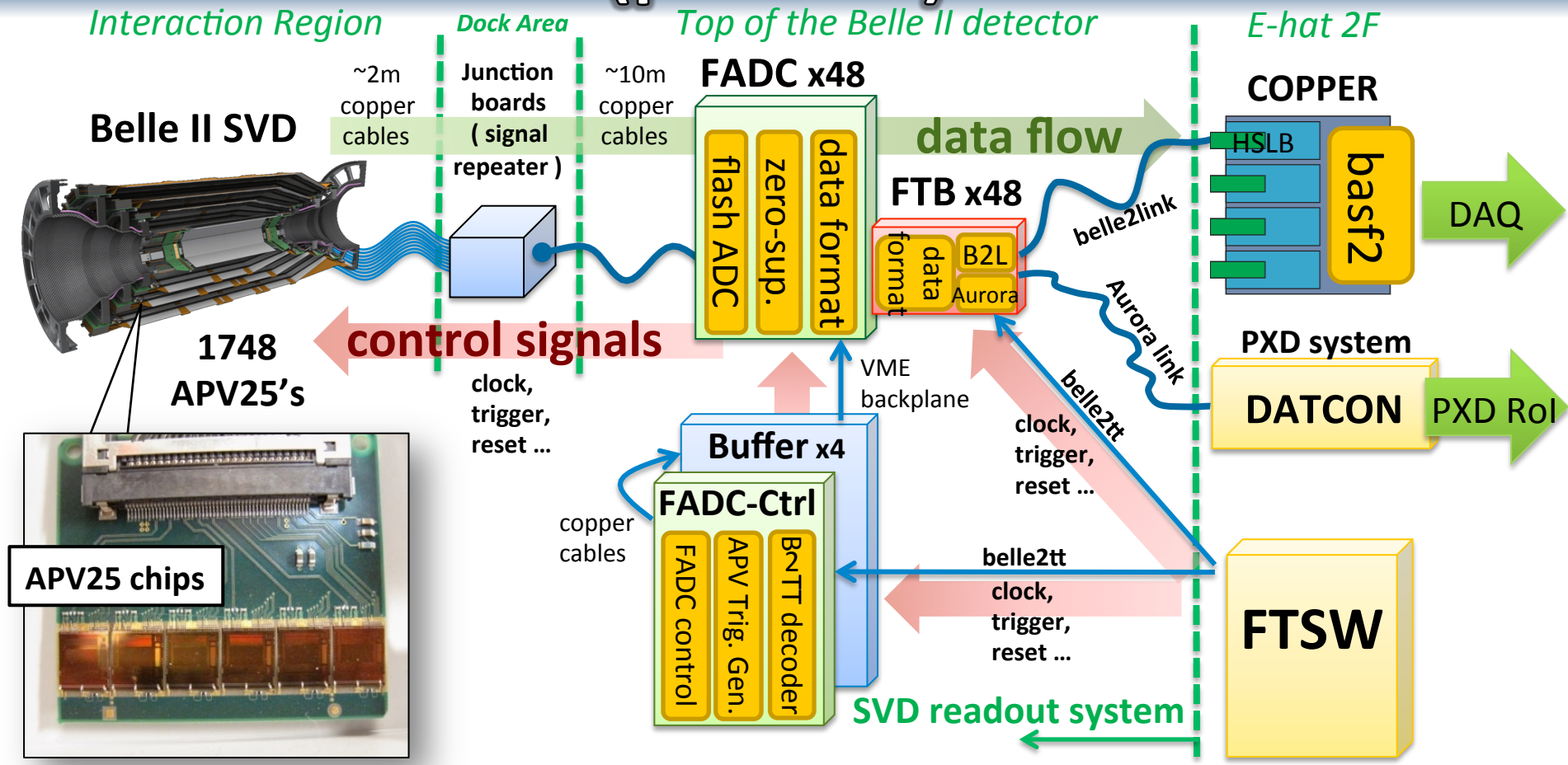
TRG/DAQ Workshop

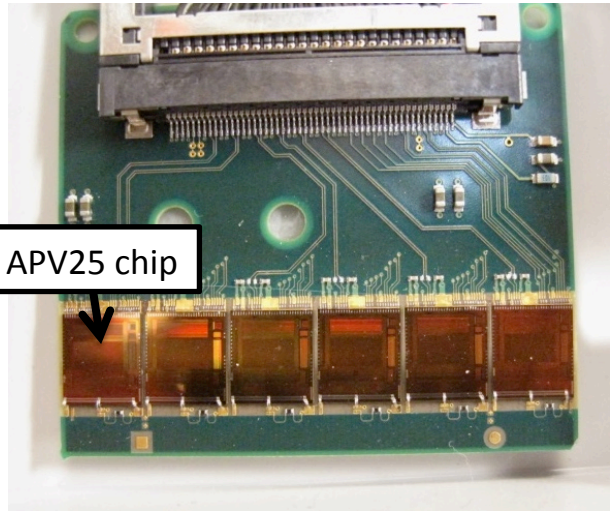
SVD Readout System Overview (phase-3)



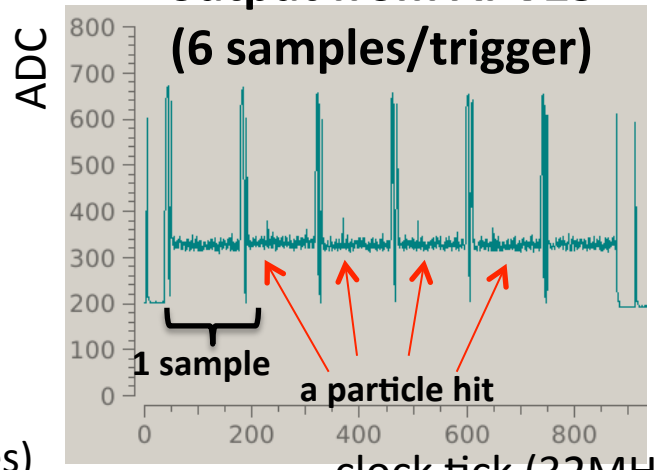
SVD readout system is driven by 32MHz clock.

APV25 and Requirement on Triggers

- **APV25 chip**
  - Front-end electronics for DSSD signal readout
  - Provides 128-channels analog signals sampled among several clock ticks
  - Shaping time: 50 nsec
  - Suitable for high occupancy in Belle II SVD
- **6- and 3-samples/trigger modes will be used for Belle II SVD**
  - 6-samples/trigger is preferable for good peak finding
- **Requirements on triggers from APV25**
  - **Maximum average trigger rate**:
    - **38kHz** (6-samples), **76kHz** (3-samples)
      - cf. max. trigger rate in Belle II is 30kHz
  - **Minimum trigger interval**: (3 clocks/3-samples)
    - **189nsec** (6-samples), **94nsec** (3-samples)
  - **Maximum trigger latency**:
    - **5.03 usec** (available pipe-line size of 160 samples)



output from APV25 (6 samples/trigger)



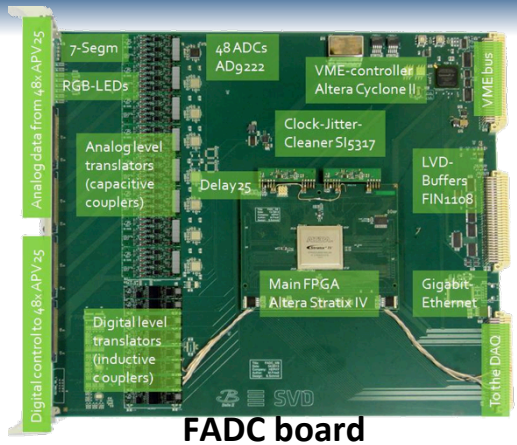
SVD internal trigger latency

- **Measurement at KEK says SVD FADC system (in final cable length) causes 230nsec trigger propagation internally.**

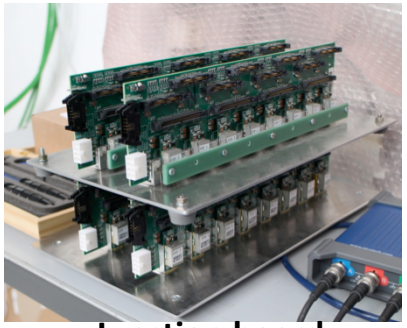
- **Maximum acceptable APV25 latency: 5.030usec**
- **Trigger distribution in FTSWs: 350nsec (from Nakao-san's measurement)**
- **Travel in FADC system: 230nsec (from our measurement)**
- **→ Trigger generation must be within less than 4.45usec**
  - 4.45 usec = 5.03 usec – 0.35 usec – 0.23 usec

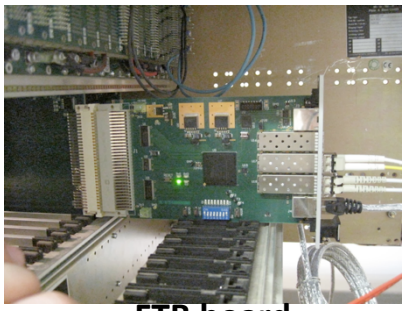
Electronics Preparation Status

- **FADC board (48 boards for phase-3)**
  - **Ver.3 board**: Produced and tested at the last DESY beam test. Good performance of data readout was confirmed on DESY beam test. Especially, stabilities of FPGA configuration and VME access are excellently improved.
  - **Ver.4 board (for phase-3)**: Final version of FADC board, in which noise performance will be improved. Schematic drawing work has been started at HEPHY. The first samples will be ready by Mar. 2017.
    - The performance will be tested with a permanent DAQ setup in DESY.
- **Junction board (48 boards for phase-3)**
  - **Board for FADC Ver.3**: Produced and tested at the DESY beam test. Working good.
  - **Board for FADC Ver.4 (for phase-3)**: Modification on schematics has been done. Once cross-check is completed, we will order PCBs.
- **FADC-Ctrl board (1 board for phase-3)**
  - **Ver.2 board (for phase-3)**: Produced and tested at the DESY beam test.
- **FTB board (48 boards for phase-3)**
  - **Ver.3 board (for phase-3)**: well tested and mass-production has been completed already.



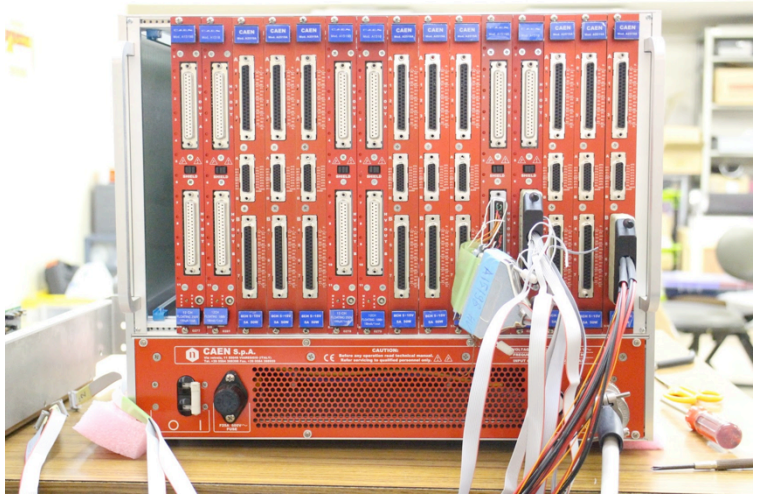
FADC board


Junction board


FTB board

Power Supply Preparation Status

- **For SVD HV and LV, CAEN modules are employed.**
  - Crate: SY4527 (Universal multichannel PS system, can be controlled with EPICS)
  - HV: A1519B (250V, 1mA, floating 12ch)
  - LV: A2519A (15V, 5A, 50W, floating 8ch)
  - Separation voltage: A1510 (100V, 10mA, floating 12ch)
- **All necessary modules are already purchased by PISA.**



CAEN HV/LV power supply modules

- **These modules were tested at the last DESY beam test. Although an A1510 module we brought DESY had a problem and didn't work, other modules excellently worked without any suspicious noise.**
- **But, we realized that the separation voltage module A1510 can supply only single polarity, while we need bipolar (-5V…+5V).**
  - By phase-3, we will introduce remote-controllable polarity switches on this separation voltage lines.

Firmware Preparation Status

- **Basically, minimum set of firmwares for data taking are already prepared.**
  - They work good in the previous DESY beam test.
- **However, still some necessary functions for the physics run are missing and further development are required.**

Remaining Tasks in Firmware Development

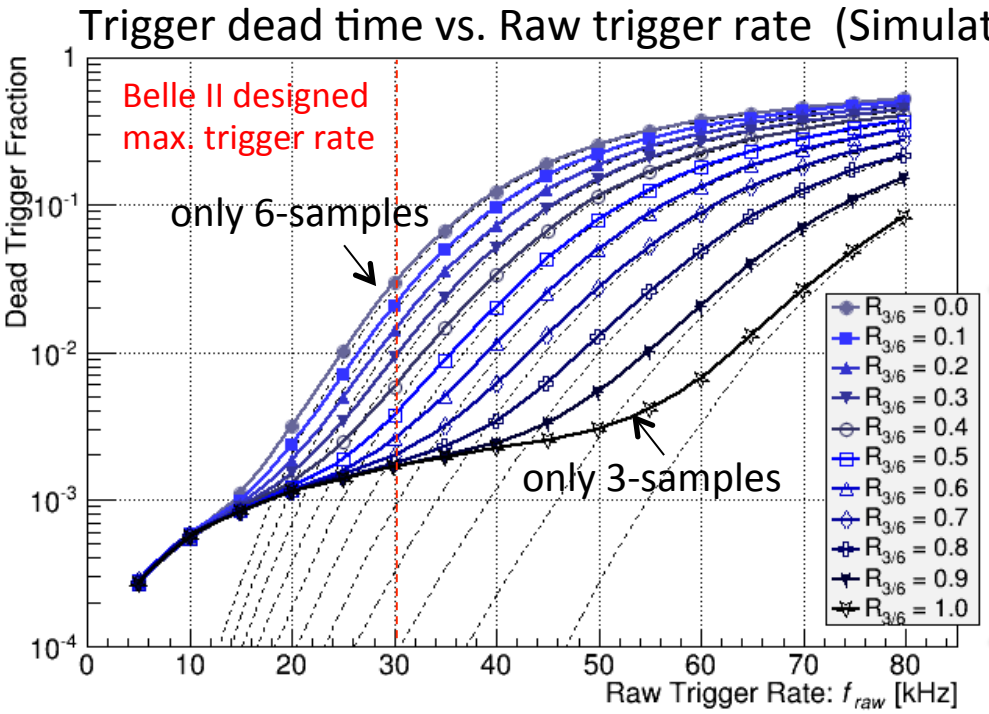
High priority: (necessary for physics run)

- **APV pipe-line address emulator (in FADC-Ctrl)**
  - Emulate pipe-line address and compare it with the transmitted address from APV with data
  - so that we can detect the event order mismatch on FADC
- **APV FIFO emulator (in master FTSW)**
  - Emulate the occupancy of FIFO in APV chip and assert trigger veto in FTSW master when FIFO is almost full
  - otherwise APV gets FIFO full with the next trigger and data are corrupted.
- **Improvement on common-mode correction (CMC) function. (in FADC)**
  - Currently 128-strips wise, but will be changed to 32-strips wise for more accurate common-mode noise reduction.
- **Fake-hit filter (in FADC)**
- **Remote FPGA configuration through VME access (in FADC)**
- **Improvement on data format of FTB-DATCON link (in FTB)**
  - Nakao-san suggested to increase the data size of the clock counter (currently 24-bits) which FTB transmits to DATCON.

Middle priority: (not mandatory, but better to have)

- **GbE data link for SVD local data taking (in FADC)**
  - For faster local data taking.
- **Zero-suppressed + Hit timing extraction mode (in FADC)**
  - The last data format for further data size suppression.
- **Function of event-by-event switching btw. 3- and 6-samples depending on trigger types. (in FADC-Ctrl + FADC)**
  - Necessary only for operation with about 30kHz or higher trigger rate.
- **New FTB data format (in FTB)**
  - w/ more useful information.

Simulated Trigger Dead Time from SVD (w/ APV25 FIFO emulator)



shown at
TRG/DAQ workshop 2014

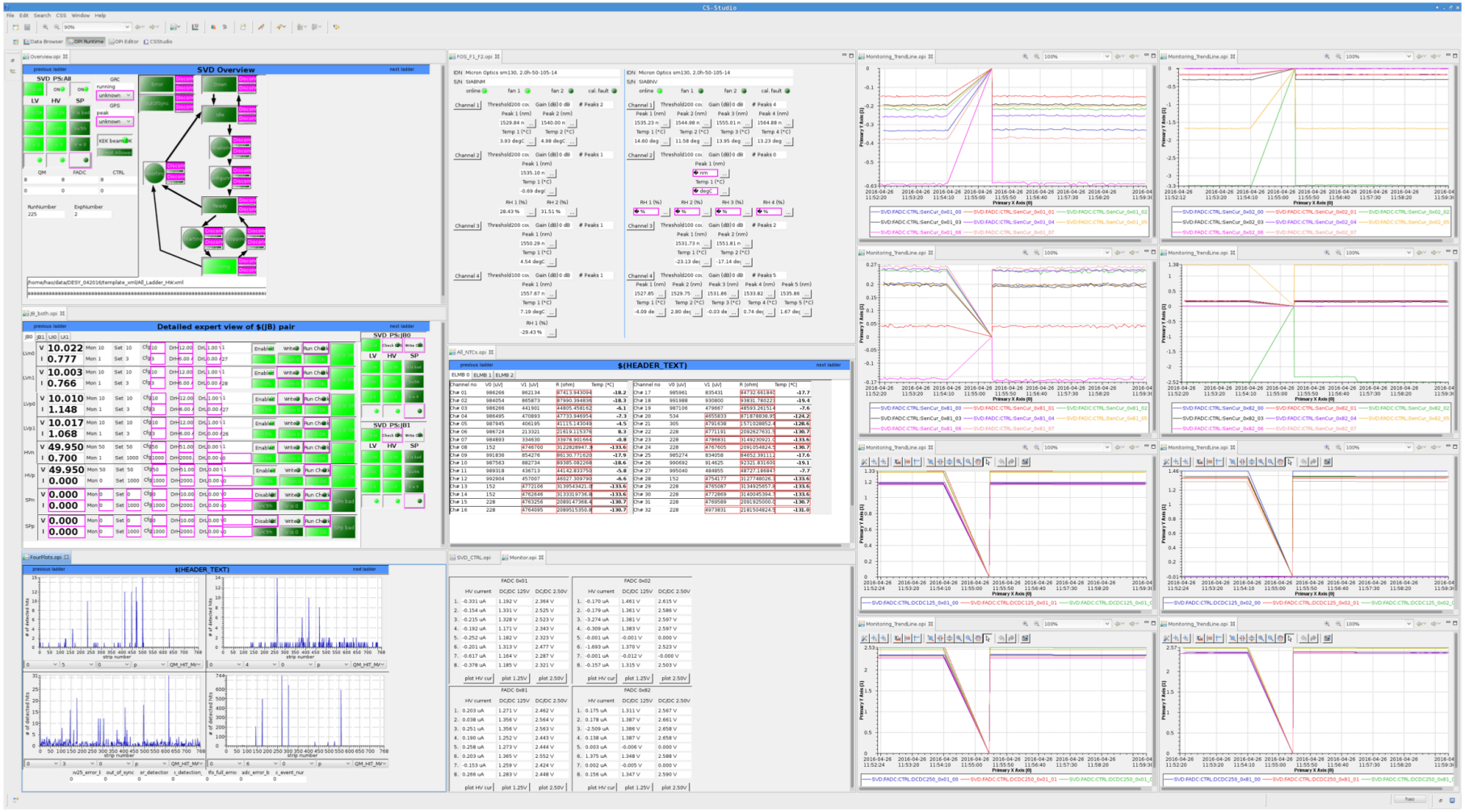
$R_{3/6}$: fraction of mixed 3-samples mode

threshold: 26 samples
no trigger/busy propagation
trigger interval: 190nsec (24 clocks)

- **Trigger dead time at 30 kHz trigger is 3%.**
- **Furthermore, the trigger dead time can be decreased by switching btw. 3-/6-samples event-by-event according to trigger timing resolution.**
- **If we can increase $R_{3/6}$ to more than 0.7, 50 kHz trigger is also acceptable.**

SVD slow control (1)

from H. Yin slides, Jun 21 B2GM



SVD slow control (2)

from H. Yin slides, Jun 21 B2GM

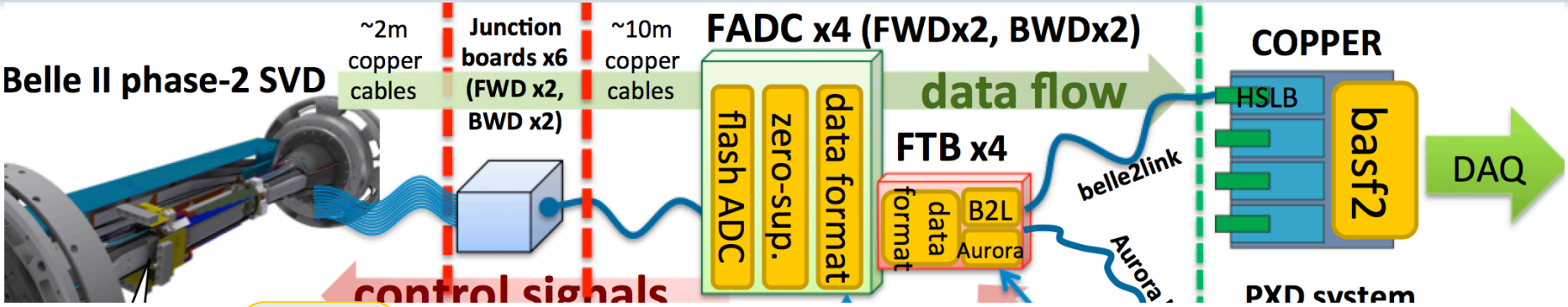
```
[28-04-2016 10:42:55]   Info::FADC_CTRL::DataServer started. Accepting conn
[28-04-2016 10:42:55]   Info::WriteToFile::File '/home/hao/data/DESY_042016
[28-04-2016 10:42:55]   Info::FADC_CTRL::Run initialized.
[28-04-2016 10:42:55]   Info::FADC_CTRL::Start configuring.
[28-04-2016 10:42:55]   Info::DataServer::Socket connection established.
[28-04-2016 10:42:56]   Info::CTRL::CTRL 'crate: 0, base address: 0xaa' has
[28-04-2016 10:43:02]   Info::FADCVME::crate: 0, base address: 0x01: has be
[28-04-2016 10:43:06]   Info::FADCVME::crate: 0, base address: 0x02: has be
[28-04-2016 10:43:11]   Info::FADCVME::crate: 0, base address: 0x81: has be
[28-04-2016 10:43:15]   Info::FADCVME::crate: 0, base address: 0x82: has be
[28-04-2016 10:43:15]   Info::HardwareRun::LocalHardwareRun successfully in
[New Thread 0x7fffa0ccd700 (LWP 2736)]
[28-04-2016 10:44:09]   Info::FADC_CTRL::Run starting.
[28-04-2016 10:45:13]   Info::FADC_CTRL::Run stopping.
[28-04-2016 10:46:26]   Info::FADC_CTRL::Run starting.
[Thread 0x7fffa1cd3700 (LWP 26726) exited]
[Thread 0x7fffa1dd4700 (LWP 26725) exited]
[New Thread 0x7fffa1dd4700 (LWP 2949)]
[New Thread 0x7fffa1cd3700 (LWP 2950)]

Program received signal SIGSEGV, Segmentation fault.
[Switching to Thread 0x7ffff4514700 (LWP 26656)]
0x00007ffff47436e8 in CAENVME_WriteCycle () from /lib/libCAENVME.so
Missing separate debuginfos, use: debuginfo-install bzip2-libs-1.0.6-12.el7
.4.46-12.el7.x86_64 libcap-2.22-8.el7.x86_64 libgcc-4.8.3-9.el7.x86_64 libs
x86_64 xz-libs-5.1.2-12alpha.el7.x86_64 zlib-1.2.7-13.el7.x86_64
(gdb) bt
#0  0x00007ffff47436e8 in CAENVME_WriteCycle () from /lib/libCAENVME.so
#1  0x927900ef8f7900fb in ?? ()
#2  0x27243a4d275d5e08 in ?? ()
#3  0x2c0911172c1b1900 in ?? ()
#4  0x2d090f182d151d07 in ?? ()
#5  0x71000203710c0000 in ?? ()
#6  0x73000002730d0400 in ?? ()
#7  0x36000000937900ee in ?? ()
#8  0x760d02043600040d in ?? ()
#9  0x947900ee76000000 in ?? ()
#10 0x987900f2957900ef in ?? ()
#11 0x700d0203997900f4 in ?? ()
```

- Mismatch of tasks during transition (no impact on Belle RC data acquisition).
- Used XML setting, designed to debug the system to temporarily replace the configuration databases. Current XML files are not user friendly.
- Warning / error communication to Belle II RC is missing. Is there an interface?
- FADC CTRL crashed 3x during the last few weeks of the beam test... The cause still unknown!

HEPHY Institut für Hochenergiephysik

Outcomes from DESY beam test (Study of SVD event order)

SVD event number in DESY BT




```
event # 0
>  ffaa0000 000000f3 d48219ff 80c50011 81c50013 82c50013 83c50011
           ======  !=    ==
event # 1
>  ffaa0000 000001f6 d4820900 80360003 81360002 82360001 83360000
           ======  !=    ==
event # 2
>  ffaa0000 000002f7 d4821901 806100fe 816100fd 826100fc 836100fc
           ======  !=    ==
```

B2L event num.

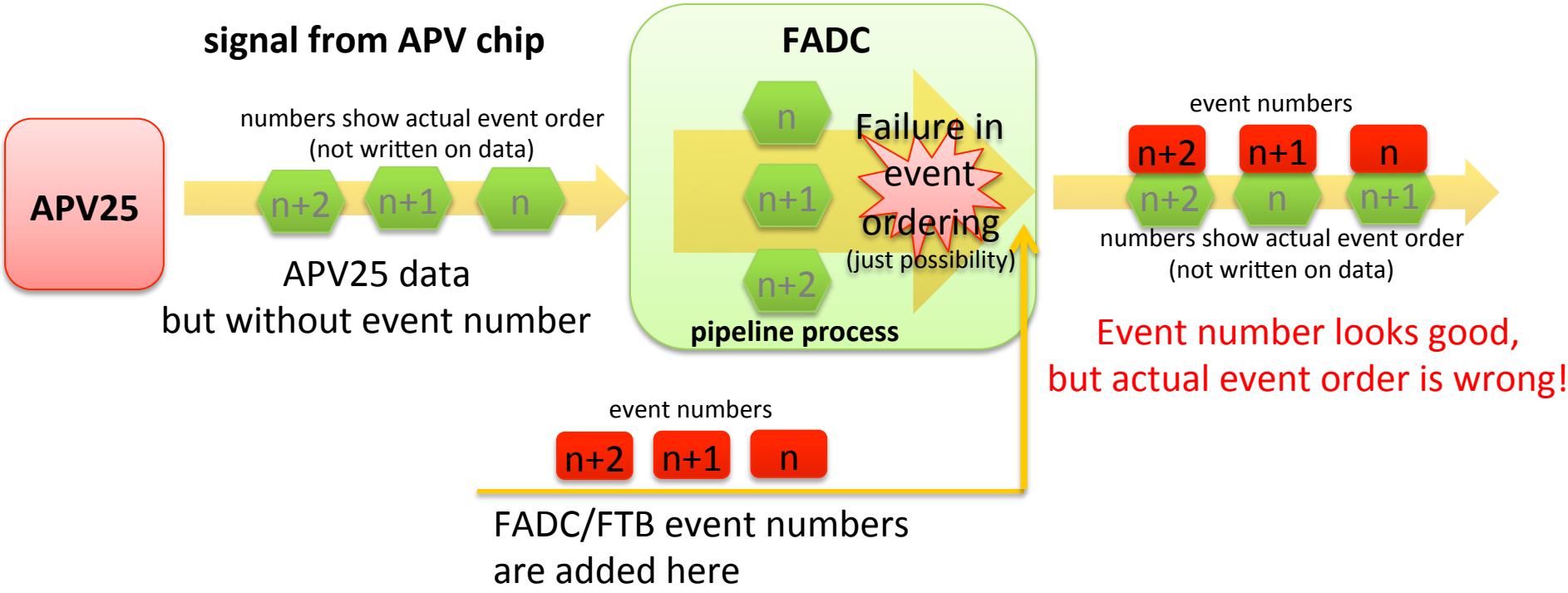
FTB event num. (24-bit)

FADC event num. (8-bit)

hit data

- **The FTB number is consistent with B2L number.**
- **FADC number is always B2L number – 1, but we know the cause of the problem and we are sure this doesn't cause the observed VXD event mixing.**

But, is the event order in FADC really correct?

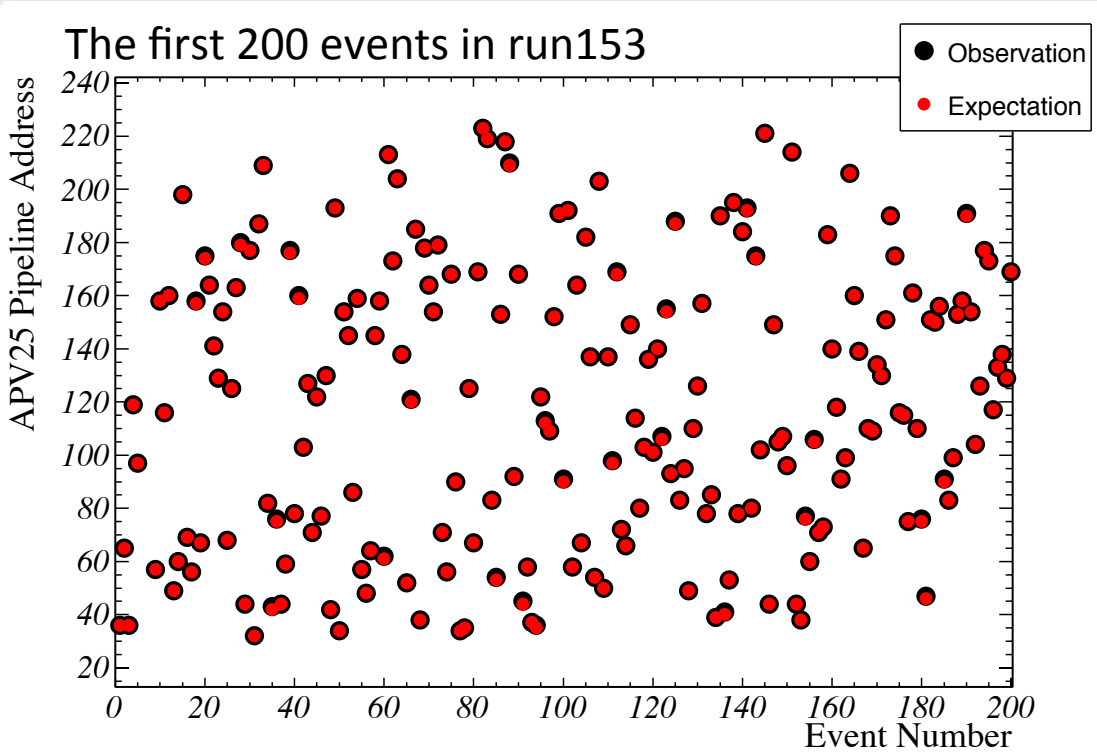


- **Nakao-san pointed out a possibility that event mixing can happen even in SVD even we see good event numbers.**
  - Because APV25 data do not contain event number.
- **This possibility has not been checked yet.**
- **We should check it by comparing APV25 pipeline address (= PLA) and FTSW clock counter value.**
  - Very roughly speaking, the APV25 PLA is compatible with the clock counter.

PLA simulation method

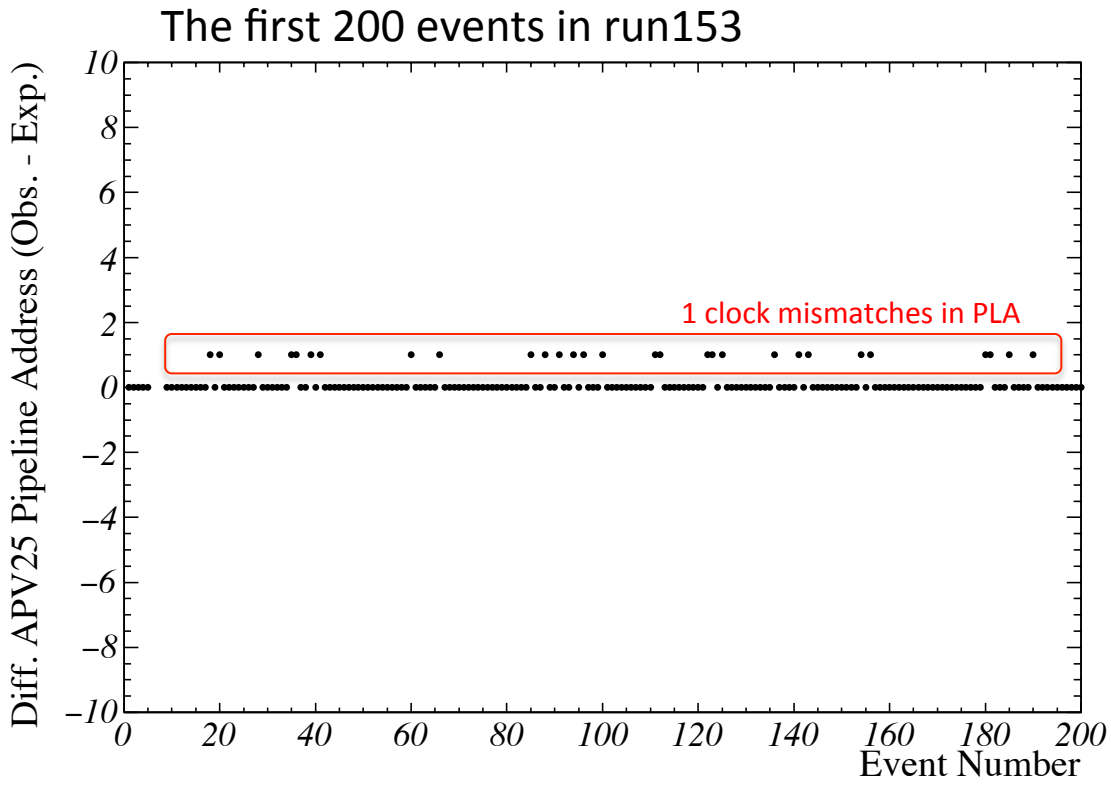
- **What is recorded on the stored data?**
  - Observed PLAs on all APV25
  - Event number
  - 127MHz Clock counter from FTSW
  - (Fine trigger timing on FADC system)
- **Basically, using PLA value in event *n-1* and difference of FTSW clock counter values between events *n-1* and *n*, we can expect PLA value in event *n*.**
  - However, exact expectation requires detailed understanding of APV25 data process, e.g. necessary process time for 1-event output.
- **In the last DESY beam test, FTSW applied a trigger veto for about 300usec or 100usec after every trigger accept due to an issue on PXD data taking.**
  - 300usec is enough time to finish readout of all 6 samples in APV25 (6 samples x 140 clocks/sample x 31nsec/clock = 26usec).
- **→ Always, next trigger comes after APV25 finishes to output the current event data.**
- **This makes the expectation of PLA behavior rather easier. We can assume a fixed number of skipped cells for the completion of the 1-event output.**

Observed vs. Expected PLA



- **Mainly, expected PLA values are consistent with observed PLA values.**
  - Also I checked all the data in run153 other than above 200 events, but didn't see any inconsistency from the expected values.
- **We can conclude SVD event order was NOT mixed up at all.**

Observed PLA – Expected PLA



- **BUT, we see 1 clock mismatches between the observation and expectation in a fraction of about 10%.**
- **So far I don't know the cause of the problem, but it is not related to the VXD event order mismatch problem.**
  - This will be studied further more to develop PLA emulator firmware.

SVD Data Format

SVD Data Format

- ***Raw mode***
  - Only for SVD internal data taking (timing adjustment, noise measurement, calibration, …). Not sent to Belle II DAQ.
    - raw ADC data for a defined length
- ***Transparent mode***
  - Data w/o zero-suppression for debugging of FADC system. (not for physics data taking.)
    - APV25 frame detection with header data and raw data of all strips
- ***Zero-suppressed mode***
  - For physics data taking.
    - Pedestal subtraction, CMC, only hits above threshold (3 or 6 samples)
- ***Zero-suppressed + hit time finding mode***
  - Future data format for further data size suppression.
    - Peak sample and peak time, all 3 or 6 samples only for unclear cases (such as double peak = pileup)
- ***Zero-suppressed (+hit time finding)*** **are the normal data formats sent to FTB + COPPER/DATCON**

SVD Data Size

The numbers of data sizes in this slide are sums of FADC+FTB data, but without B2L data.

- **Maximum size:**
  - *Transparent mode:* 64 words per channel & sample → **18725 w.**
  - *Zero-suppressed mode:* all channels have hits → **12343 words**
  - *Zero-suppressed + hit time mode:* all channels have hits & need sample data → **18485 words**

- **The actual size is much smaller. It depends on the occupancy and the number of APV25 chips (= N) on the FADC.**
  - **FTB header (2 words) + FADC header (1 word) + APV header (N words) + DSSD hit data (occupancy*128*1(3-samples) or 2(6-samples) words) + FADC trailer (1 word) + FTB trailer (1 word)**
    - **= 5 + (occ.*128 + 1)*N (3-samples)**
    - **= 5 + (occ.*256 + 1)*N (6-samples)**
  - **1% occupancy** makes **~176 words** (*zero-suppresed mode,* 6 samples)

Global Schedule

Detector Preparation Schedule

- **Dec. 2016: 3rd DESY beam test campaign**
- **Now SVD ladders are under mass production in all the production sites**
- **Assembly of SVD will start on Feb. 2017 at KEK B1.**
- **Phase-2: A partial VXD system will be installed for phase-2 commissioning.**
  - connected to the global Belle II DAQ system
  - w/ BEAST sensors for beam background study in VXD volume
- **Cosmic-ray commissioning: In parallel to phase-2, full VXD will be assembled and tested with**
  - connected to a secondary Belle II DAQ system
- **Phase-3:**
  - Full VXD installation and operation

Thanks!

backup slides from here

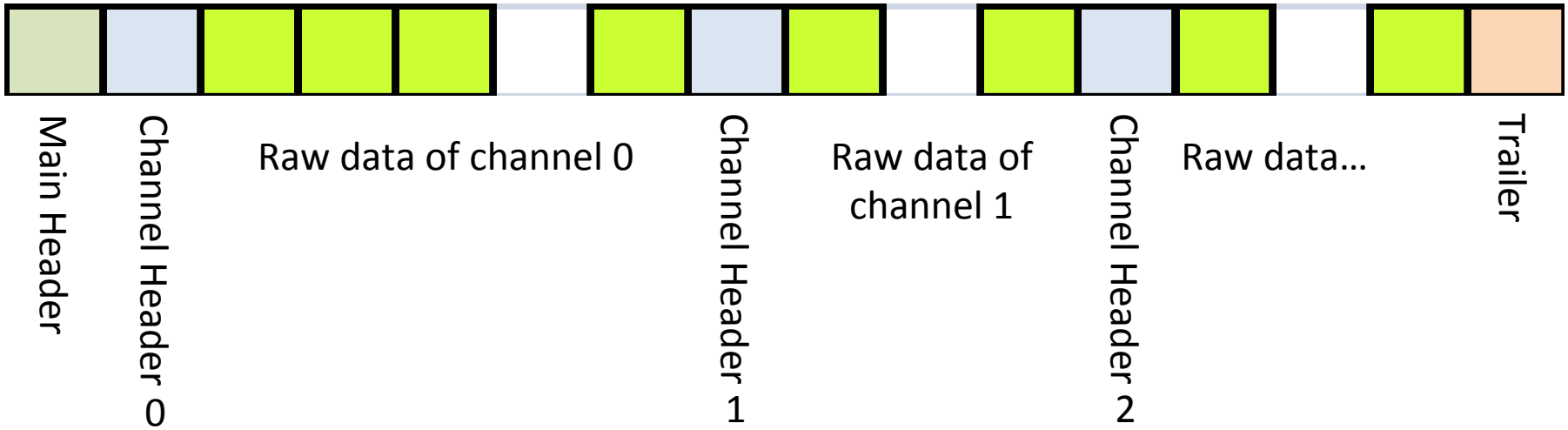
Data Format: Raw Mode

bit	Main Header	Channel Header	Raw Data	Trailer
31	1	1	0	1
30	1	0	Reserved	1
29	0	Channel # (0…47)	Reserved	1
28	Run type		Reserved	0
27			Data sample N+1	Reserved
26	Local event			
25				
24				
23	FADC # (0…255)	Reserved		Reserved
22		Reserved		
21		ADC delay (0…49)		
20				
19				
18				
17				
16				
15	Trigger number (D15:D0)	# of data samples to follow	Reserved	CRC16 checksum
14			Reserved	
13			Reserved	
12			Data sample N	
11				
10				
9				
8				
7				
6				
5				
4				
3				
2				
1				
0				

- **Run type**
  - 00…raw
  - 01…transparent
  - 10…zero-suppressed
  - 11…zero-suppressed + hit time finding
- **Event type**
  - 000…TTD event
  - 100…local software trigger
  - 101…local intcal

Raw Mode Example

- **One data frame consists of**
  - 1 Main Header
  - 1 Channel Header per active APV25 input (up to 48)
  - X/2 words for raw data for each active APV25
    - X…number of ADC samples (written in channel header)
  - 1 Trailer



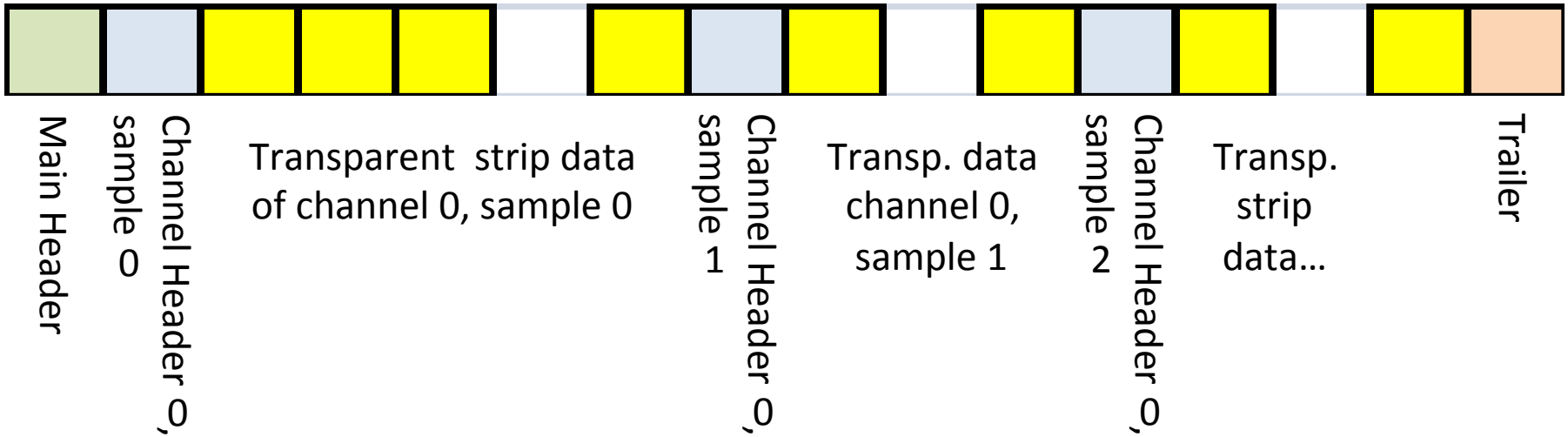
Data Format: Transparent Mode

bit	Main Header	Channel Header	Tranparent Data	Trailer
31	1	1	0	1
30	1	0	Reserved	1
29	0	Channel # (0…47)	Reserved	1
28	Run type		Reserved	0
27			Data strip N+1	Error 2
26	Local event			Error 1
25				Error 0
24				Wired-or error
23	FADC # (0…255)	Pipeline address (0…255)		Emulated pipeline address (0…255)
22				
21				
20				
19				
18				
17				
16				
15	Trigger timing & type (from TTD)	Error bit	Reserved	CRC16 checksum
14		Sample # (0…5)	Reserved	
13			Reserved	
12			Data strip N	
11		CMC2 (signed half-byte)		
10				
9				
8				
7	Trigger number (D7:D0)	CMC1 (signed byte)		
6				
5				
4				
3				
2				
1				
0				

- **Error bit**
  - Extracted from APV25 header
- **Wired-or error**
  - OR of all APV25 error bits
- **Error 0, 1, 2**
  - indicators for abnormal conditions

Transparent Mode Example

- **One data frame consists of**
  - 1 Main Header
  - 1 Channel Header per active APV25 input (up to 48)
  - 64 words for raw strip data for each active APV25 and sample
  - 1 Trailer



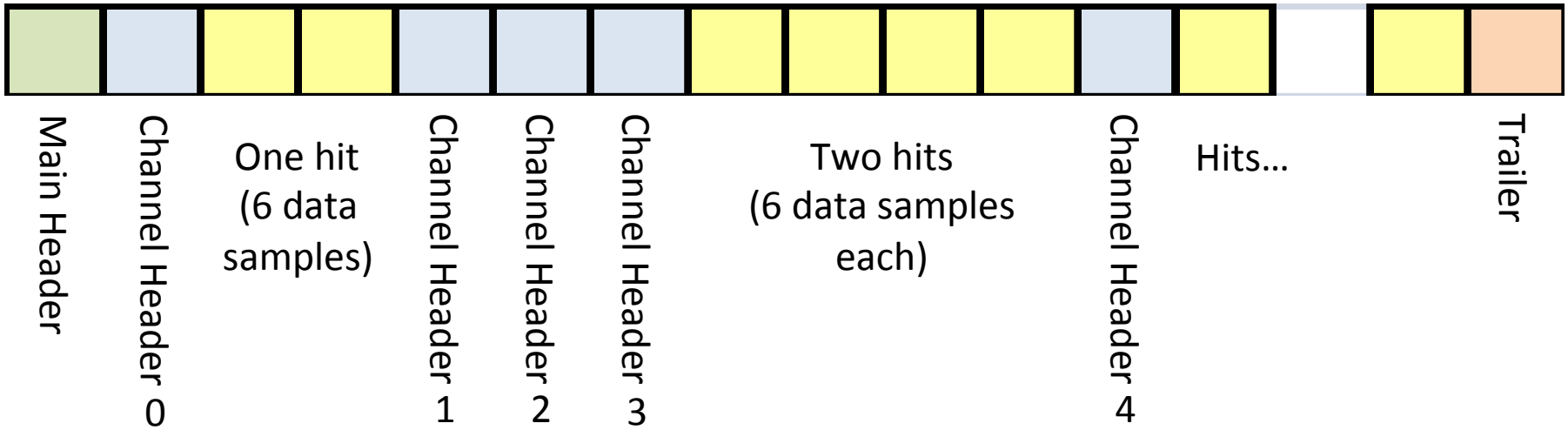
Data Format: Zero-suppressed Mode

bit	Main Header	APV Header	0-suppressed data	0-suppressed data	Trailer
31	1	1	0	0	1
30	1	0	Strip number (0…127)	Strip number (0…127)	1
29	0	APV # (0…47)			1
28	Run type				0
27					Error 2
26	Local event				Error 1
25					Error 0
24					Wired-or error
23	FADC # (0…255)	Pipeline address (0…255) *	Data sample 2 ***	Data sample 5	Emulated pipeline address (0…255)
22					
21					
20					
19					
18					
17					
16					
15	Trigger timing & type (from TTD)	Error bit **	Data sample 1 ***	Data sample 4	CRC16 checksum
14		Reserved			
13					
12					
11		CMC2 (signed half-byte) *			
10					
9					
8					
7	Trigger number (D7:D0)	CMC1 (signed byte) *	Data sample 0	Data sample 3	
6					
5					
4					
3					
2					
1					
0					

- **Remarks**
  - * of first sample
  - ** wired-or of all samples
  - *** only if >1 samples
- **Second yellow block only appears if 6 samples are read out**

Zero-suppressed Mode Example

- **One data frame consists of**
  - 1 Main Header
  - 1 Channel Header per active APV25 input (=up to 48)
  - 2N data words with N hit strips (in case of 6 samples)
    - No data words if no hits found
  - 1 Trailer



Data Format: Zero-suppressed + Hit Time

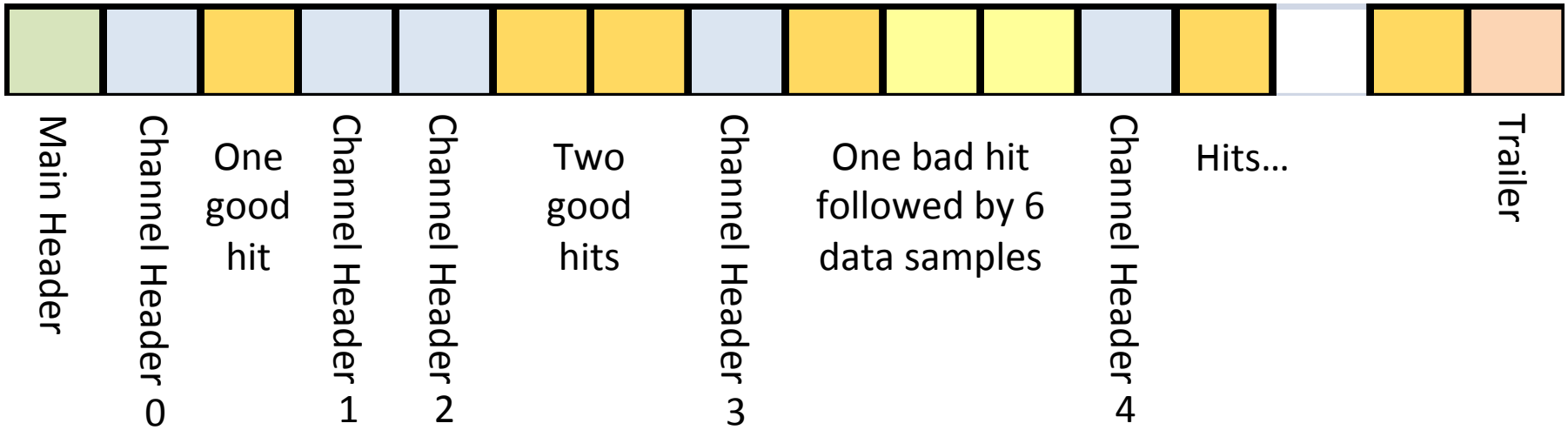
bit	Main Header	APV Header	Hit finding data	0-suppressed data	0-suppressed data	Trailer
31	1	1	0	0	0	1
30	1	0	Strip number (0…127)	Strip number (0…127)	Strip number (0…127)	1
29	0	APV # (0…47)				1
28	Run type					0
27						Error 2
26	Local event					Error 1
25						Error 0
24						Wired-or error
23	FADC # (0…255)	Pipeline address (0…255) *	Reserved	Data sample 2 ***	Data sample 5	Emulated pipeline address (0…255)
22			Reserved			
21			Reserved			
20			Reserved			
19			Samples next			
18			Peak sample # (0…5)			
17						
16						
15	Trigger timing & type (from TTD)	Error bit **	Peak time & quality	Data sample 1 ***	Data sample 4	CRC16 checksum
14		Reserved				
13						
12						
11		CMC2 (signed half-byte) *				
10						
9						
8						
7	Trigger number (D7:D0)	CMC1 (signed byte) *	Data sample at peak	Data sample 0	Data sample 3	
6						
5						
4						
3						
2						
1						
0						

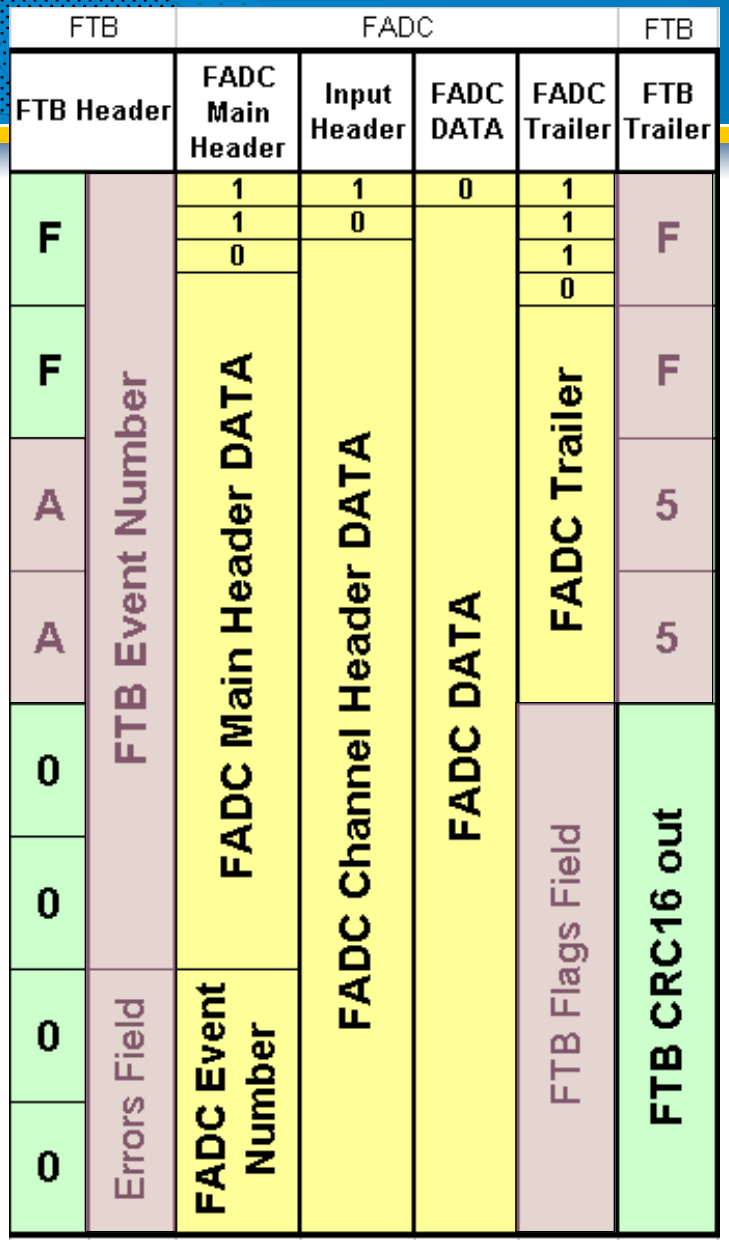
(Only if 6 samples)

- **Normally, only peak sample and peak time is sent (orange)**
- **Yellow sample data word(s) only appears if hit time cannot be found reliably**
  - E.g. double-peak due to pile-up
  - “Samples Next” = 1 in such a case

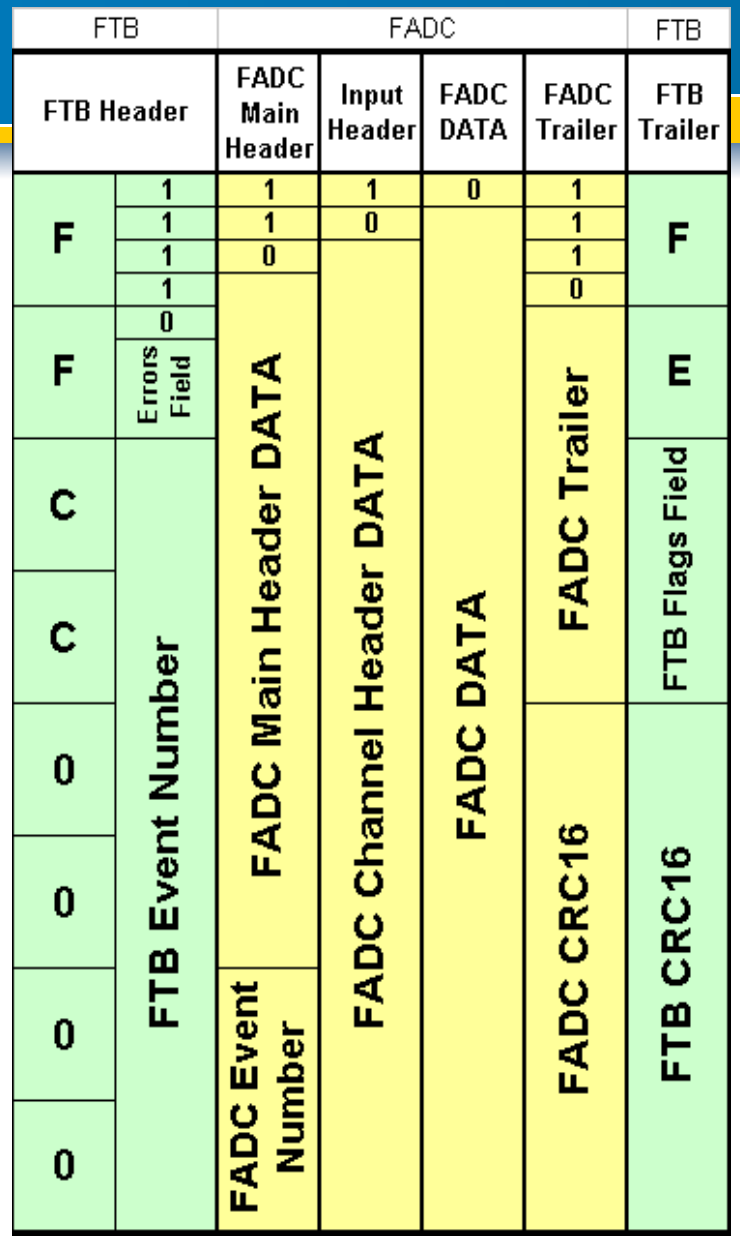
Zero-suppressed + Hit Time Example

- **One data frame consists of**
  - 1 Main Header
  - 1 Channel Header per active APV25 input (=up to 48)
  - N data words with N hit strips
    + 2 data words per bad hit (no timing found)
  - 1 Trailer





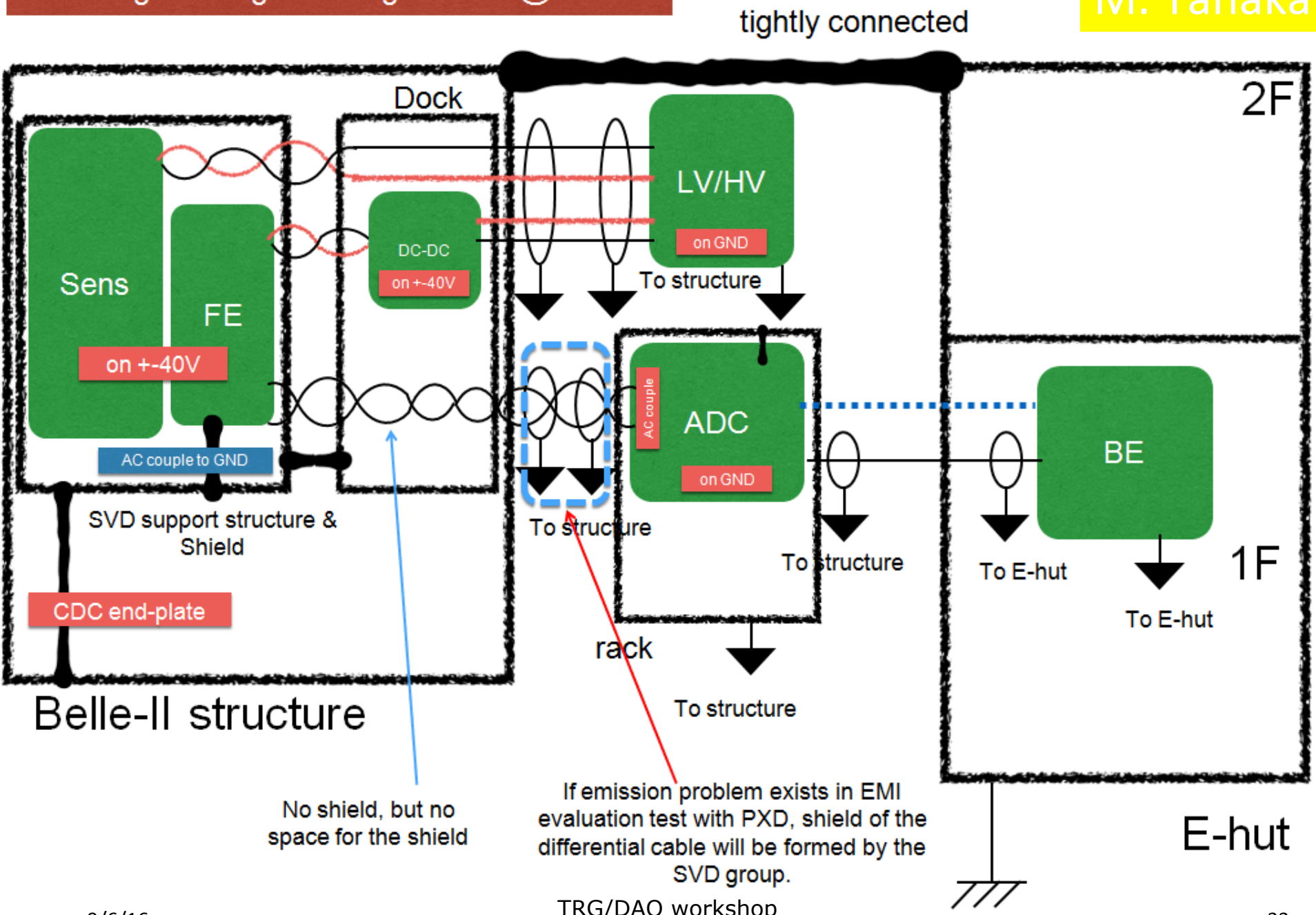
Current FTB data format @ Sep. 2016



Future FTB data format

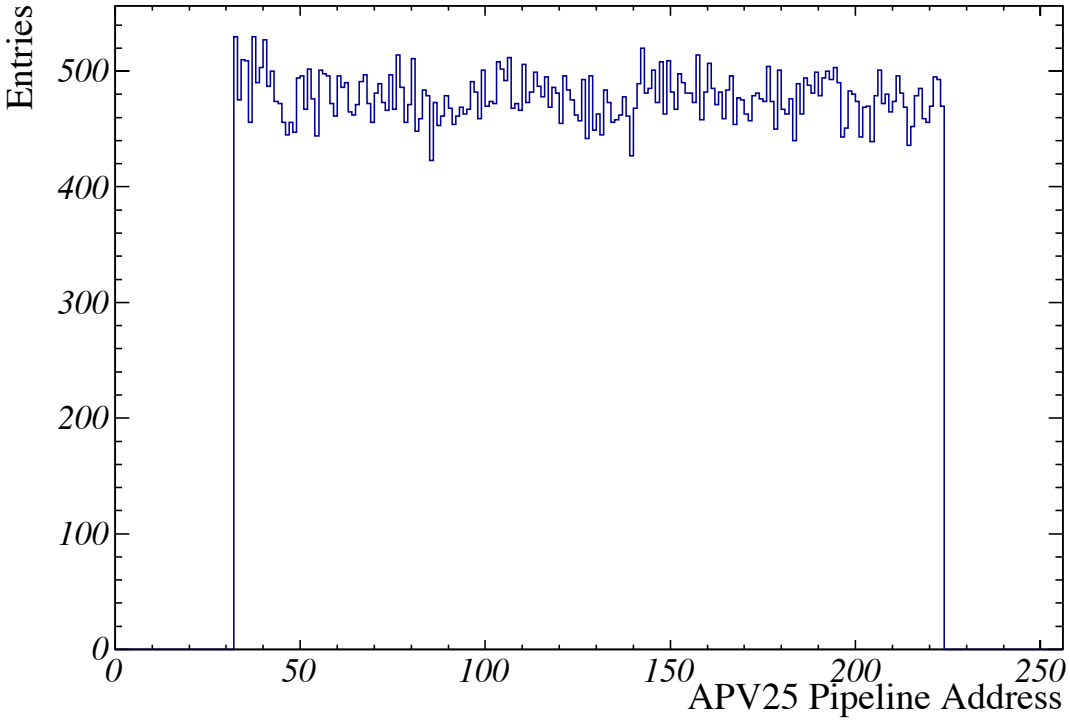
SVD grounding/shielding scheme@2015

M. Tanaka



PLA distribution

All the data in run153



- **All the PLA values shown here are gray-decoded ones.**
- **I realized that PLA values range not from 0 to 191, but from 32 to 223.**
- **The distribution looks reasonably uniform within statistics.**