Timeline

- Original idea was to start the R&D for the upgrade from 2018, but it may be deferred by one year because of the delay in Belle II schedule.

- It will require two years to complete the R&D.

- We will start the mass production of new readout cards from next year after the R&D, and complete the production in 3 years.

- The actual replacement of COPPERs will start in 2nd year of the production at the earliest.

- Subsystem-by-subsystem replacement is planned (as we did in Belle I to replace FASTBUS TDC with COPPERs).

- Complete the replacement by 2023(could be 2024) at the earliest.