TRG General

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TRG/DAQ Workshop in BINP

2016/09/05

TRG (L1) : Requirements and Strategy

- **Requirements** (☑ = ok, ☒ = under study or unknown)
  - ☑ **High efficiency** — **almost 100% for Upsilon 4S events**
    - No dead-time -> pipeline
    - Redundant and independent TRG logics -> 3 main TRG
  - ☒ **Max. average rate** — **30 kHz @ 8×10^{35} $cm^{-2}s^{-1}$**
    - Limited by DAQ
    - Good background reduction necessary
    - Flexible TRG logics to manage BG rates
    - Low level event reconstruction to identify BG
  - ☑ **Latency** — **~5 usec**
    - Limit from SVD front-end
  - ☑ **Timing precision** — **less than 10 nsec**
    - Request from SVD front-end
  - ☒ **Event separation** — **400 nsec**
    - Request from DAQ
- **Belle triggering scheme is employed again**
  - Sub-Triggers + Global Decision Logic
  - Basic idea is same, but each components will be improved

    Data flow : parallel -> high-speed serial

    Data rate : 16 Mbps -> 190 Mbps (CDC wire case)

    Logic : hard-coded -> FPGA

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Belle-II TRG System

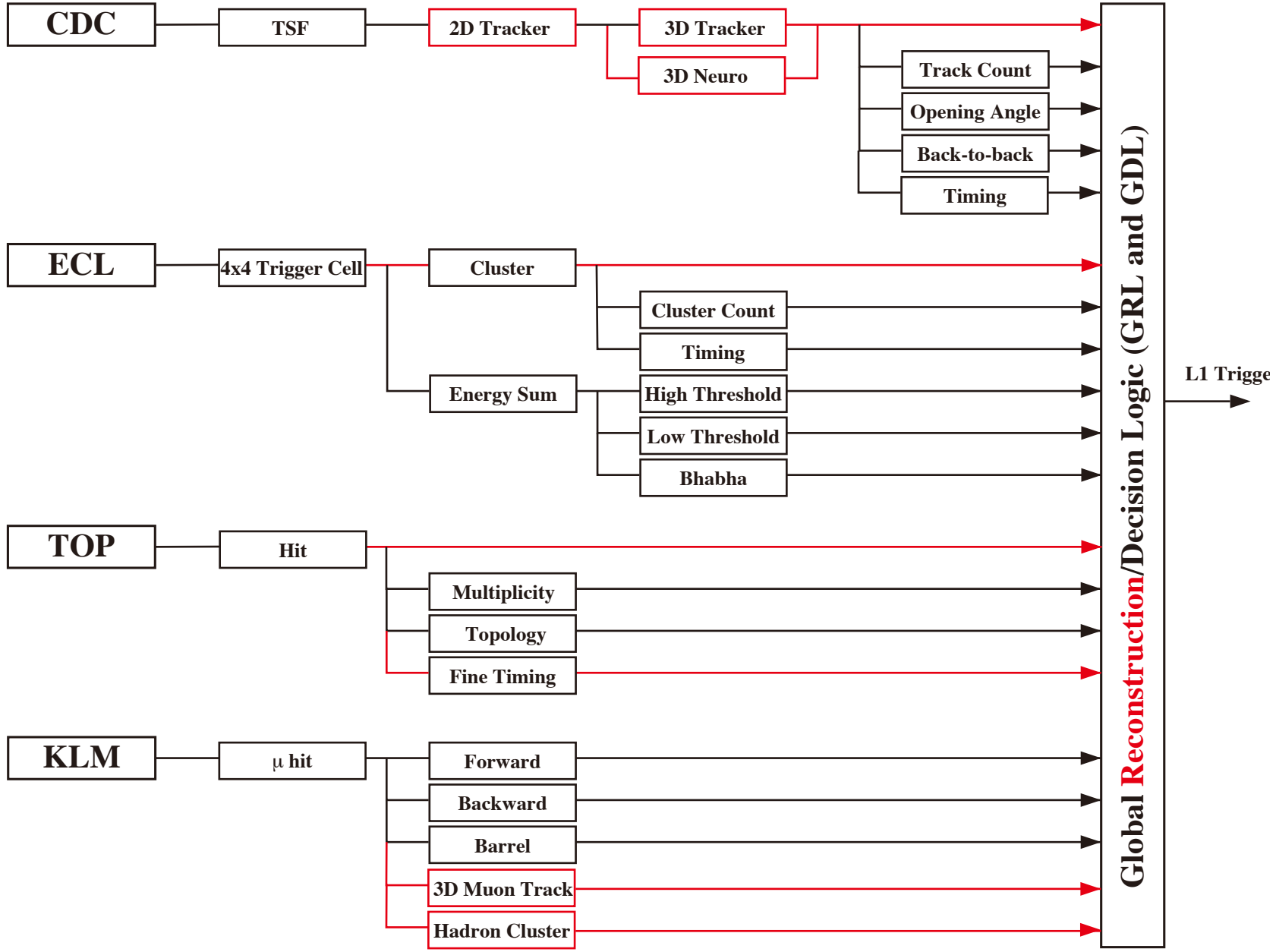
Korea U.
National Taiwan U.
Fu Jen Catholic U.
National United U.
KIT
TUM
KEK

Hanyang U.
BINP

U. Pittsburgh
U. Hawaii

Virginia Tech
U. Hawaii
Indiana U.

National Taiwan U.
KEK



New in Belle II

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Sub-Triggers

- **CDC : for charged tracks (barrel only)**
  - **Momentum measurements : 2D and 3D**
  - **Impact parameter : dz (no dr)**
  - **Track counting : up to 12 tracks / charge**
  - **Event timing : jitter ~ 30ns**
  - **Event topology : back-to-back, opening angles, etc**
- **ECL : for neutral and charged tracks**
  - **Energy sum**
  - **Position and energy measurements : cluster by cluster**
  - **Cluster counting**
  - **Event timing : jitter ~ 30ns**
  - **Bhabha event ID**
- **TOP : for timing for charged tracks (barrel only)**
  - **Event timing : jitter < 10ns**
- **KLM**
  - **Muon tracking**

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L1 Latency

- **L1 total latency budget : 4400 ns (was 4900 ns)**
  - **UT3 to UT3 latency (GTH, 11Gbps) : 380 ns**

- **Sub-trigger latency budget**
  - **Parallel sub-systems : 3800 ns (including sub->GRL transmission)**
  - **GRL : 140 + 380 ns**
    (GRL : 700 -> 140 ns : GRL can do simple matching only)
  - **GDL : 100 ns**
  - **Total : 4420 ns**

- **Latency budget is quite tight for GRL and GDL**
  - **Most of latency reservation for future extension was cut off due to the longer latency of L1 distribution inside SVD**
  - **TRG group strongly request to SVD group to reduce the latency of L1 distribution as much as possible**
  - **Even 50 ns reduction can help TRG (GRL) decision**

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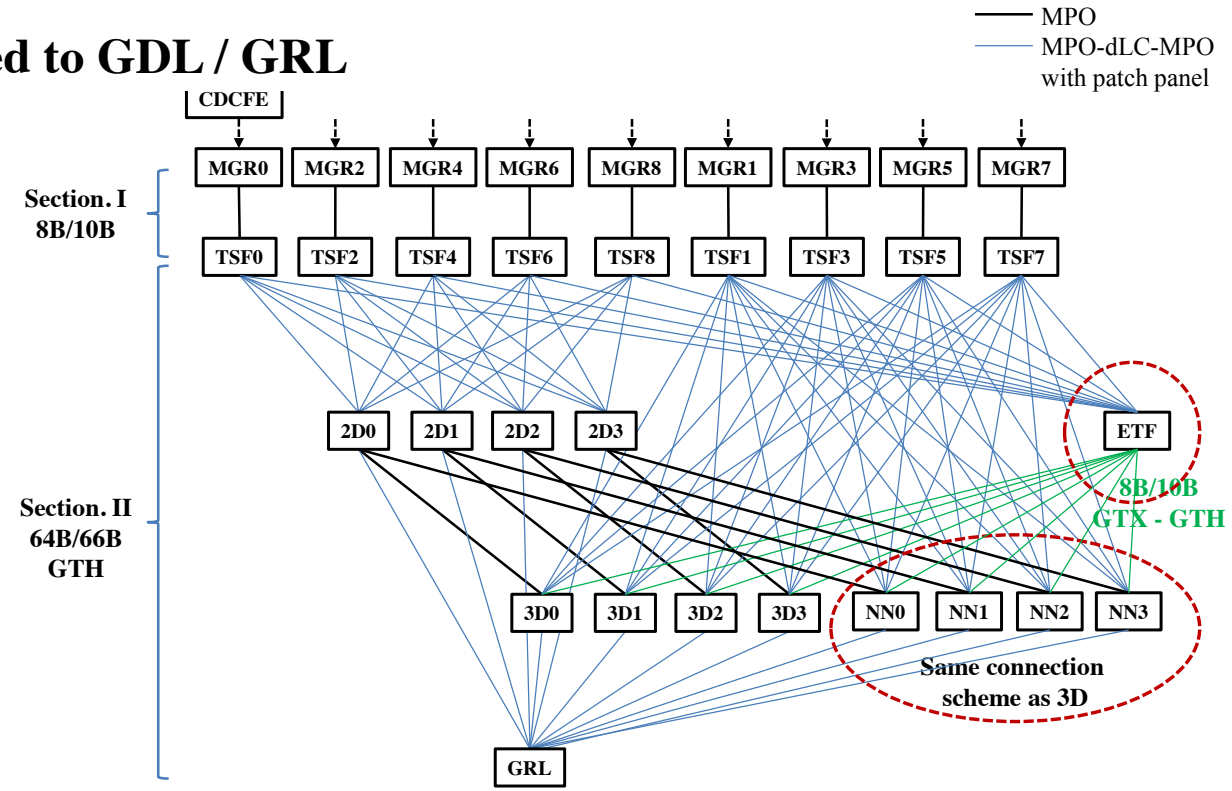
TRG Data Flow

- **Raw level protocol was developed (Y.T. Lai)**
  - **To synchronize data timing of connected modules**
  - **Prepared for GTP(8b10b) / GTX(8b10b) / GTH(64b66b)**

- **Used for**
  - **Entire CDC trigger**
  - **Sub-trigger connected to GDL / GRL**



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Technical Issues to Be Solved / Improved

- **Firmware download problem (Merger)**
  - **We can not download a firmware to some mergers**
  - **No cure is found so far**
  - **We will replace FPGAs on such mergers**
- **Instability of making data flow (Merger, UT3)**
  - **Example : Merger-TSF in CDC trigger**
  - **Number of lanes between Merger-TSF : 73x4=292 (8b10b, GTX)**
  - **Fraction of successful link-up lanes after power-on : about 90%**
  - **Unsuccessful lanes should be reset until link-up**
  - **GTH (64b66b) has similar issues**
  - **Investigate negotiation process to improve successful rate**
- **Instability of making firmware with GTH (UT3)**
  - **Example : TSF-2D in CDC trigger**
  - **Some GTH lanes can not be link-up when resource usage is quite high**
  - **Modifications on irrelevant logic may cause link-down of GTH lanes**
  - **Position of link-down lanes are depending on firmware compilation**
    - **This is not seen in GTX case**
  - **Ask Xilinx to improve situation**

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UT4

- **Development started**
  - **For more precision in logics : bigger resource size, higher data transfer**
  - **For replacement of UT3**
- **FPGA : Xilinx Ultra-scale XCVU080**
  - **GTY x32 : 0.5 - 30.5 Gbps**
  - **GTH x32 : 0.5 - 16.3 Gbps**
- **Optical module**
  - **QSFP28 x16 : up to 25 Gbps**
  - **Stacked QSFP**
- **Development schedule**
  - **Specification : by 2016/06**
  - **Bidding : 2016/08**
  - **Fabrication : 2016/12**
  - **Delivery : 2017/01**

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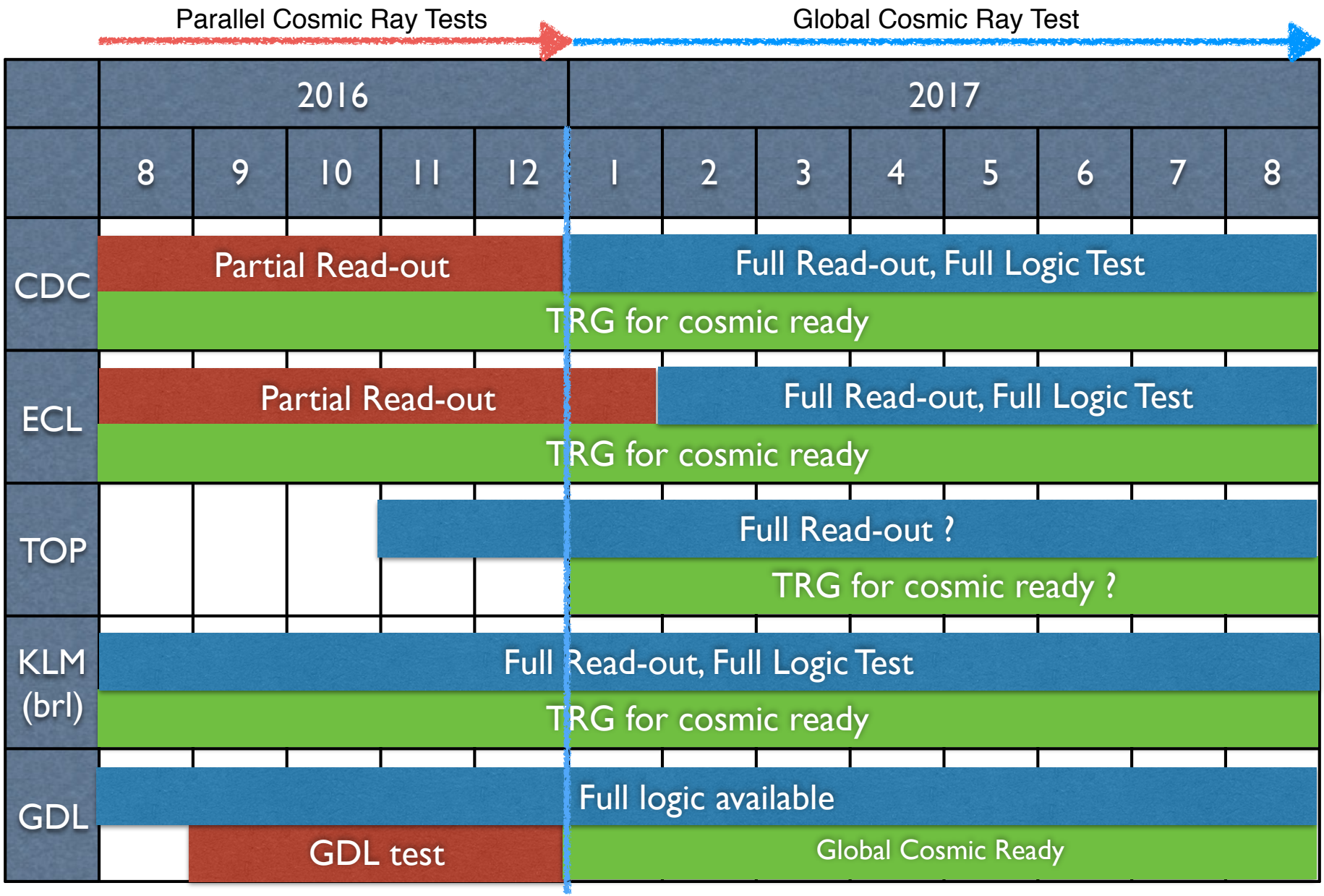
TRG Schedule in 2016



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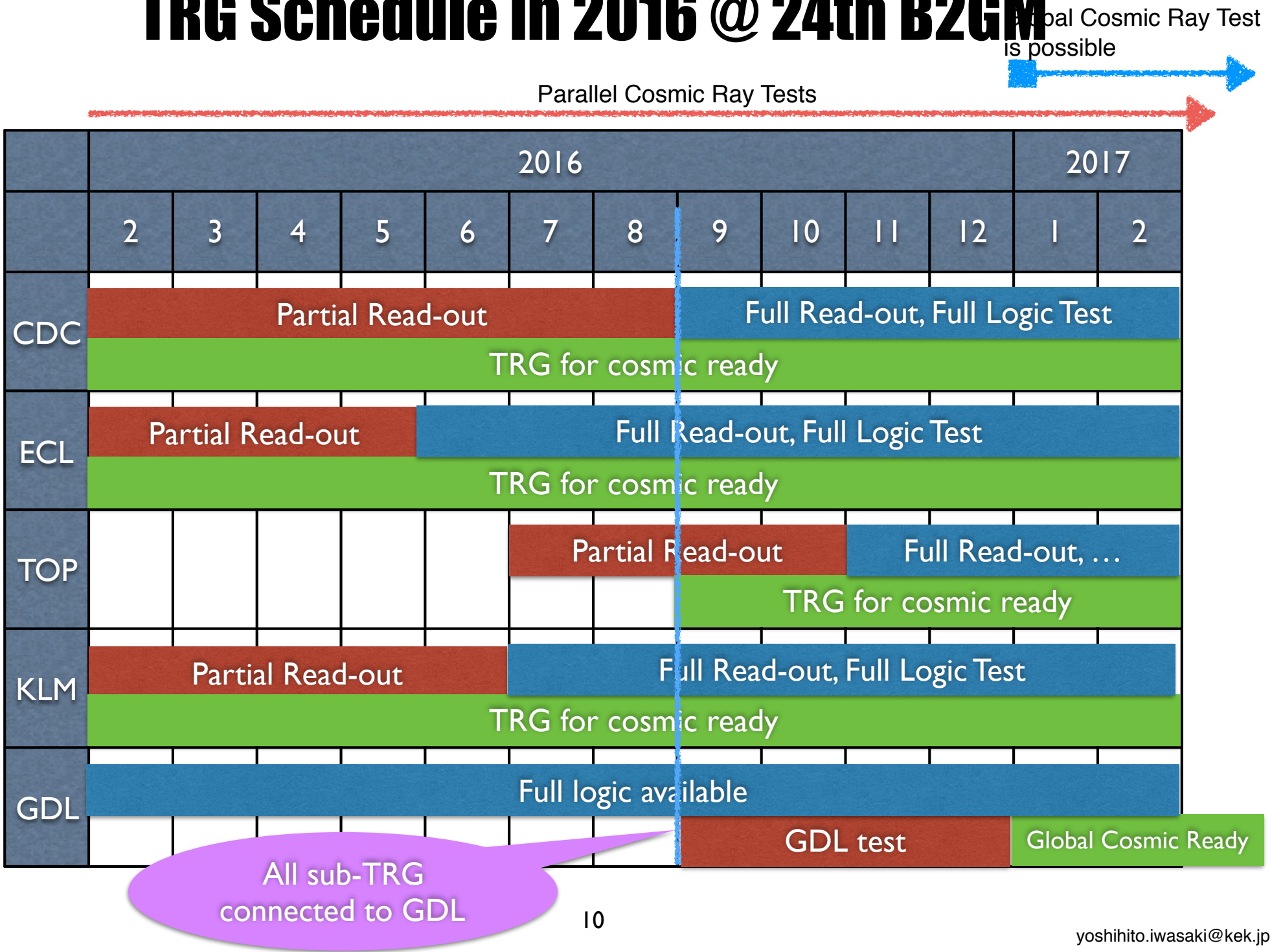
TRG Schedule in 2016 @ 24th B2GM



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