ECL trigger status

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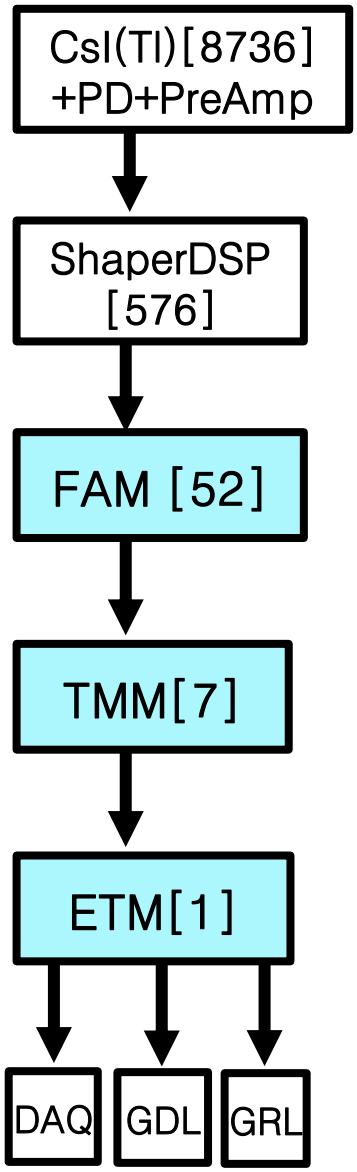
2016/09/3-5 TRG/DAQ Workshop

Contents

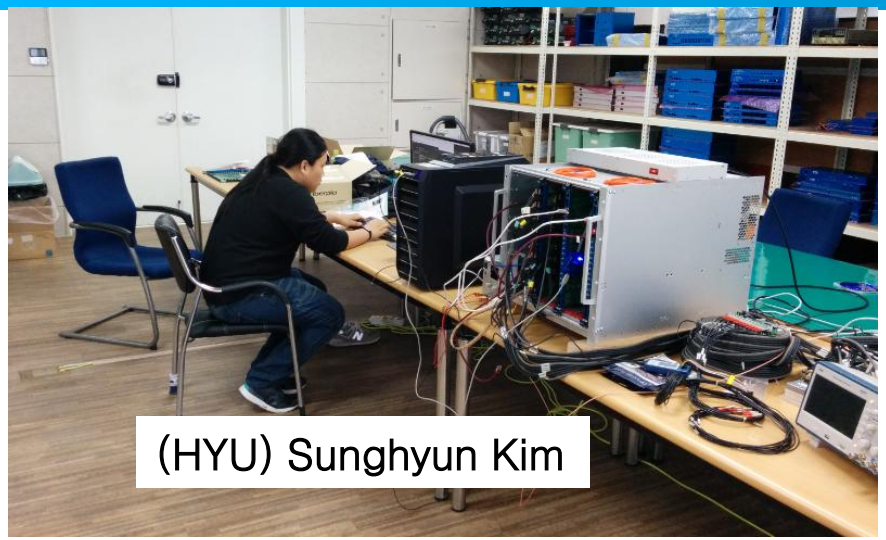
- Introduction(ECL trigger)
- FAM/TMM mass production/installation
- Optical link issues
- Control and monitoring system
- ECL trigger server
- Summary/Plan

Belle2 ECL trigger system



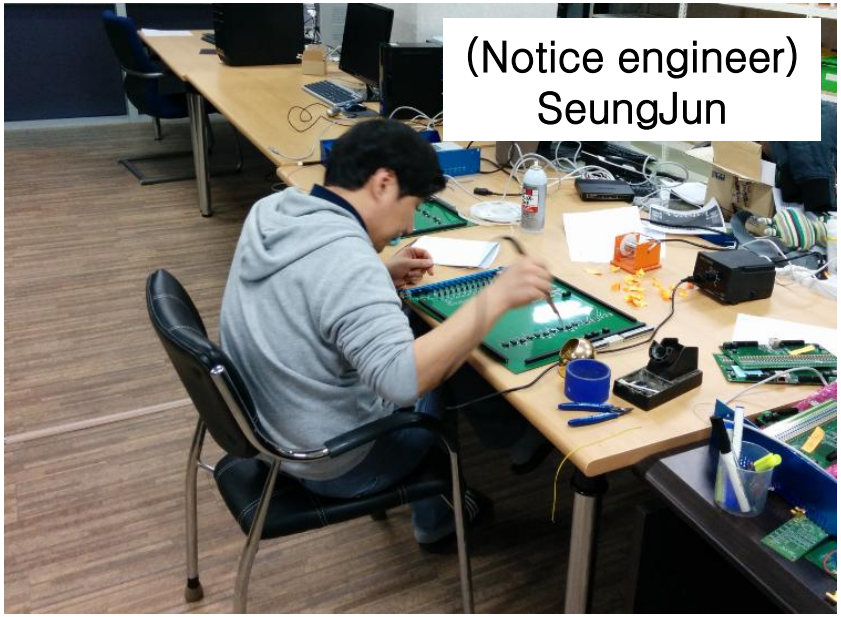
- FAM
  - Receive 576TC analog data from ShaprDSP
    - 1TC consists of 4x4=16Xtals
  - Digitization with FADC
  - TC E&T rec. by waveform analysis(χ^2 fit) on kintex7
- TMM
  - Play an role of merger w/ kintex7
- ETM
  - Make a ECL trigger decision by all TC E&T on virtex6
  - Send ECL trigger summary to GDL
  - Send cluster data to GRL
  - Send fired TC E&T to HSLB
- 1st version of firmware for FAM/TMM/ETM are ready
- 1st version of control & monitoring software are ready.

ECL trigger manpower


(HYU) Sunghyun Kim


(HYU) InSoo Lee

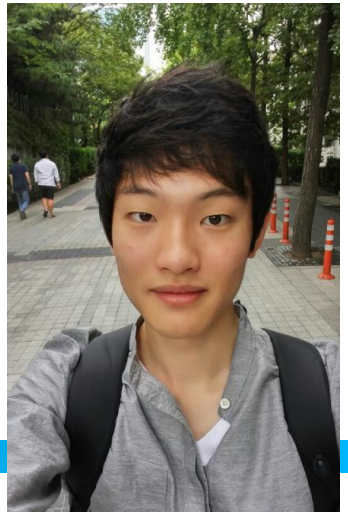
(Notice director)
SangYeol Kim


(Notice engineer)
SeungJun

New students from Korea University

(KU) Wonji Choi

(KU) YoungJun Kim

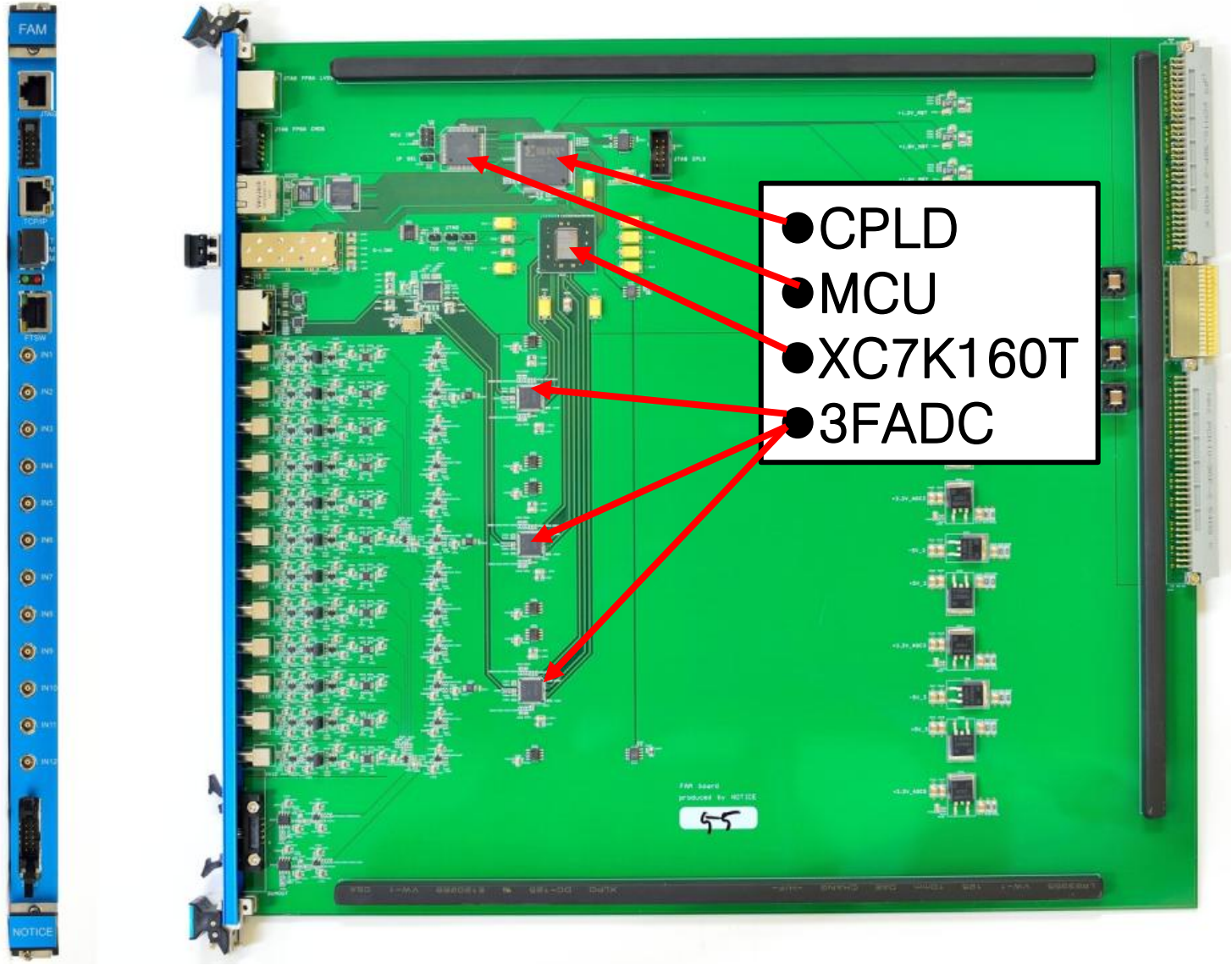


FAM/TMM mass production/installation

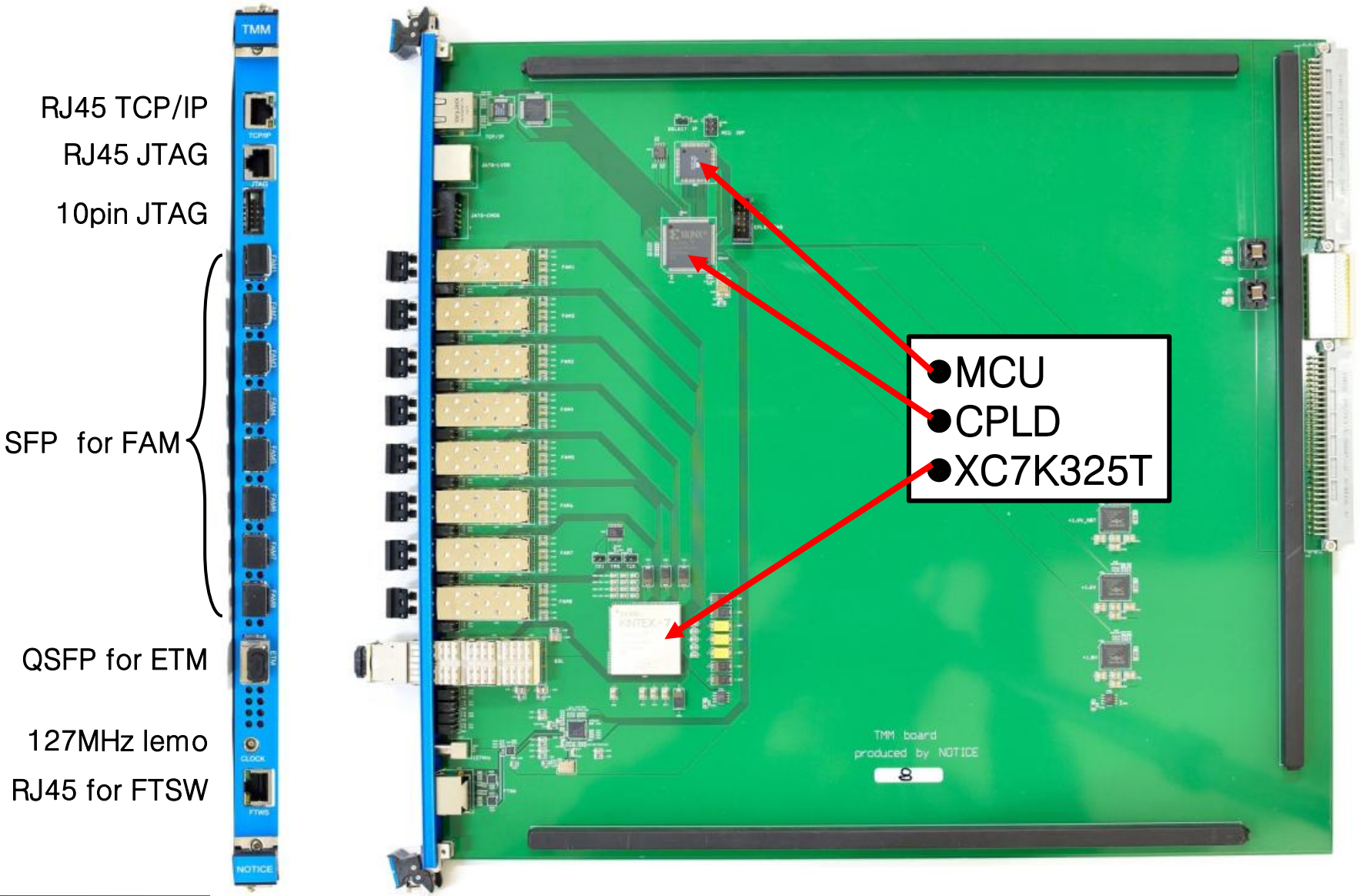
- (Feb/??) FAM mass production started.
- (Mar/19) FAM mass production done.
- (Mar/21) FAM test started @ Notice.
- (Apr/08) TMM mass production started.
- (Apr/25) TMM mass production done.
- (Apr/25) TMM test started @ Notice.
- (Apr/30) TMM test done @ Notice.
- (May/11) FAM test done @ Notice.
- (May/26) FAM/TMM cable labeling, cabling started.
- (Jun/13) FAM and TMM delivered at KEK.
- (Jun/15) FAM and TMM installation to E-hut/Belle2 done!

- FAM
  - 60(52+8) FAM produced
  - 57 in KEK and 3 in Notice
- TMM
  - 10(7+3) TMM produced
  - 9 in KEK and 1 in Notice

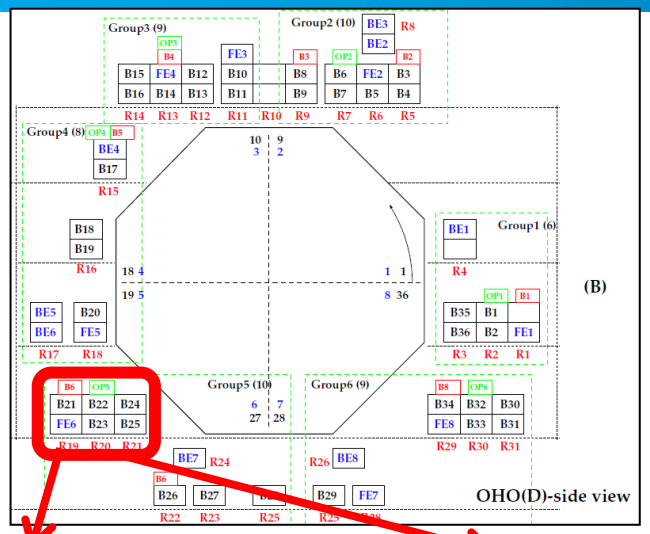
FAM


RJ45 JTAG
10pin JTAG
RJ45 TCP/IP
SFP
RJ45 FTSW
12 analog Input
analog sum output
FAM
NOTICE
CPLD
MCU
XC7K160T
3FADC

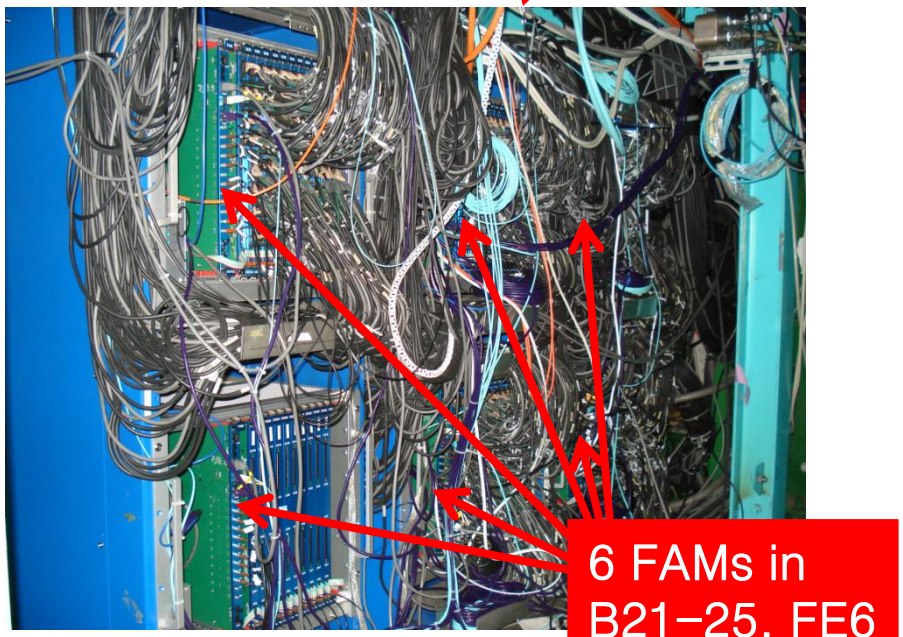
TMM

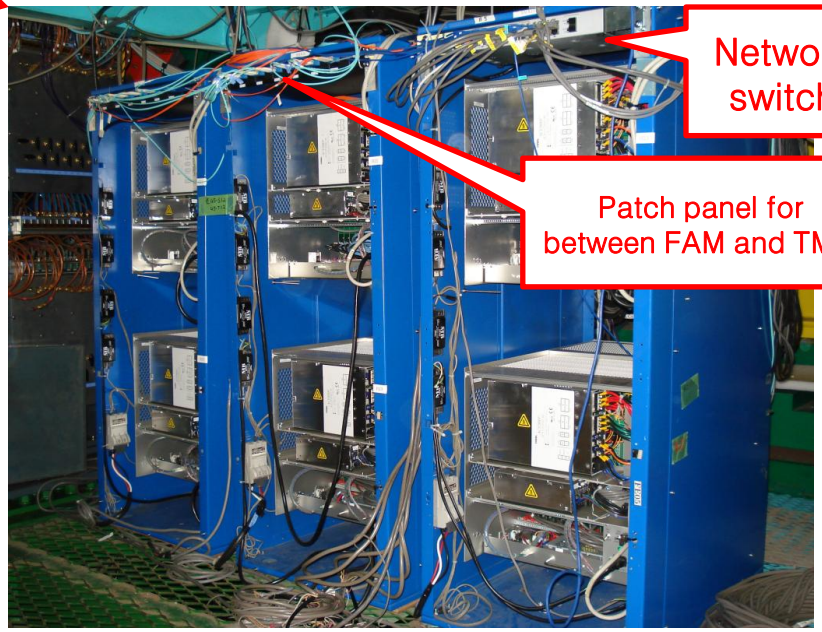

RJ45 TCP/IP
RJ45 JTAG
10pin JTAG
SFP for FAM
QSFP for ETM
127MHz lemo
RJ45 for FTSW
TMM
NOTICE
MCU
CPLD
XC7K325T
TMM board
produced by NOTICE

FAM (@ detector)

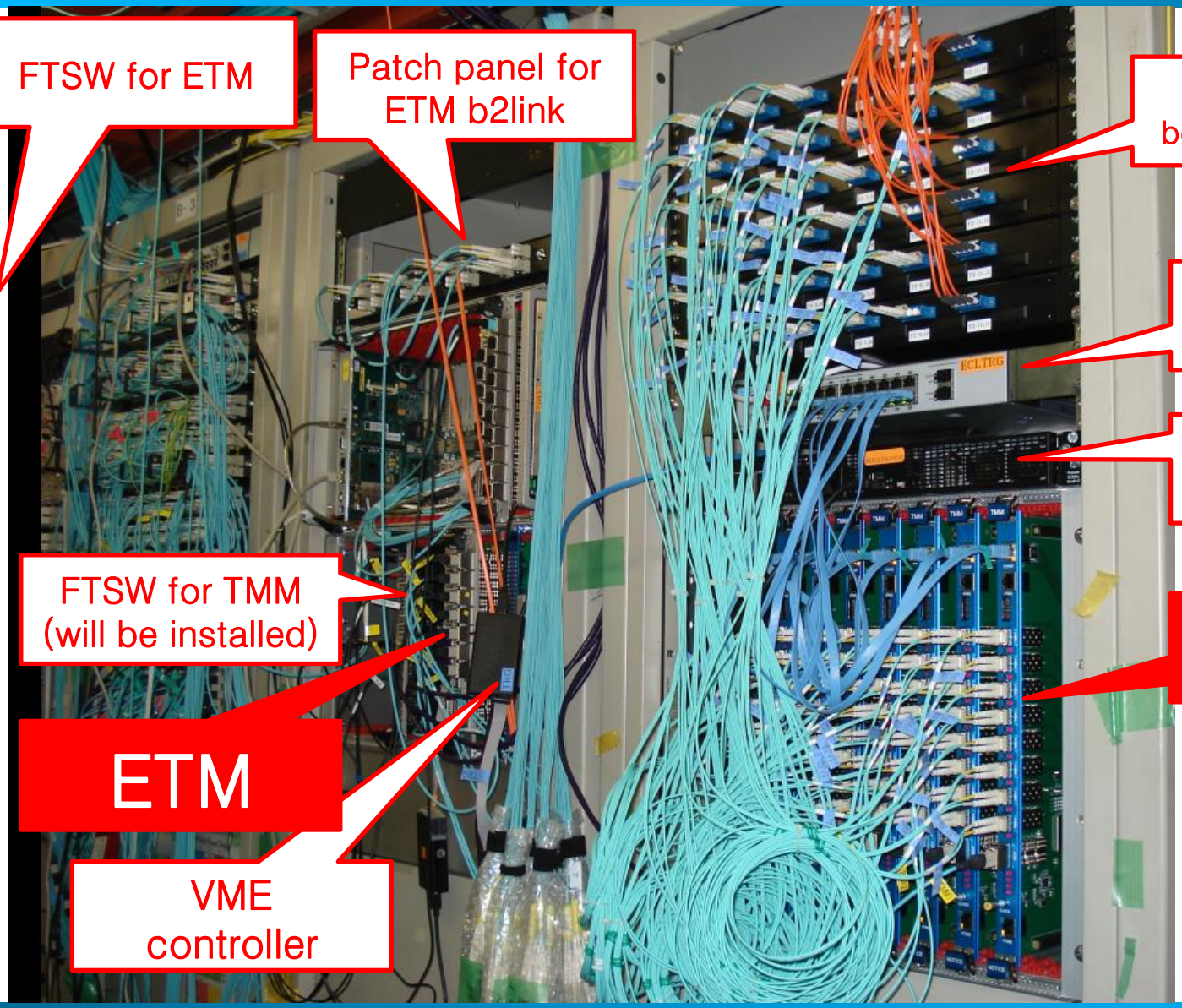


- 52 FAMs have been installed to 52 VME crates around Belle2.
- All cables are connected except for luminosity monitor
  - LC pair
  - Cat7 for FTSW
  - Cat5 for TCP/IP
  - Lemo for ShaperDSP





TMM and ETM (@E-hut)



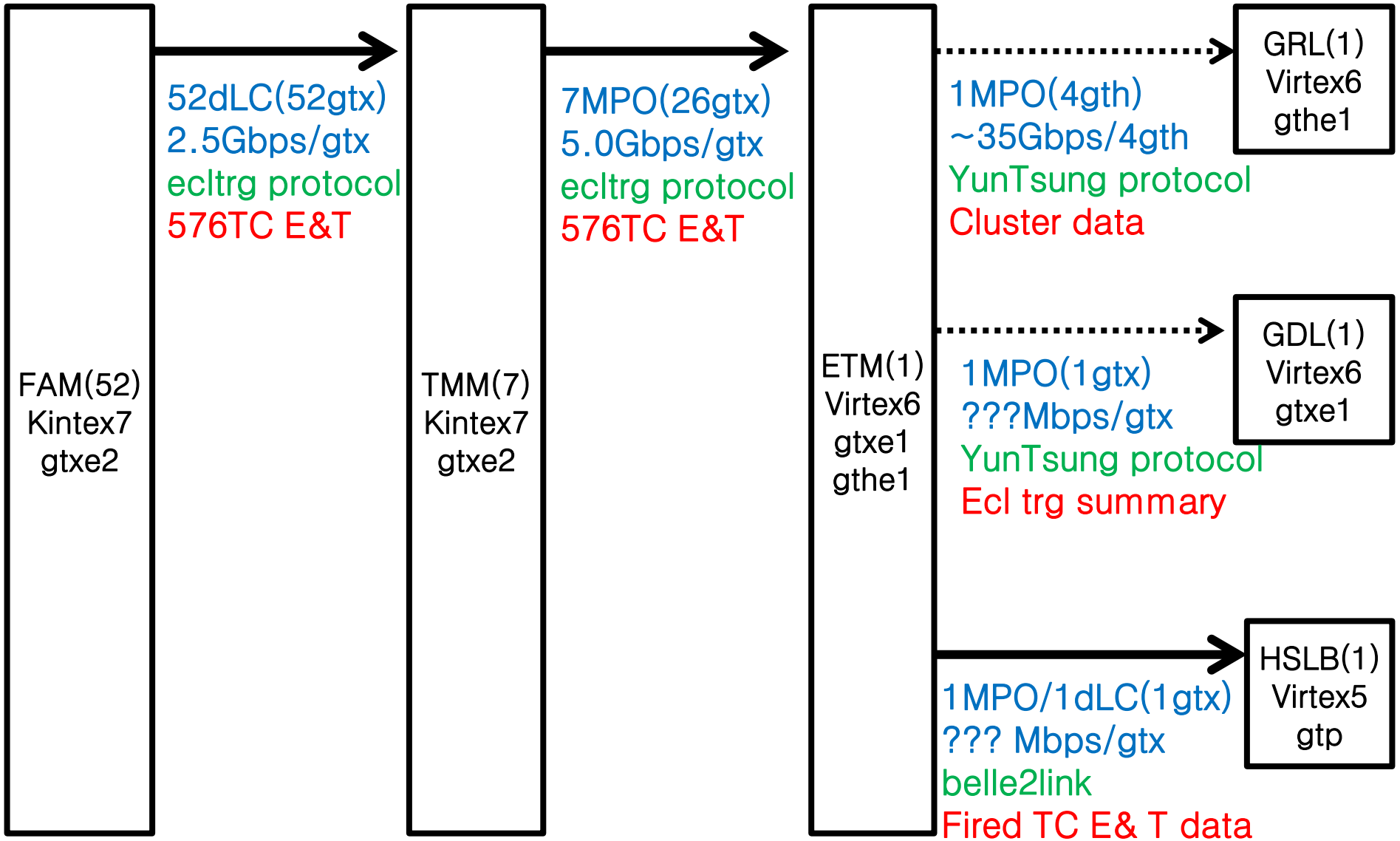
Optical link issues

(1)Data misalignment problem
- FAM→TMM
- TMM→ETM

(2)Link up instability after reboot
- TMM→ETM

(3)Link instability after link up
- FAM→TMM
- TMM→ETM

Optical link



Optical link(data format)

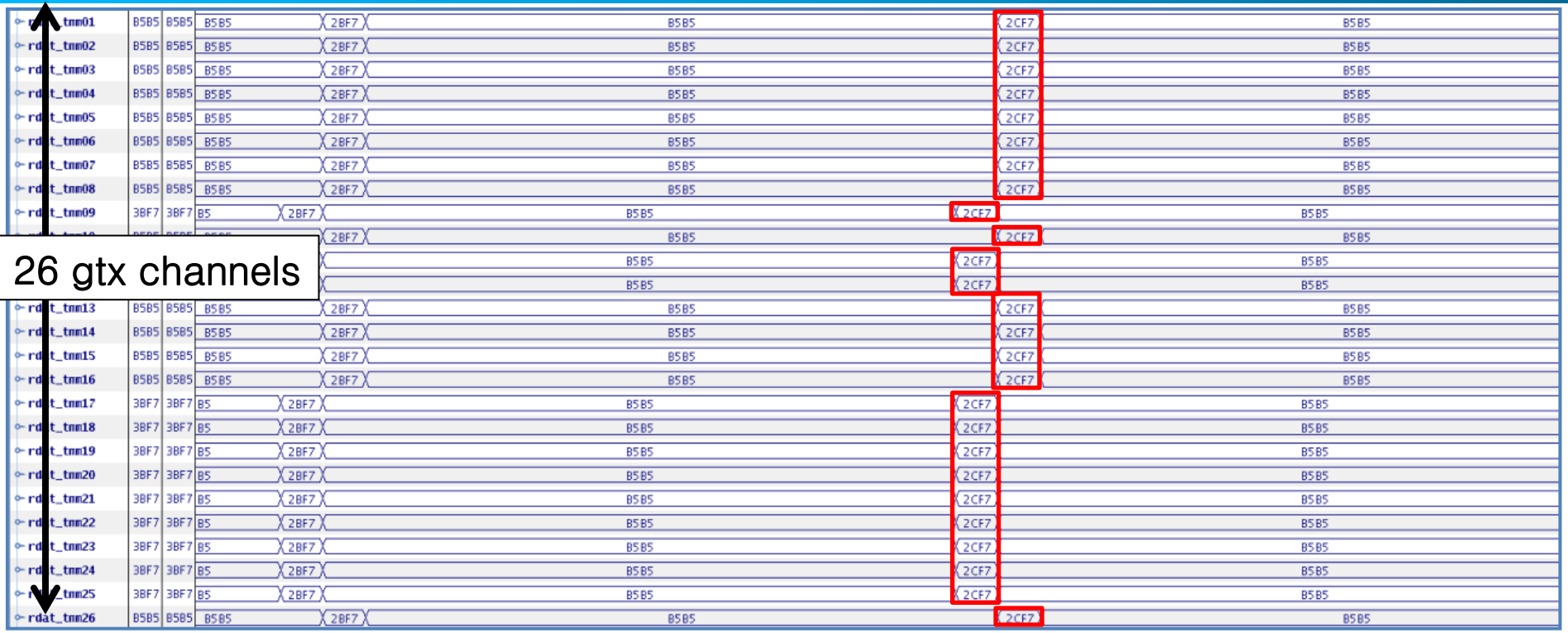
- FAM↔TMM (1gtx)

  - 16 bit HEADER & 12 x 20 bit TC data = 256 bit
  - by 16 clock with 127MHz (= 1 clock with 8MHz)

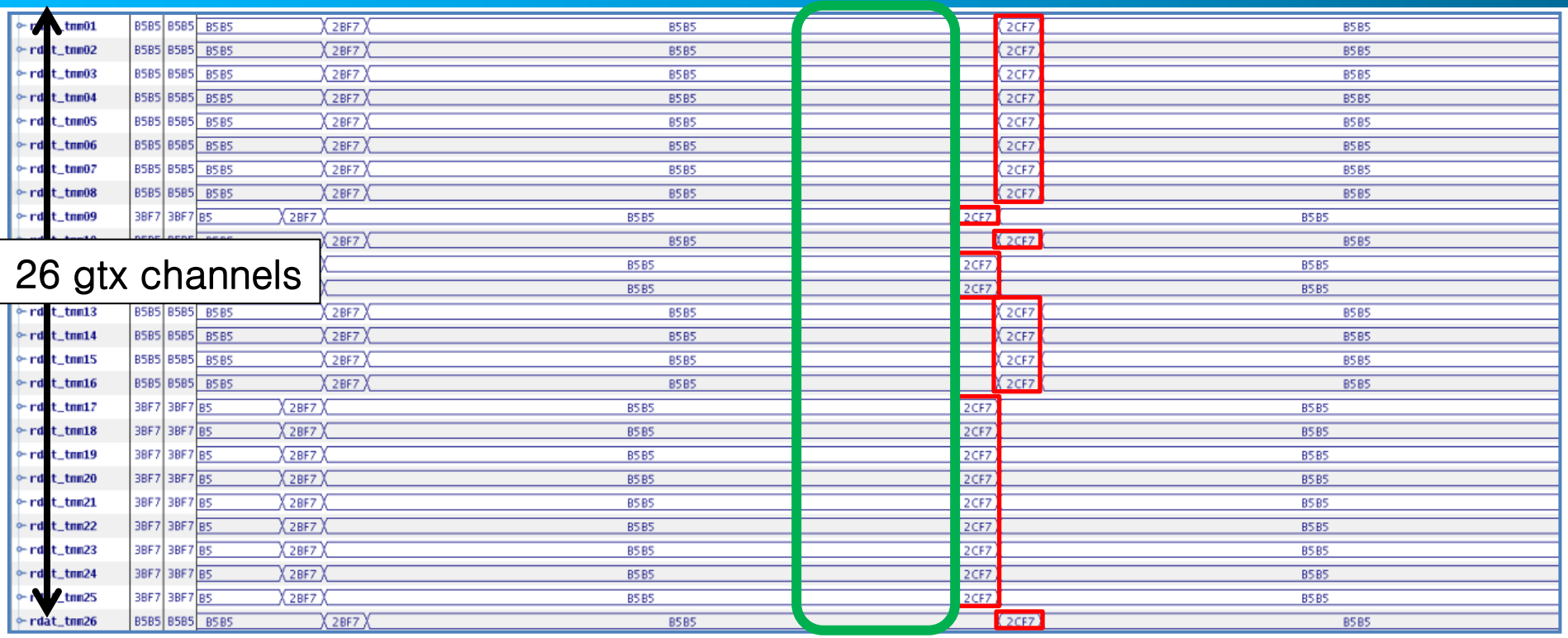
  - HEADER = 0 & revoclk(10 downto 4) & 8bit K-character
  - 16 bit data = a part of TC data or B5B5
  - TC data = 12TC x 20bit(1TC) = 240bit
  - 1 TC data = 1bit(hit) & 7bit(timing) & 12bit(energy) = 20bit
    - 7bit(timing) is from fitter, LSB=1ns.

- TMM↔ETM (1gtx)
  - Data format is (almost) same as FAM↔TMM
  - 2 FAM data by 1 gtx are sent simultaneously.
  - # of bit with 1 clock is 512 bit.

(1)Data misalignment (TMM→ETM)

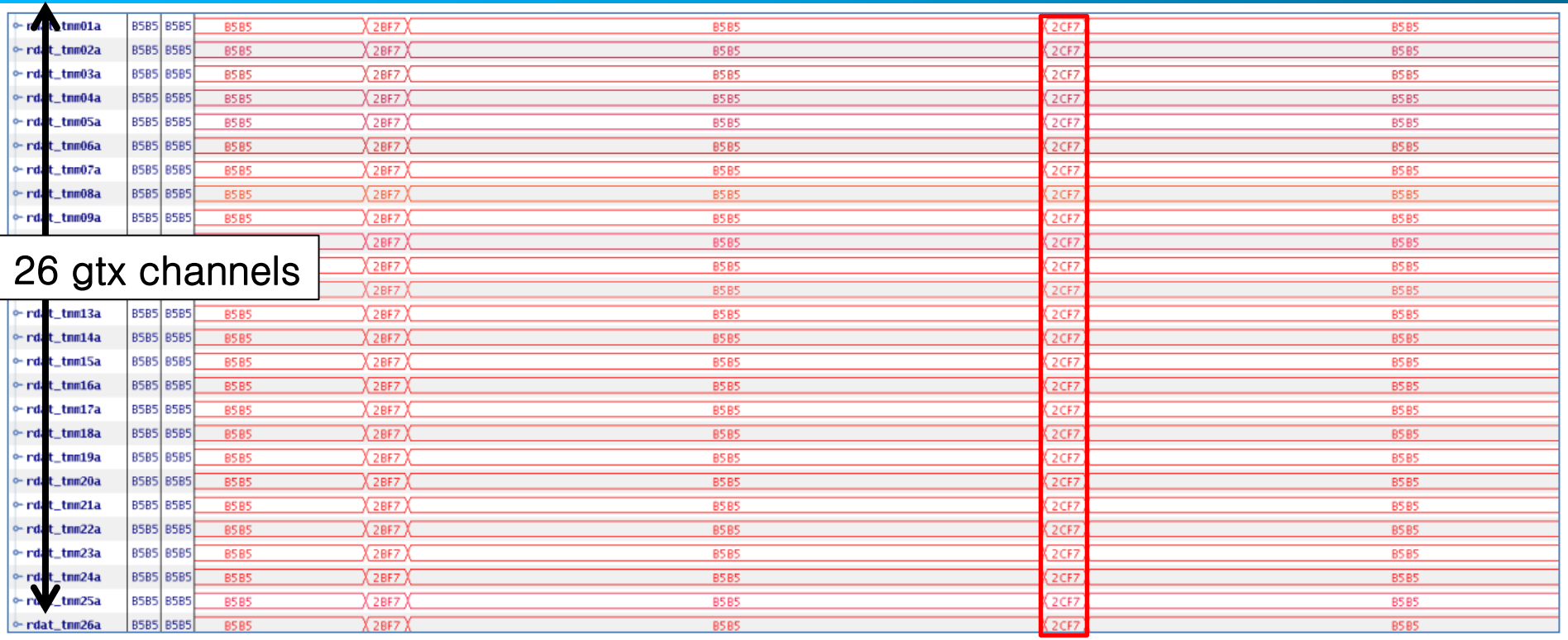


(1)Data misalignment (TMM→ETM)



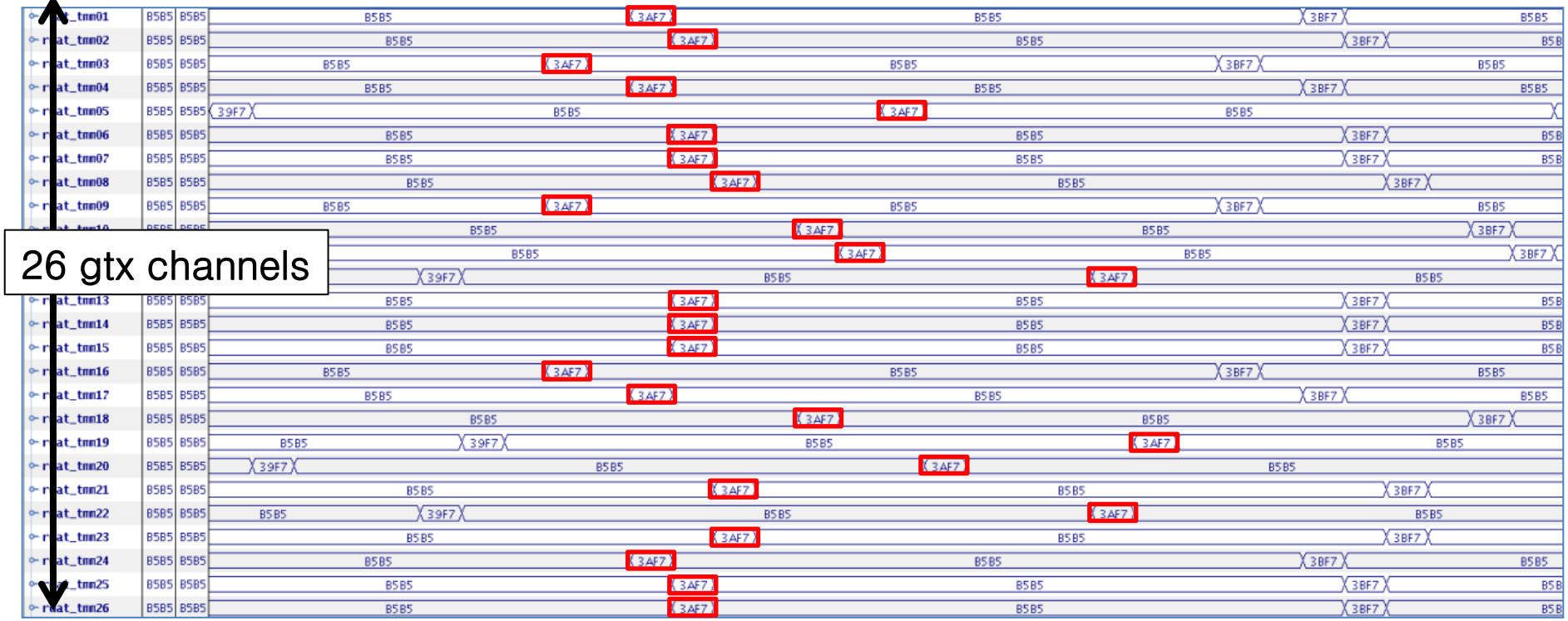
- Alignment logic
  - Check all gtx data are B5B5 for a few clocks
  - Check each header delay from earliest header
  - Align each channel based on measured delay with 16bit Serial Register LUT.
- Alignment logic is active only for link up channel.
- Additional latency due to alignment is 8 to ~100 ns.
- Alignment results can be monitored by ecl trigger server.

(1)Data misalignment (TMM→ETM)



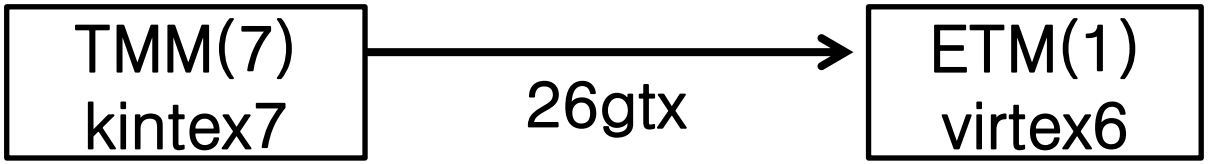
- Same logic was implemented in FAM→TMM too.
- Alignment logic is working (almost) perfectly.
- In some special case, this logic does NOT work.
  - TMM reboot after ETM is up

(1)Data misalignment (TMM→ETM)



- When TMM reboot after ETM up, data shifts are too bad…
- Solution: Send gtxrxreset to all 26 gtx on ETM by hand.
- Plan: better to implement an automatic recovery logic.

(2)Link up instability of TMM→ETM after reboot



- Many links didn't go to up state after reboot or power-up
  - There was a bug to do gtxtxreset & gtxrxreset
    - Some of links were still down.
  - Prepare pllrxreset signal
    - All 26 gtx links were up.
    - But, pllrxreset always has to be sent after rebooting.
  - Sunghyun and SangYeol found source of this problem.
    - minimum unit of TMM→ETM is 40bit(32x10b/8b)
    - Kintex7 maximum bitslip = 40
    - Virtex6 maximum bitslip = 20
    - This problem was gone by implementing a patch to ETM
      - Additional latency is 1clock(=8ns).

(3)Link instability after link up

- Some links were down(and automatically recovered)
  - 8/20-21(48hour monitoring)
    - FAM-TMM: FAM52 2down
    - TMM-ETM: ch22 17down, ch23-26 1down
  - 8/23 (12hour monitoring)
    - FAM-TMM: FAM25 1down, FAM34 3down (b2tt down)
    - TMM-ETM: ch13-16 2down, ch17-20 4down, ch21 2down

- Removing and inserting QSFP mitigates the problem…
  - Planning to replace QSFP
- Preparing monitoring firmware logic to check in details
  - How long time link is down: ~50μs
  - Which signal in link up/down definition have a problem

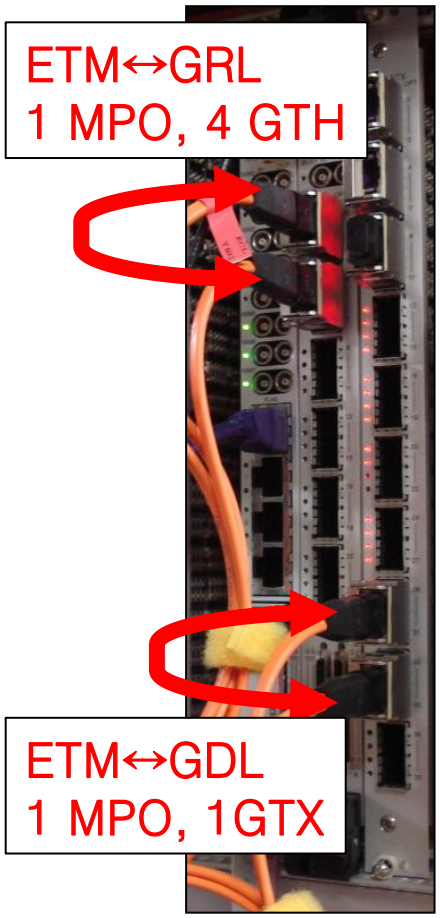
FAM b2tt down problem

- FAM b2tt down happened
  - Before KEK shutdown: FAM 45
    - Fixed by disconnecting&connecting LAN cable(FTSW)
  - 8/18: FAM 20
    - Fixed by disconnecting&connecting LAN cable(FTSW)
  - 8/20-25
    - FAM 25, 34
    - Fixed by disconnecting&connecting LAN cable(FTSW)
  - 9/1~
    - FAM 35

- Detail investigation is needed, but it might take time to fix…

Link status on ETM→GDL and GRL

- YunTsung prepared designs of ETM→GDL and GRL links.
- Testing w/ single UT3 w/o actual ETM firmware by chipscope.



- Latency check

	v1	v2
ETM→GDL	~1.1μs	0.47μs
ETM→GRL	~0.9μs	0.31μs

- Data misalignment in ETM→GRL(4gth)

- Plan to do more check.
- Logic(ETM→GDL) will be implemented to ETM as top priority after TRG/DAQ workshop.

Control & Monitoring system

FAM

```
=======================================
  0  : Quit
  1  : Status
  2  : Reset general monitor param
  3  : R temparature
  4  : R pedestal
  5  : R TC E threshold
  6  : R TC hit rate
  7  : R TC hit rate(maximum)
 10  : R TC E/T rec. type
 11  : W TC E/T rec. type
 12  : Set basic parameters
 13  : Set LUT for fitter
 20  : Reboot
 21  : (X not ready)Firmware download
=======================================

Select action?
1
firmware version : FAM(63), b2tt(46)
clock            : OK
NClkDwn          : OK
b2tt             : OK
Nb2ttDwn         : OK
gtxlink          : OK
NgtxlinkDwn      : OK
```

TMM

```
================================
 0   : Quit
 1   : status
 2   : general monitor reset
 3   : fam data align status
10   : link down check(temporal)
20   : reboot
================================

Select action?
1

firmware version : TMM(27), b2tt(46)
-------------------------------------------------------------------------------------------------
TMM #     :        1         2         3         4         5         6         7
-------------------------------------------------------------------------------------------------
clock     :        1         1         1         1         1         1         1
clk NDwn  :        0         0         0         0         0         0         0
b2tt      :        1         1         1         1         1         1         1
b2tt NDwn :        0         0         0         0         0         0         0
fam link  : (11111111) (11111111) (11111111) (11111111) (11111111) (11110000) (11111111)
fam NDwn  :       OK        OK        OK        OK        OK        OK        OK
etm link  :    (1111)    (1111)    (1111)    (1111)    (1111)    (1100)    (1111)
etm NDwn  : (0 0 0 0) (0 0 0 0) (0 0 0 0) (0 0 0 0) (0 0 0 0) (0 0 0 1) (0 0 0 0)
temp.     :  (28, 26)  (28, 26)  (28, 26)  (28, 26)  (28, 26)  (28, 26)  (28, 25)
-------------------------------------------------------------------------------------------------
TCHitRate(Hz) :
-----------------------------------------------------------------
(ch #):    1    2    3    4    5    6    7    8   (tot)
-----------------------------------------------------------------
TMM 1 :    0    0    0    0    0    0    0    0 (    0)
TMM 2 :   59   52   56   47   47   49   60   55 (  425)
TMM 3 :   65   56   56   40   56   49   68   60 (  450)
TMM 4 :   54   70   55   48   54   52   55   66 (  454)
TMM 5 :   60   57   59   67   51   50   47   56 (  447)
TMM 6 :   51   45   46   46    0    0    0    0 (  188)
TMM 7 :    0    0    0    0    0    0    0    0 (    0)
-----------------------------------------------------------------
```

- All 52FAM, 7TMM, ETM, 576TC can be controlled & monitored.
- Keep updating control & monitoring system.

Monitoring system(TC hit rate/FAM)

- Total TC hit rate of each FAM.
- TC energy threshold = 30 ADC ~ 100MeV.

Typical hit rate (8/22)

FAMHitRate(Hz) :

(ch #) :	1	2	3	4	5	6	7	8
TMM # 1:	0	0	0	0	0	0	0	0
TMM # 2:	59	66	66	69	73	55	65	48
TMM # 3:	68	54	61	60	66	59	57	57
TMM # 4:	66	60	58	62	52	56	70	60
TMM # 5:	60	65	50	55	68	83	56	44
TMM # 6:	42	46	46	57				
TMM # 7:	0	0	0	0	0	0	0	0

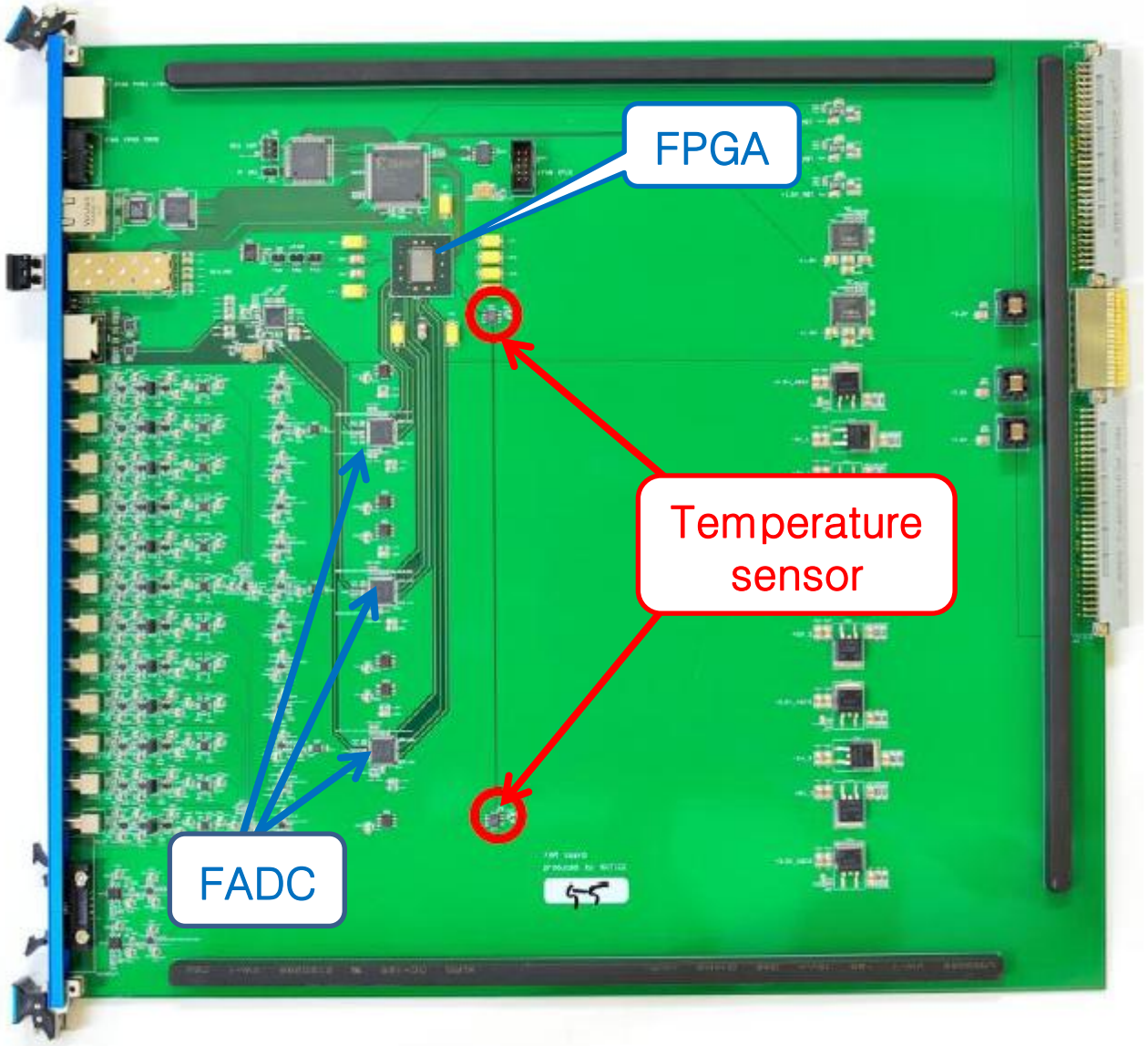
Maximum hit rate in 8/20-21(48h)

FAMMaxHitRate(Hz) :

(ch #) :	1	2	3	4	5	6	7	8
TMM # 1:	0	0	0	0	0	0	0	0
TMM # 2:	85	89	92	976	116	88	5451	2806
TMM # 3:	597	89	5036	172	94	88	85	84
TMM # 4:	85	88	3871	82	224	83	83	88
TMM # 5:	101	87	88	88	89	87	89	88
TMM # 6:	84	87	88	413				
TMM # 7:	0	0	0	0	0	0	0	0

- Hit rates are very high for some FAM sometimes
  - TC by TC hit rates were no monitored in this check.
  - Probably there were high noise sometimes(guess)
- Wonji and YungJun supervised by InSoo are preparing a program which monitors all TC noise as a function of time.

2 temperature sensor on FAM

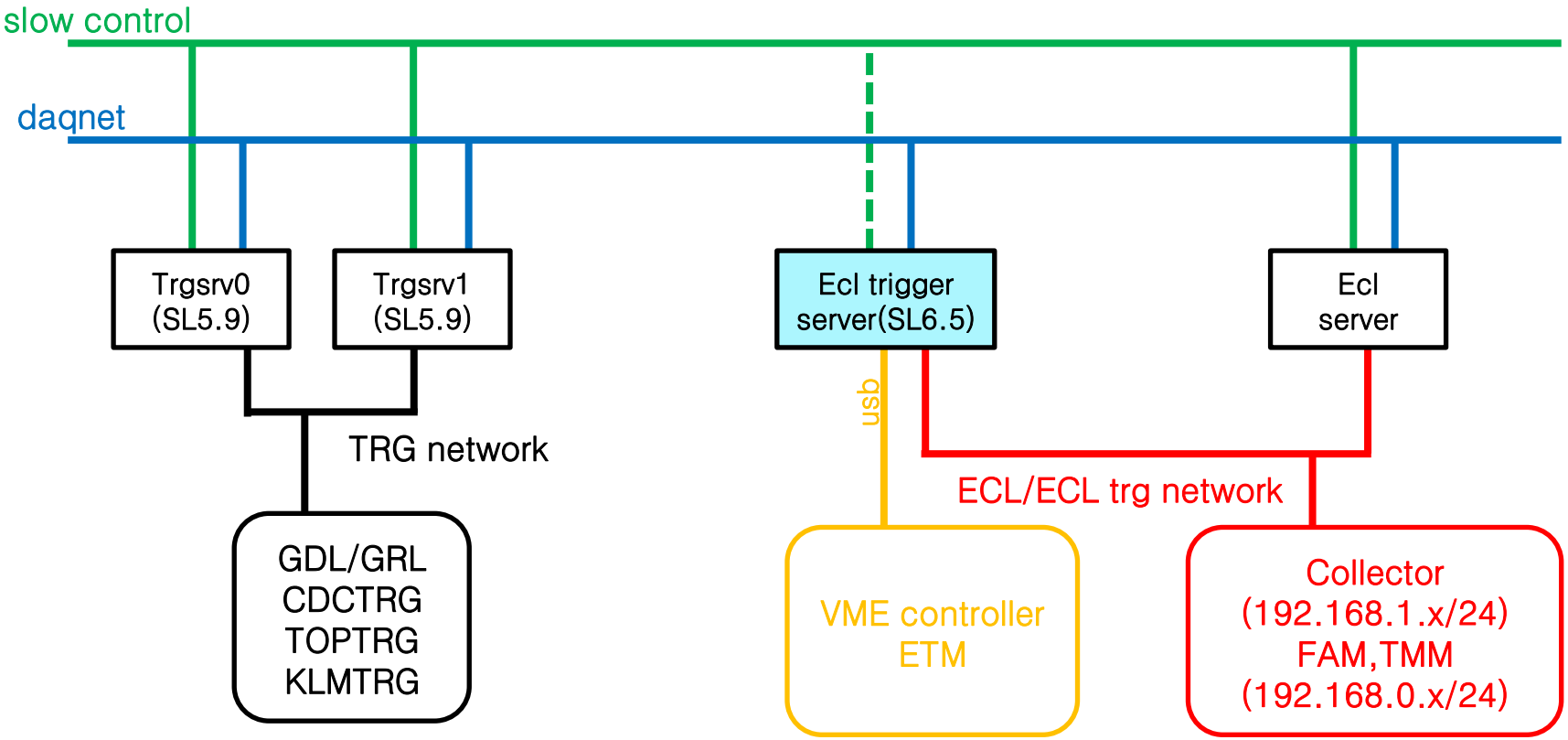


Monitoring system(temperature on FAM)

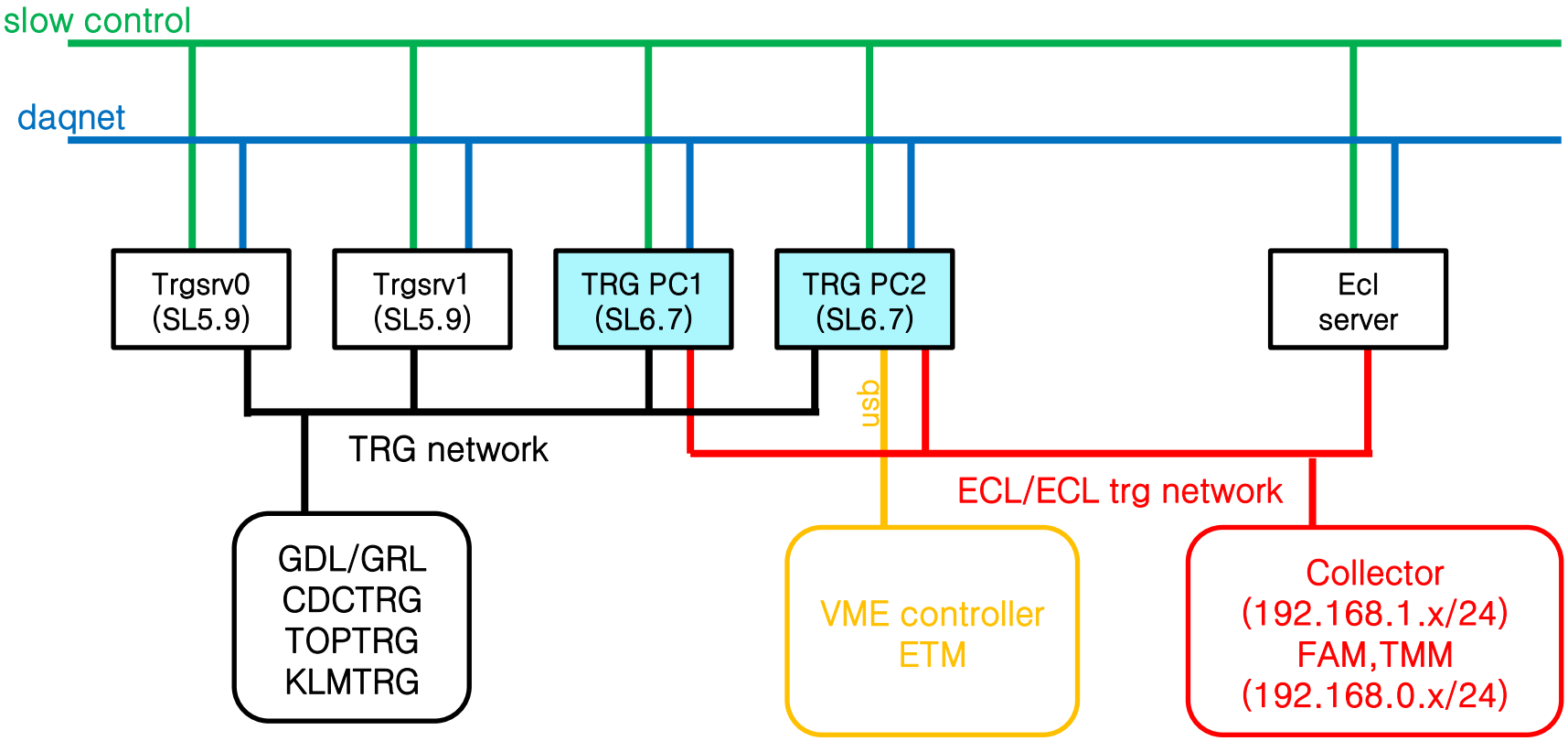
	1	2	3	4	5	6	7	8
TMM #1 :	(41, 34)	(38, 34)	(28, 24)	(29, 26)	(40, 32)	(30, 26)	(40, 32)	(34, 30)
TMM #2 :	(34, 32)	(32, 28)	(30, 27)	(29, 26)	(28, 26)	(29, 26)	(28, 25)	(29, 26)
TMM #3 :	(28, 25)	(30, 28)	(28, 26)	(30, 28)	(29, 26)	(30, 26)	(32, 27)	(28, 26)
TMM #4 :	(32, 29)	(32, 31)	(32, 30)	(32, 30)	(33, 29)	(33, 30)	(30, 28)	(31, 29)
TMM #5 :	(30, 28)	(30, 28)	(32, 29)	(34, 30)	(31, 28)	(32, 30)	(31, 28)	(34, 30)
TMM #6 :	(31, 28)	(32, 30)	(36, 31)	(32, 30)				
TMM #7 :	(40, 32)	(30, 27)	(28, 25)	(31, 30)	(41, 34)	(38, 32)	(38, 32)	(40, 33)

- Temperatures are in rage of 30–40°C
- The reason why 10°C difference appears is unknown…
  - Performance variation of VME fan ?
- Acceptable temperature of FPGA and FADC ~80°C
  - (some distance between sensor and FPGA/FADC)
- Wonji and YungJun with InSoo are preparing a program to monitor temperature as a function of time.
- Plan to measure FPGA temp. of FAM/TMM/ETM directly.

ecl trigger server/network(now)



ecl trigger server/network(new)



- Purpose of new TRG servers(TRG PC1 and PC2):
  - One of them is backup for another.
  - GUI server for GDL,GRL and all sub-trigger
  - ECL trigger sever
- Everything on current ecl trigger server will be moved to TRG PC1 and PC2.

Summary

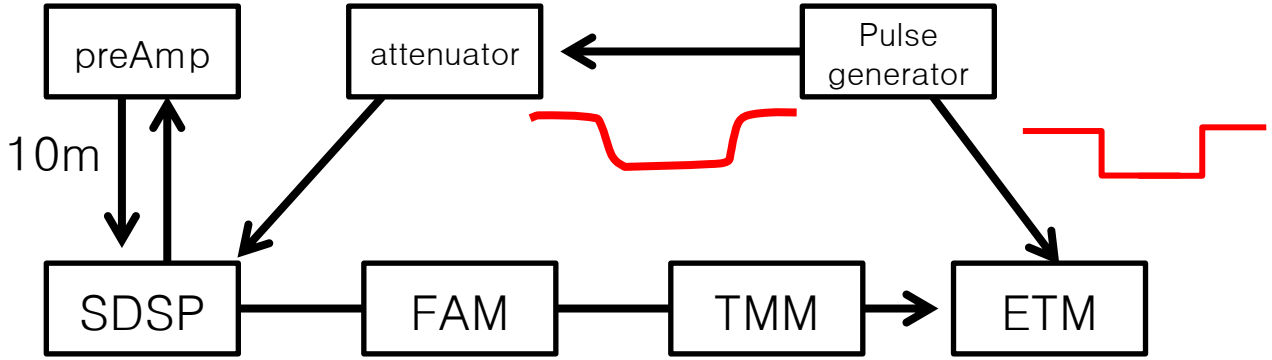
- Summary
  - All ECL trigger modules(FAM,TMM,ETM) installed.
  - Critical problems in optical links were fixed.
  - Working on ETM→GDL/GRL link, and full ecl trigger chain (FAM→TMM→ETM→GDL/GRL) will be ready soon(in Sep.)
  - Update of control & monitoring system is ongoing.

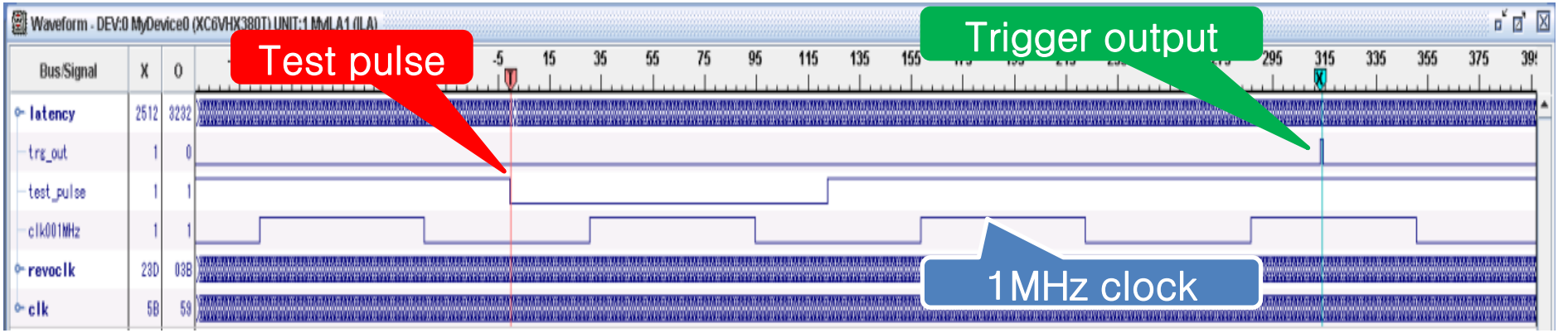
- Plan
  - ETM→GDL/GRL connection (Sep)
  - Investigate optical link and FAM b2tt issues(Sep)
  - Server replacement (Sep-Oct)
  - Slow control (Oct-)
  - Calibration study(TC E&T correction, fitter, pedestal, etc)
  - FAM fitter update(timing bias corr, double pulse fitter)
  - Link protocol update(to control all module by ETM)

backup

Latency measurement

- Latency at ETM output must be < 3.5–3.7μs
- Yuriy prepared test pulse generator for us.





- Latency(fit method) is measured to be ~2.5μs
  - For simple method, latency was adjusted to be ~2.5μs

Protocol (FAM↔TMM)

- SYNC = K27.7 = 0xFB
- RDY = K23.7 = 0xF7
- HEADER = K29.7 = 0xFD
- TMM SYNC = K27.7 + TMM => K0xFB, 0x54, 0x4D, 0x4D
- TMM RDY = K23.7 + TMM => K0xF7, 0x54, 0x4D, 0x4D
- FAM SYNC = K27.7 + FAM => K0xFB, 0x46, 0x41, 0x4D
- FAM data = K29.7 + counter(8 bit) + data(240 bit)

A)TMM side

1. send **SYNC** to FAM
2. wait receiver CDR locked
3. align FAM **SYNC**
4. send **RDY** to FAM
5. detect **HEADER** and align data
6. process data

B)FAM side

1. send **SYNC** to TMM
2. wait receiver CDR locked
3. align TMM **SYNC** or **RDY** (check only **TMM** character)
4. if **RDY** sensed, start sending data

C)Protocol between TMM and ETM are same as FAM and TMM.

Plan of system test after installation

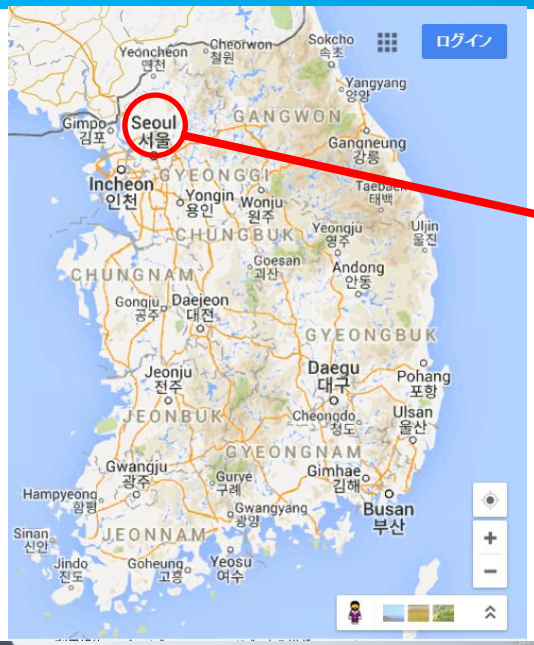
- Light yield check of all fiber using MultiFiberPro
- Cable connection check using
  - Test pulse from FAM
  - Test pulse from Collector
- FTSW installation for TMM
- Noise check
  - Noise of each TC
  - Coherent noise
- Temperature
- TC hit rate
- Pedestal level check and adjustment
- Xtal by Xtal energy calibration (fast shaper on ShaperDSP)
- Latency estimation of each TC
- Remote mcu firmware update check

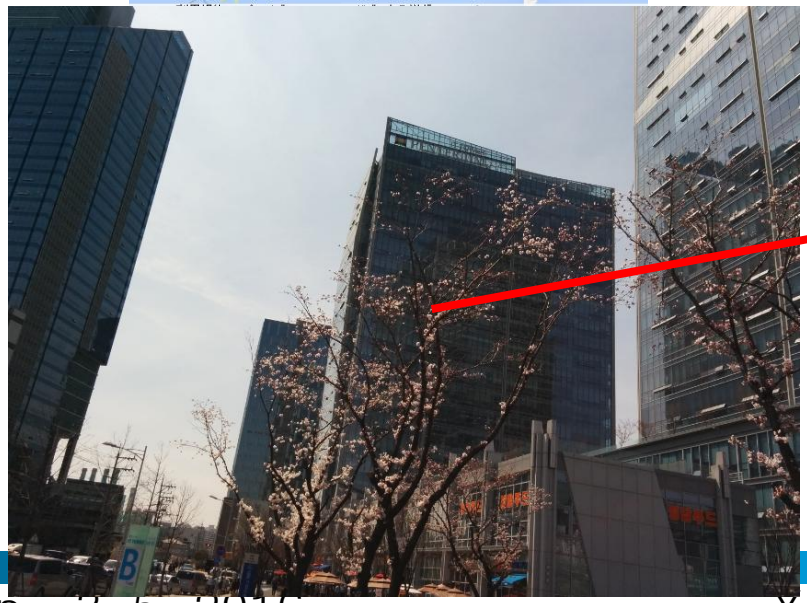
CRT status

- Took data on 8/22.
  - Trigger was based on only Barrel, but all Barrel TC.
  - Trigger rate is ~1 kHz
  - TC hit rate is ~60 Hz (TC energy threshold=30ADC~100MeV)
  - ~30min. run and ~2M event
  - Data side ~6Gbyte
  - No corrupted data was found !
  - But, data to b2link was dummy (intentionally this time)

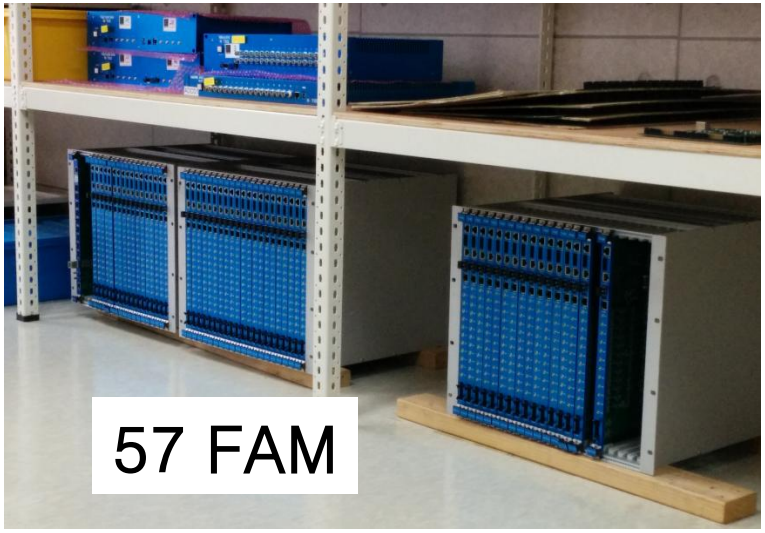
- ETM firmware modification is needed to take real cosmic data by b2link.
  - First, Sunghyun prepared firmware to send all TC data
    - Too many BRAM comsumption
  - Sunghyun is modifying firmware to send only fired TC data to b2link
  - Memory resource, timing constraint, compile time problem exist
    - those can be solved, but need more time.

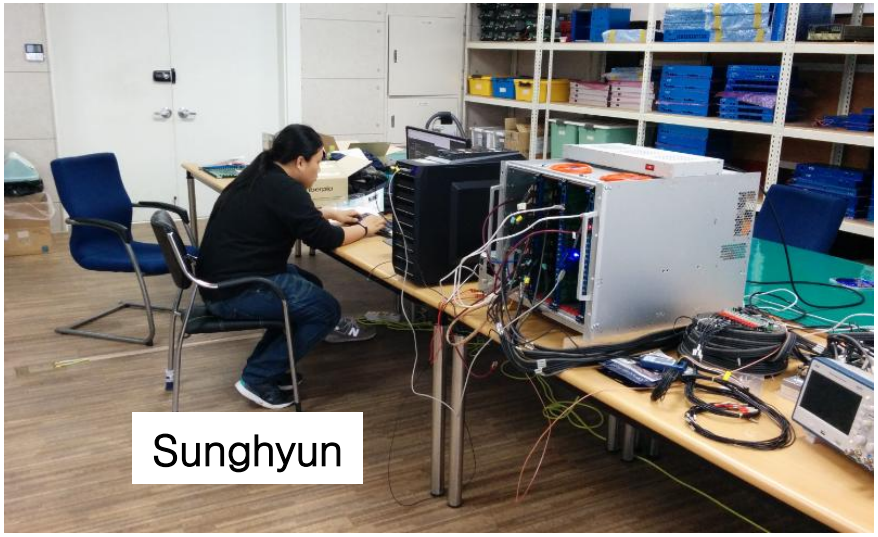
FAM and TMM test @ Notice

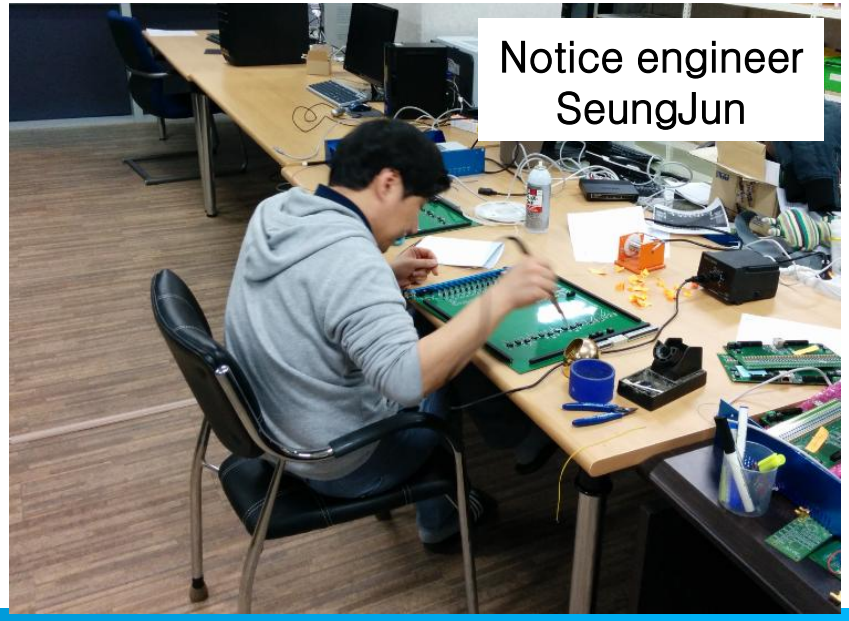




FAM and TMM test @ Notice







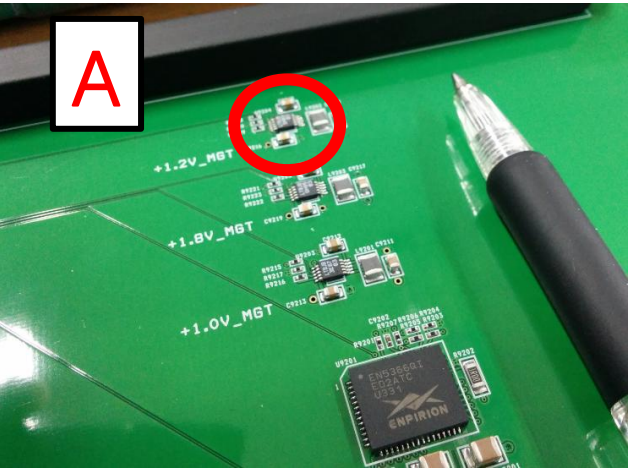
FAM(Check items)

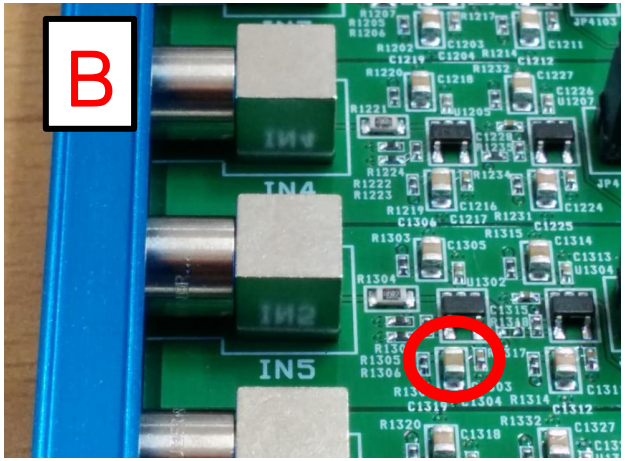
- Firmware downloading
  - MCU through 6 pin connector
  - CPLD though 10 pin connector
  - FPGA though 10 pin connector
- MGT and SFP check with ibert
- RJ45
  - TCP/IP communication
  - FTSW (all 4pins: ack, trg, rsv, clk)
- LEDs nearby RJ45 and SFP
- 2 temperature sensors
- Noise of FADC output w/ and w/o ShaperDSP
- TC E linearity and σ(E) using fitter
- TC analog sum output: linearity test

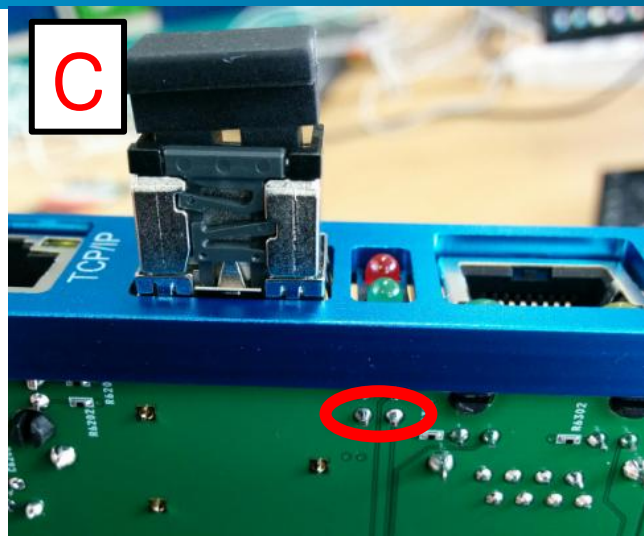
TMM(check items)

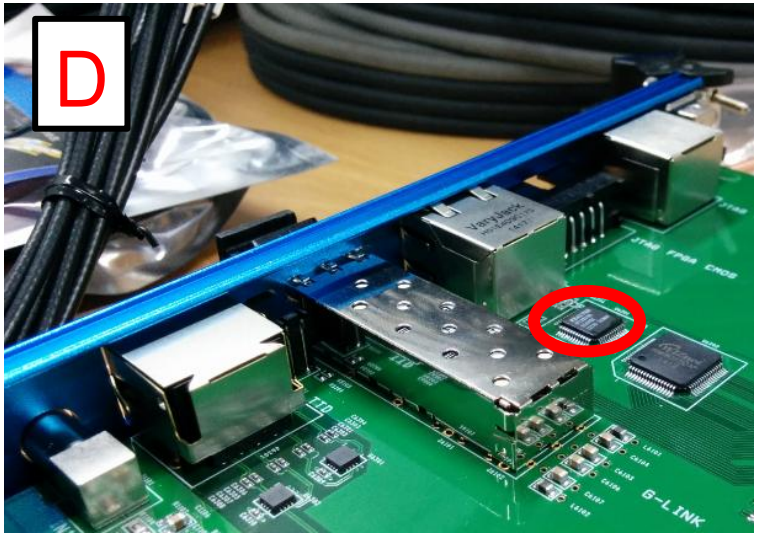
- Firmware downloading
  - MCU through 6 pin connector
  - CPLD though 10 pin connector
  - FPGA though 10 pin connector
- Optical transceiver check with ibert
- RJ45
  - TCP/IP communication
  - FTSW (all 4pins: ack, trg, rsv, clk)
- LEDs nearby RJ45 and SFP/QSFP
- 2 temperature sensors
- Lemo(127MHz) input

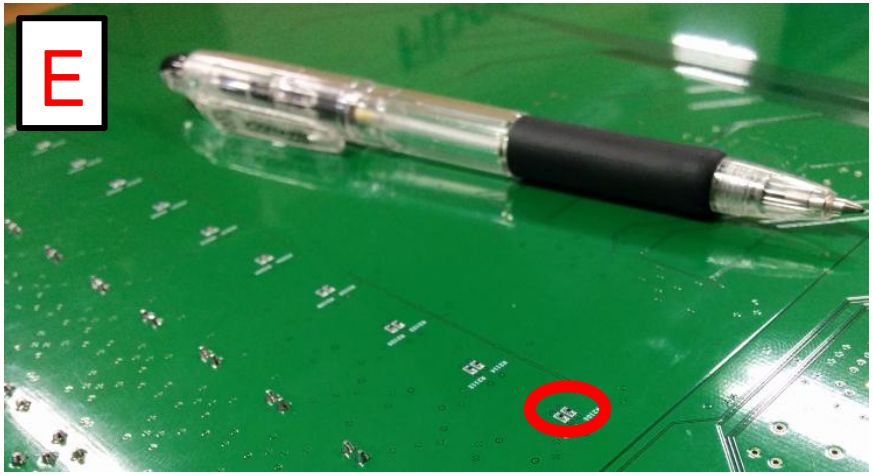
FAM hardware problems





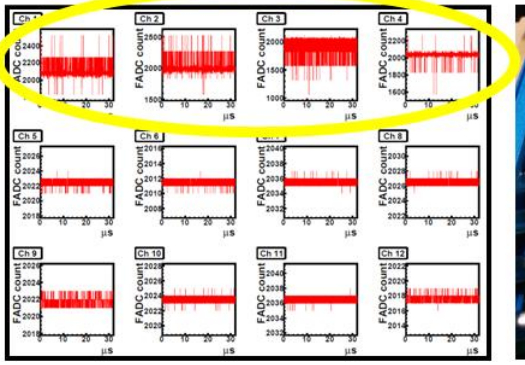


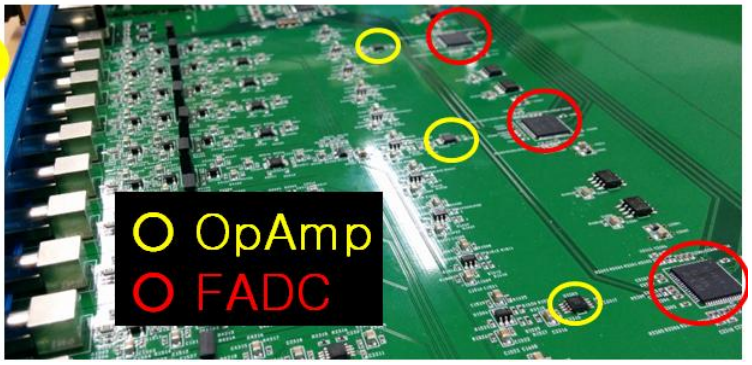




FAM problem/update after mass production

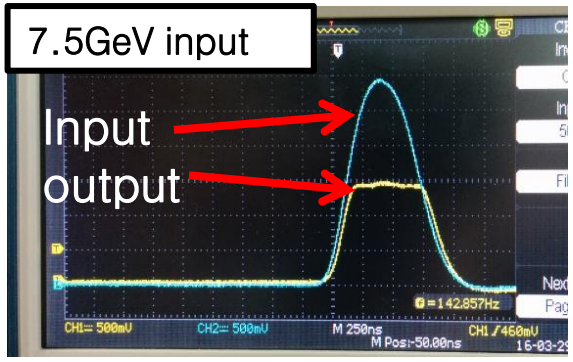
- FADC alignment problems were observed in 7 out of 60 FAMs

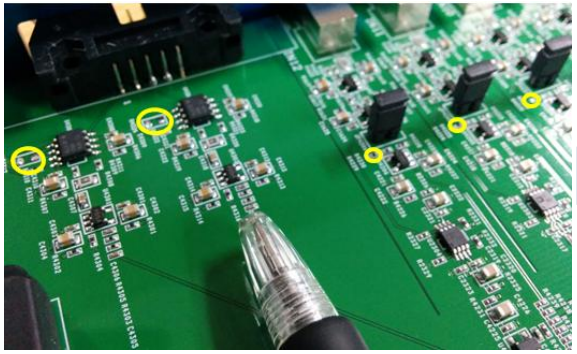


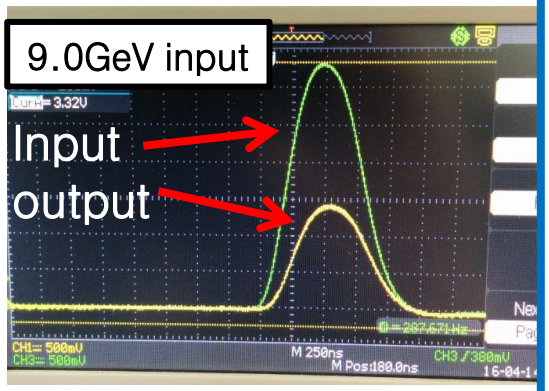


  - OpAmp were from not reliable supplier because N (OpAmp) < less than MOQ.
  - All OpAmp(3x60=180) are replaced to texas instruments products.

- Saturation of TC analog sum output



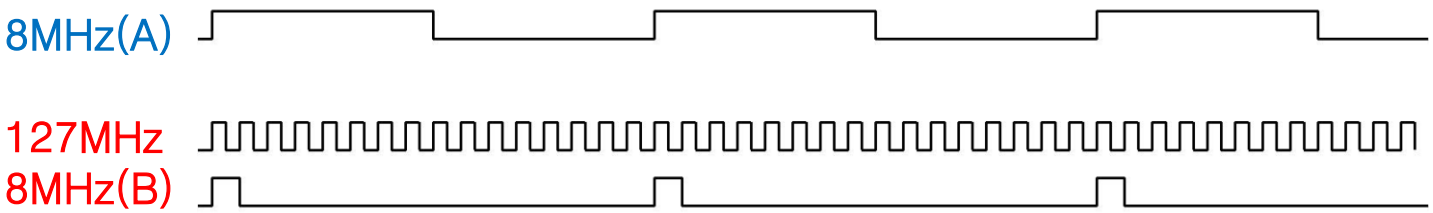




  - 2 registers(50Ω) and 12 registers(160Ω) / 1 FAM changed to 100Ω and 910Ω
  - Gain change from 1.0 to 0.46
  - Took 2 days to replace 14x57=798 registers for all FAMs by SangYeol and SeungJun

FAM problem/update after mass production

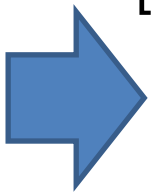
- Inconsistent fitter results btw FPGA and simulation in a few FAMs out of 60.
  - Problem was gone after changing clock treatment



- b2tt link instability
  - No link, repeat up and down, strange behaviors,…
  - All solved by
    - Clock generator parameter settings
    - Modify firmware of all of mcu, CPLD, and FPGA
  - b2tt link auto recovering logic are implemented in mcu
- Functionality of TCP/IP remote firmware update
  - mcu remote update is possible now (upgraded by SangYeol)

[old]

	FAM	TMM
MCU	X	X
CPLD	X	X
FPGA	O	O

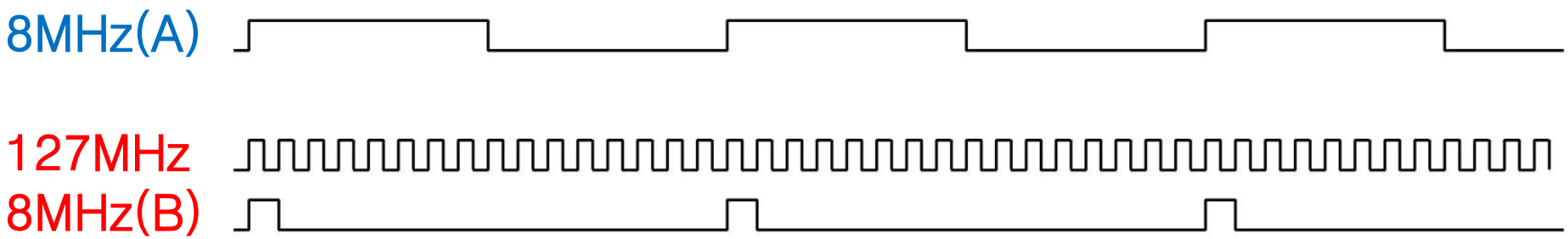


[new]

	FAM	TMM
MCU	O	O
CPLD	X	X
FPGA	O	O

FAM

- Fitter results between FPGA and simulator were inconsistent in a few FAMs.
- The problem was solved by following SangYeol's suggestion.



- (old) 8MHz(A) was used for 8MHz data timing
- (new) 8MHz(B) with 127MHz is used for 8MHz data timing

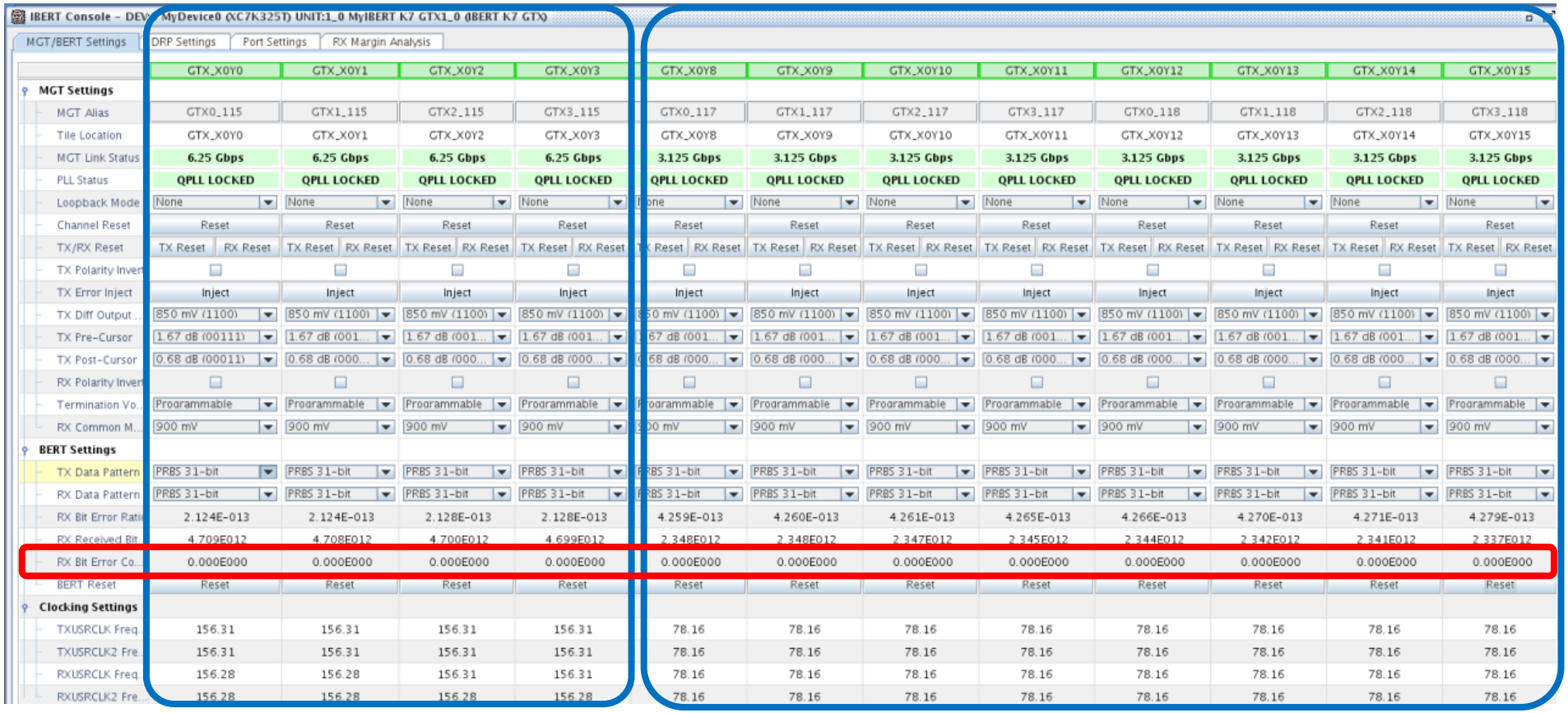
- Much less possibility to have signal timing shift due to each signal latency.

TMM(ibert)

~10min run for each TMM

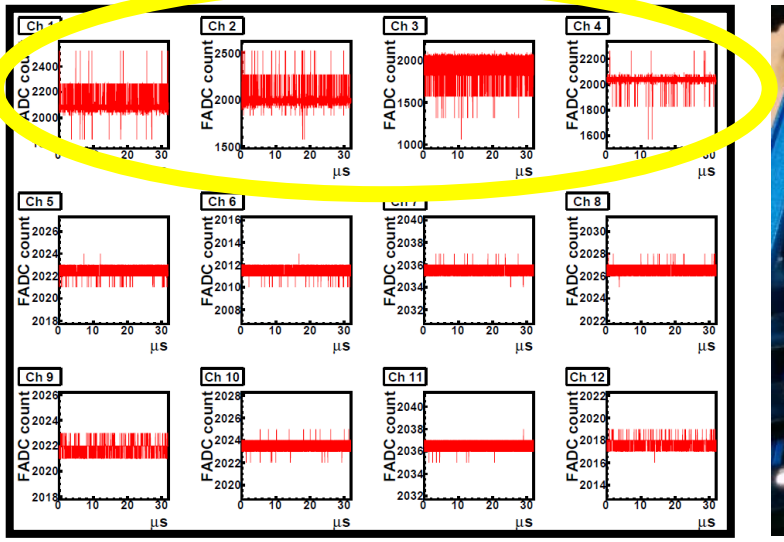
1QSFP(TMM↔ETM)

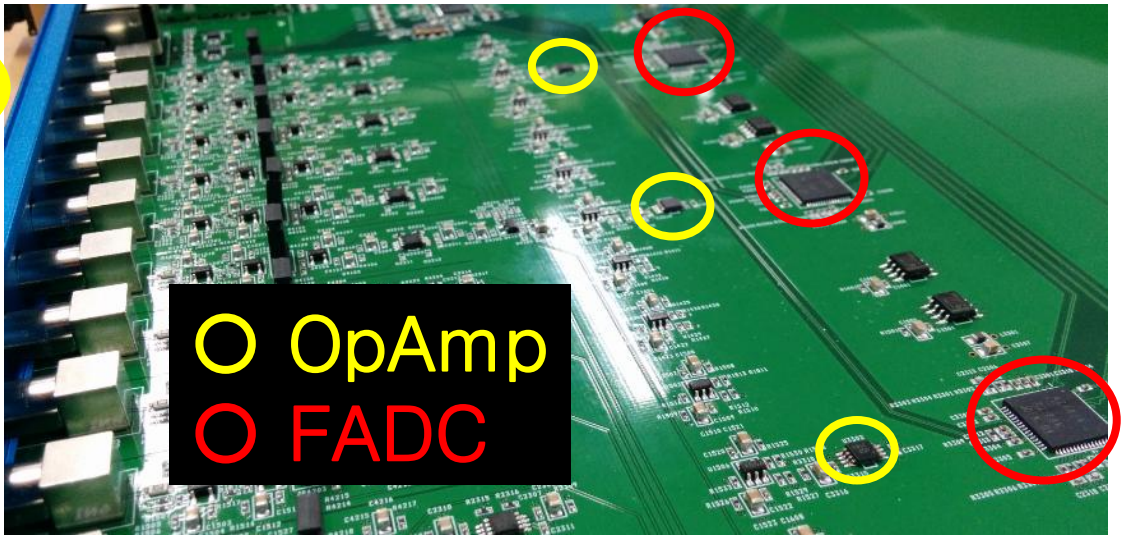
8 SFP(TMM↔FAM)



FADC alignment problem

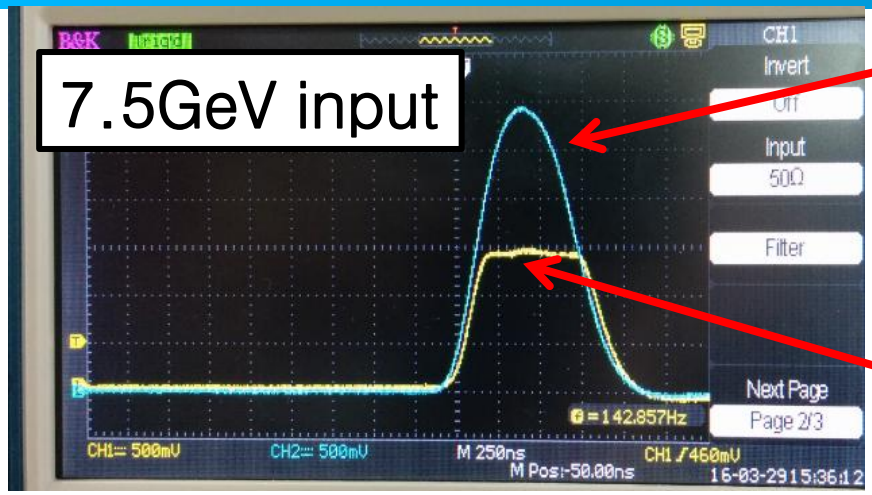
- FADC alignment problems were observed in 7 out of 60 FAMs





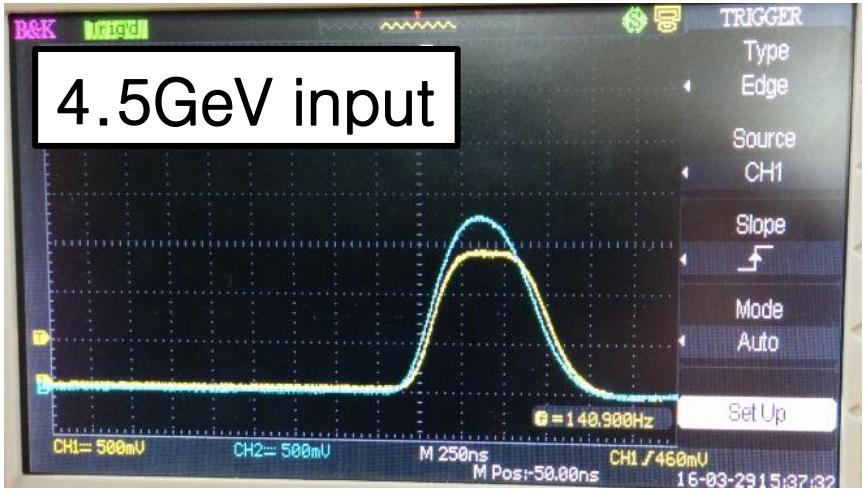
- OpAmp were from not very reliable supplier because # of OpAmp needed was less than MOQ.
- SangYeol got reliable ones(texas instruments)
- All OpAmp(3x60=180) are replaced to reliable ones.
- The problem was gone.

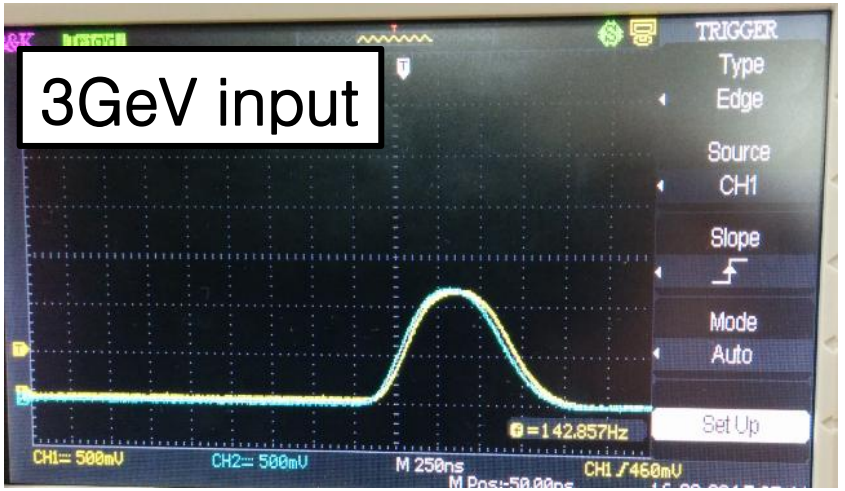
Saturation of TC analog sum output



Input

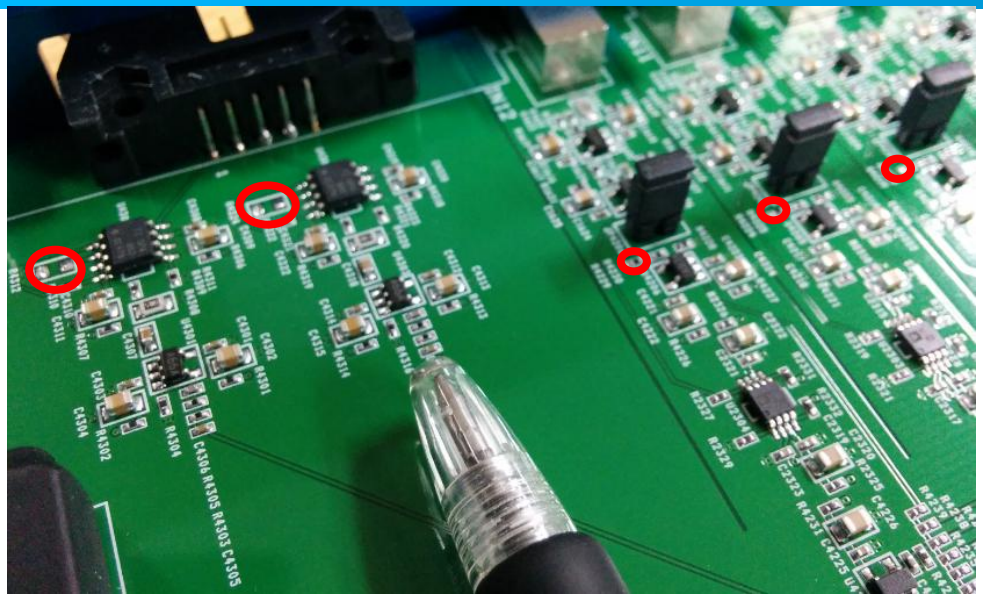
Output

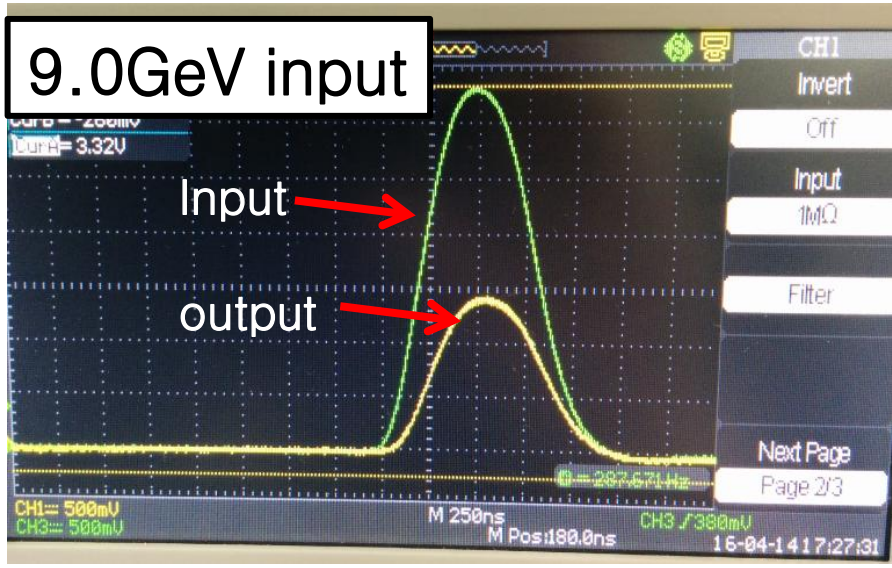




- In addition, register in V→I convertor for analog sum output on FAM was designed to be 50Ω by assuming 50Ω register on luminosity monitor, but it's 100Ω…

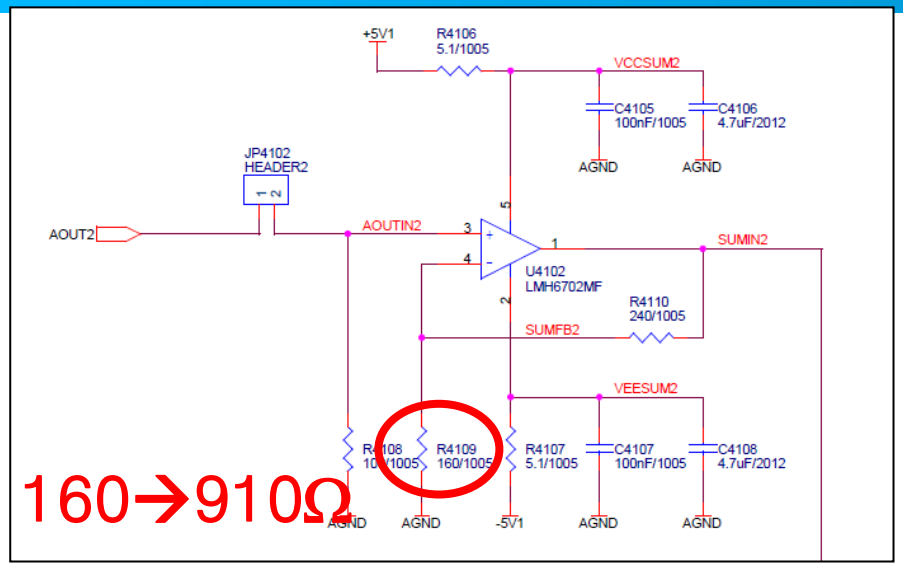
Saturation of TC analog sum output

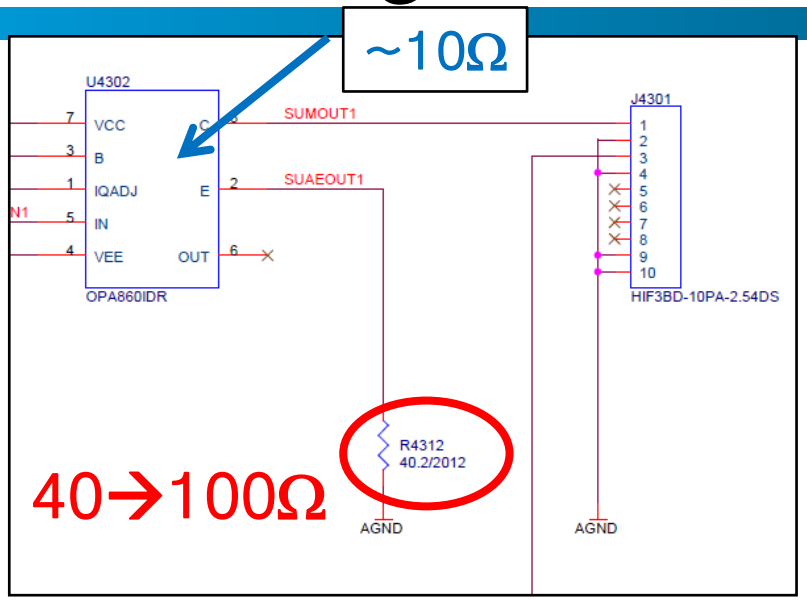




- 2 registers(50Ω) / 1 FAM were replaced to 100Ω
- 12 registers(160Ω) / 1 FAM were replaced to 910Ω
- Gain:
  - Original ~1.0
  - New ~ 0.46
- It took 2 days to replace 14x57=798 registers in total by SangYeol and SeungJun

Register replacement for analog sum





- Original gain =
  [10/(10+40)] x [(240+240)/240] x
  [(240+160)/160] x [50/(10+40)] = ~1.0
  (assuming 50Ω register at luminosity monitor)
- New gain =
  [10/(10+40)] x [(240+240)/240] x
  [(240+910)/910] x [100/(10+100)] =~0.46
  (assuming 100Ω register at luminosity monitor)

Clock chip(cdce62005) problem

- b2tt link was often not up for 3 FAMs.
  - Sometimes it is up after VME power recycle, but in most cases, it does not goes up state.
  - Problem appears when;
    - FTSW and FAM are on at same time
    - FTSW is on after FAM is on.
- Reason:
  - Parameters of PLL in clock chip was not optimized well.
  - Many parameters and combinations, not easy to optimize

- Solution:
  - Change the parameters back to default ones in data sheet (by assuming the default ones are optimized).
  - Change clock frequency of input clocks to PLL to use default parameter setting to PLL.