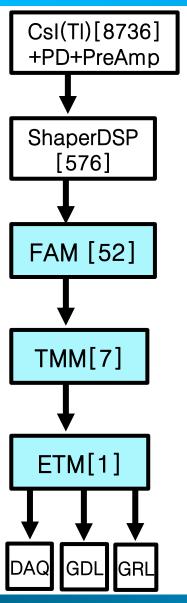
# ECL trigger status

Y.Unno Hanyang univ. 2016/09/3-5 TRG/DAQ Workshop

# Contents

- Introduction(ECL trigger)
- •FAM/TMM mass production/installation
- Optical link issues
- Control and monitoring system
- •ECL trigger server
- •Summary/Plan

# Belle2 ECL trigger system



●<u>FAM</u>

- Receive 576TC analog data from ShaprDSP
  - ●1TC consists of 4x4=16Xtals
- Digitization with FADC
- •TC E&T rec. by waveform analysis( $\chi^2$  fit) on kintex7

●<u>TMM</u>

Play an role of merger w/ kintex7

- ●<u>ETM</u>
  - Make a ECL trigger decision by all TC E&T on virtex6
  - •Send ECL trigger summary to GDL
  - •Send cluster data to GRL
  - Send fired TC E&T to HSLB
- 1<sup>st</sup> version of firmware for FAM/TMM/ETM are ready
  1<sup>st</sup> version of control & monitoring software are ready.

#### Y.Unno

# ECL trigger manpower







New students from Korea University (KU) Wonji Choi (KU) YoungJun Kim



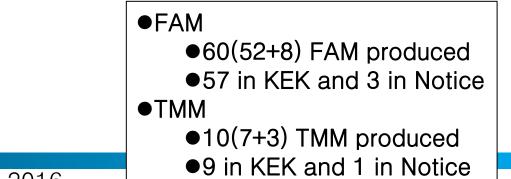
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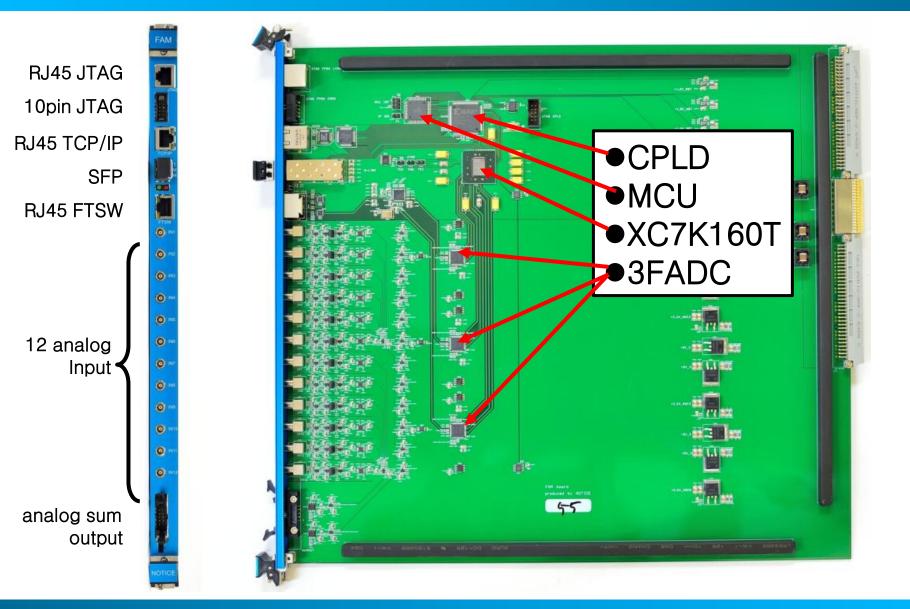
## FAM/TMM mass production/installation

- •(Feb/??) FAM mass production started.
- •(Mar/19) FAM mass production done.
- •(Mar/21) FAM test started @ Notice.
- •(Apr/08) TMM mass production started.
- •(Apr/25) TMM mass production done.
- •(Apr/25) TMM test started @ Notice.
- •(Apr/30) TMM test done @ Notice.
- •(May/11) FAM test done @ Notice.
- •(May/26) FAM/TMM cable labeling, cabling started.
- •(Jun/13) FAM and TMM delivered at KEK.

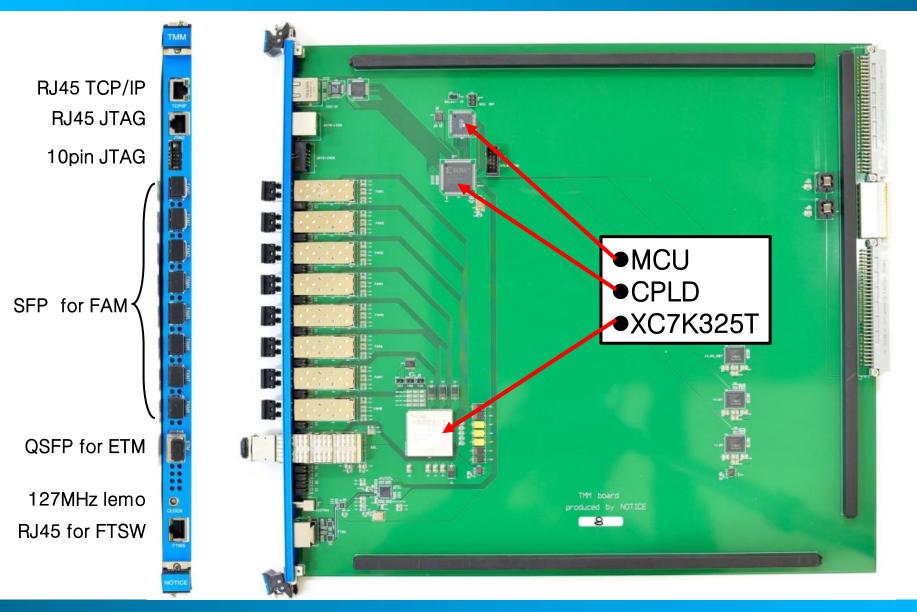
(Jun/15) FAM and TMM installation to E-hut/Belle2 done!



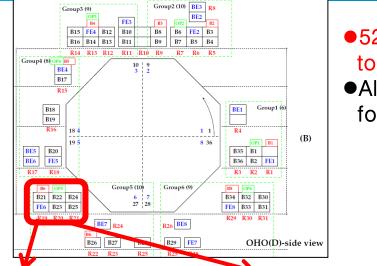
## FAM



## TMM



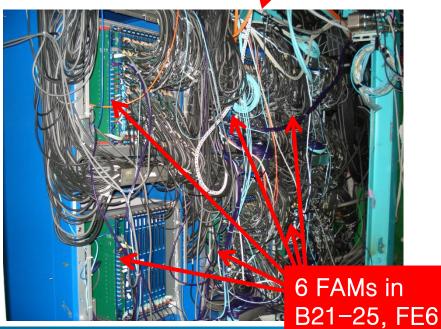
# FAM (@ detector)

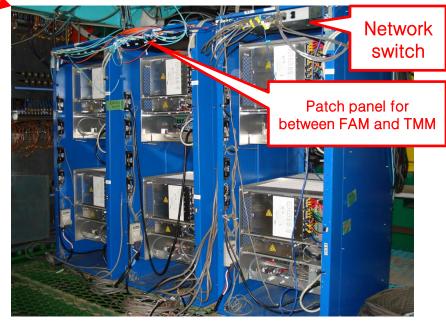


•52 FAMs have been installed to 52 VME crates around Belle2.

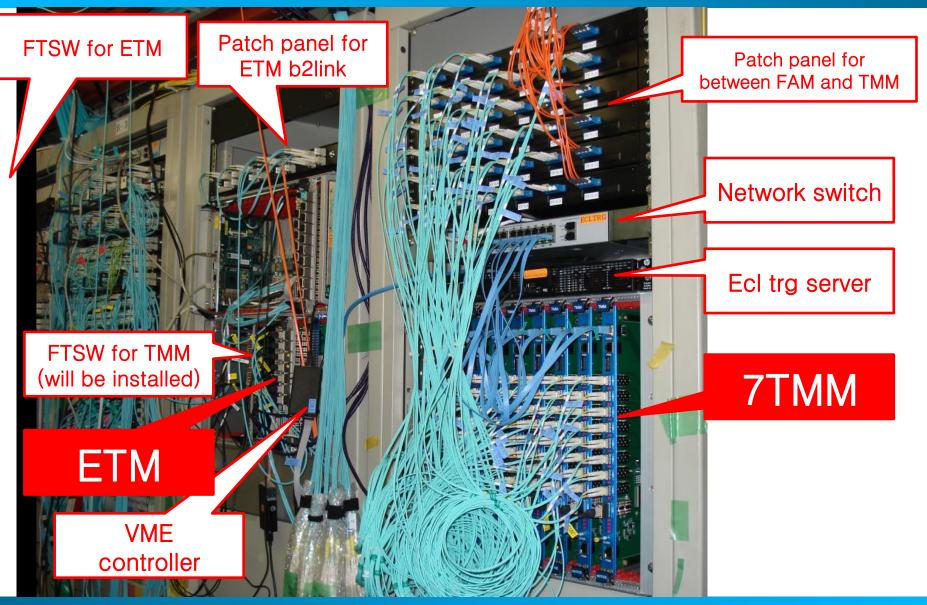
•All cables are connected except for luminosity monitor

- ●LC pair
- Cat7 for FTSW
- ●Cat5 for TCP/IP
- Lemo for ShaperDSP

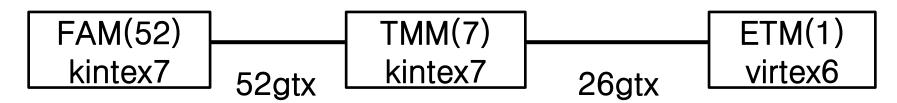




# TMM and ETM (@E-hut)



# **Optical link issues**



- (1)Data misalignment problem
  ●FAM→TMM
  ●TMM→ETM
- (2)Link up instability after reboot●TMM→ETM
- (3)Link instability after link up
  ●FAM→TMM
  ●TMM→ETM

# **Optical link**

	52dLC(52gtx) 2.5Gbps/gtx ecltrg protocol 576TC E&T		7MPO(26gtx) 5.0Gbps/gtx ecltrg protocol 576TC E&T		1MPO(4gth) ~35Gbps/4gth YunTsung protoco Cluster data	GRL(1) Virtex6 gthe1
FAM(52) Kintex7 gtxe2		TMM(7) Kintex7 gtxe2		ETM(1) Virtex6 gtxe1 gthe1	1MPO(1gtx) ???Mbps/gtx YunTsung protoco Ecl trg summary	GDL(1) Virtex6 gtxe1
					1MPO/1dLC(1gtx) ??? Mbps/gtx belle2link Fired TC E& T data	HSLB(1) Virtex5 gtp

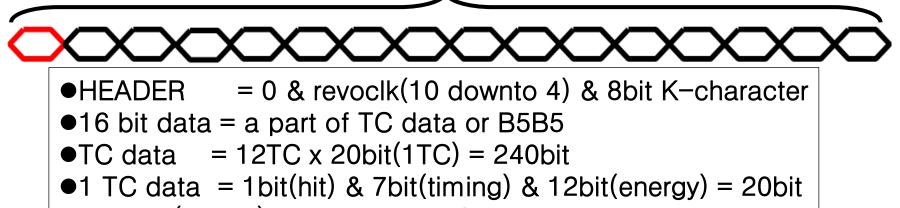
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# Optical link(data format)

## ●FAM↔TMM (1gtx)

•16 bit HEADER & 12 x 20 bit TC data = 256 bit

• by 16 clock with 127MHz (= 1 clock with 8MHz)



•7bit(timing) is from fitter, LSB=1ns.

#### ●TMM↔ETM (1gtx)

●Data format is (almost) same as FAM↔TMM

- •2 FAM data by 1 gtx are sent simultaneously.
- •# of bit with 1 clock is 512 bit.

o~ r.	trm01	B5B5	8585	B5 B5	) ( 2B	BF7 X B585		2CF7	B5B5
o~ rd	t_tm02	B5B5	8585	B5B5	) 2B	BF7 X B585		2CF7	8585
∽rd	t_tnm03	8585	8585	B5B5	) ( 2B	8F7 8585		2CF7	8585
o~ rd	t_tnm04	B5B5	8585	B5B5	) 2E	8F7 ( B5B5		2CF7	B5B5
o~ rd	t_tnm05	B5B5	8585	B5 B5	) 2E	8F7 8585		2CF7	8585
o~ rd	t_tnm06	<b>B5B5</b>	8585	B5B5	) ( 2B	BF7 B5B5		2CF7	B585
o~ rd	t_tnm07	B5B5	8585	B5 B5	) 2B	8F7 8585		2CF7	8585
o~ rd	t_tnm08	B5B5	8585	B5B5	28	BF7 X B585		2CF7	8585
∽rd	t_tnm09	3BF7	3BF7	B5 (2B	F7)	B5B5	X 2CF7		B5B5
	t tool0	DEDE	0505	05.05	X 28	8F7 8585		2CF7	8585
20	S atv	0	hc	nnolo	$\sim$	B5B5	(2CF7)		B585
20	y yıx	C		annels	X	B5 B5	(2CF7)		B5B5
o~ rd	t_tnm13	B5B5	8585	B5 B5	28	8F7 X 8585	X	2CF7	8585
o~ rd	t_tnm14	B5B5	8585	B5B5	) 2E	8F7 ( B5B5	X	2CF7	B585
o~ rd	t_tnm15	B5B5	8585	B5B5	) ( 2B	8F7 8585	X	2CF7	8585
o~ rd	t_tnm16	B5B5	8585	B5B5	) ( 2B	8F7 8585	X	2CF7	8585
o~ rd	t_tnm17	3BF7	3BF7	B5 (2B	F7)	B5 B5	(2CF7)		B5B5
o~ rd	t_tnm18	3BF7	3BF7	85 X 28	F7)(	8585	(2CF7)		8585
o~ rd	t_tnm19	3BF7	3BF7	B5 (2B	F7)	B5 B5	(2CF7)		8585
o~ rd	t_tnm20	3BF7	3BF7	B5 (2B	F7) (	B5 B5	(2CF7)		8585
o~ rd	t_tnm21	3BF7	3BF7	85 X 28	F7) (	8585	(2CF7)		8585
o~ rd	t_tnm22	3BF7	3BF7	B5 (2B	F7)(	B5 B5	(2CF7)		B5B5
o~ rd	t_tnm23	3BF7	3BF7	B5 X 2B	F7 )	8585	(2CF7)		8585
	t_tnm24	38F7	3BF7	B5 (2B	F7)(	B5B5	(2CF7)		B585
o~ r	_tnm25	3BF7	3BF7	B5 (2B	F7 )	B5 B5	( 2CF7)		B5B5
o~ rda	it_tnm26	8585	8585	8585	<u>) ( 28</u>	8F7 ( 8585		2CF7	8585

∽ rat_trm01	8585 8585 B5E	B5 (	(2BF7) B5B5		(2CF7	B585
∽rd t_tnm02	8585 8585 <u>858</u>	B5 X	(2BF7) B5B5		2CF7	8585
⊶rd t_tnm03	8585 8585 <u>858</u>	B5 X	(28F7) 8585		2CF7	8585
∽rd t_tnm04	8585 8585 <u>858</u>	B5 (	(2BF7) B5B5		2CF7	B585
⊶rd t_tmm05	8585 8585 <u>858</u>	B5 X	(2BF7) 8585		2CF7	8585
⊶rd t_tnm06	8585 8585 <u>858</u>	<u>85 (</u>	(2BF7) B5B5		2CF7	B585
⊶rd t_tmm07	B5B5 B5B5 B5B	B5 (	(2BF7) B5B5		2CF7	8585
⊶rd t_tnm08	8585 8585 B58	B5 (	(28F7) 8585		2CF7	8585
⊶rdt_tnm09	38F7 38F7 85	( 2BF7 )	(	2.067		B5B5
and themato	0505 0505 050	~~X	(2BF7) 8585		(2CF7	8585
26 at	x chan	nolo 🕅	B585	2CF7		8585
	x Ullal		B5B5	2CF7		8585
°rd t_tnm13	B5B5 B5B5 B5B	85 X	(28F7) 8585		2CF7	8585
∽rdt_tnm14	8585 8585 <u>858</u>	B5 X	(2BF7) B5B5		2CF7	B585
⊶rd t_tnm15	8585 8585 <u>858</u>	B5 (	(2BF7) 8585		2CF7	8585
⊶rd t_tnm16	8585 8585 <u>858</u>	B5 X	(2BF7) 8585		2CF7	8585
⊶rd t_tnm17	38F7 38F7 85	( 28F7 )	B5B5	2CF7		B5B5
⊶rd t_tnm18	38F7 38F7 85	X 28F7 X	8585	2CF7		8585
∽rdt_tnm19	38F7 38F7 85	( 28F7 )	B585	2CF7		B5B5
⊶rd t_tnm20	38F7 38F7 85	( 28F7 )	B5 B5	2CF7		8585
∽rd t_tnm21	38F7 38F7 85	( 28F7 (	8585	2CF7		8585
∽rd t_tnm22	38F7 38F7 85	( 28F7 )	B5B5	2CF7		B5B5
⊶rd t_tnn23	38F7 38F7 85	( 28F7 (	8585	2CF7		8585
⊶rd t_tnm24	38F7 38F7 85	( 28F7 )	B585	2CF7		8585
⊶rti_tmm25	38F7 38F7 85	( 2BF7 )	B5B5	2CF7		B5 B5
∽rdat_tnm26	8585 8585 <u>858</u>	B5 X	(2BF7) 8585		2CF7	8585

#### •Alignment logic

- •Check all gtx data are B5B5 for a few clocks
- •Check each header delay from earliest header
- •Align each channel based on measured delay with 16bit Serial Register LUT.
- •Alignment logic is active only for link up channel.
- •Additional latency due to alignment is 8 to ~100 ns.
- •Alignment results can be monitored by ecl trigger server.

∘- reat_tm	1 <b>01a</b> B5	85 B5B5	8585	( 28F7 )	8585	(2CF7)	B5B5
⊶ ndat_tm	1 <b>02a</b> 85	85 B5B5	8585	( 28F7 )	8585	(2CF7)	8585
⊶ rdi t_tm	1 <b>03a</b> 85	85 8585	8585	( 28F7 )	8585	(2CF7)	8585
∘- rdat_tm	104a B5	85 B5B5	8585	( 28F7 )	8585	(2CF7)	B5 B5
•-rdat_tm	1 <b>05a</b> B5	85 B5B5	8585	(28F7)	B585	(2CF7)	8585
⊶ ndi t_tm	1 <b>06a</b> B5	85 B5B5	8585	( 28F7 )	8585	(2CF7)	8585
⊶ ndat_tm	1 <b>07a</b> 85	85 8585	8585	28F7)	8585	(2CF7)	8585
⊶ ndat_tm	108a B5	5 B5B5	8585	(28F7)	8585	(2CF7)	8585
⊶ ndi t_tm	1 <b>09a</b> 85	35 B5B5	8585	( 28F7 )	8585	C2CF7	8585
				( 28F7 )	8585	(2CF7)	8585
26 /	aty (	ha	innels 📄	(28F7)	8585	(2CF7)	8585
	gin (	ла		( 2BF7 )	8585	(2CF7)	8585
•- rdi t_tm	n <b>13a</b> B5	85 B5B5	8585	(28F7)	8585	(2CF7)	8585
⊶ ndat_tm	n14a 85	85 8585	8585	(28F7)	8585	(2CF7)	8585
⊶ ndat_tm	n <b>15a</b> 85	85 8585	8585	28F7)	8585	2CF7	8585
⊶ ndat_tm	n <b>16a</b> B5	85 8585	8585	( 2BF7 )	8585	(2CF7)	8585
⊶ ndi t_tm	n <b>17a</b> 85	85 B5B5	8585	( 2BF7 )	8585	(2CF7)	8585
⊶ ndat_tm	1 <b>8a</b> 85	5 B5B5	8585	( 28F7 )	8585	(2CF7)	8585
⊶ rdat_tm	n <b>19a</b> 85	5 8585	8585	(28F7)	8585	2CF7	8585
⊶ ndat_tm	1 <b>20a</b> B5	85 8585	8585	(2BF7)	8585	2CF7	8585
⊶ ndi t_tm	n <b>21a</b> B5	85 B5B5	8585	( 2BF7 )	8585	(2CF7)	8585
⊶ ndat_tm	122a 85	5 B5B5	8585	(28F7)	8585	(2CF7)	8585
⊶ rdat_tm	123a 85	85 8585	8585	( 28F7 )	8585	(2CF7)	8585
⊶ rdit_tm	1 <b>24a</b> B5	85 8585	8585	( 2BF7 )	8585	(2CF7)	B5B5
•-ratm	125a 85	85 B5B5	8585	( 2BF7 )	8585	(2CF7)	8585
∽ rdat_tm	1 <b>26a</b> 85	5 B5B5	8585	X 28F7 X	8585	(2CF7)	8585

Same logic was implemented in FAM→TMM too.
Alignment logic is working (almost) perfectly.
In some special case, this logic does NOT work.
TMM reboot after ETM is up

~	t_tmm01	8585	B5B5		B5B5	( 3AF7 )	E	35 B5	X 38F7 X	B5B5
o~ n	at_tmm02	8585	B5B5		B585	( 3AE7 )		8585	( 3BF7 )	B5 B
∽ra	at_tmm03	8585	8585	B	585	( 3AF7 )	B5 B5		(3BF7)	8585
∽ n	at_tmm04	8585	B5B5		8585	( 3AF7 )	E	3585	( 3BF7 (	8585
∽ra	at_tmm05	8585	8585	39F7 (		8585	( BAF7		8585	X
∽ na	at_tmm06	8585	8585		8585	( 3AF7 )		8585	( 3BF7 )	B5 B
∽ra	at_tmm07	8585	B5B5		B5B5	( 3AF7 )		B5B5	( 3BF7 )	B5 B
o~ n	at_tmm08	8585	B5B5		B5B5	( 3AF7		8585	X 38F7 X	
∽ra	at_tmm09	8585	B5B5	B	585	( 3AF7 )	B5 B5		(3BF7)	8585
~ P 2	t ten10	0505	DEDE		B5 B5		( 3AF7	8585		(3BF7)
26	tto (		ha	nnels		585	( 3AF7 )	B5	B5	( 3BF7 )
20	y yıx	C	la	1111013	( 39F7 )		8585	( 3AF7 )	8585	
	at_tmm13	-	BSB5	•	B585	( 3AF7 )		8585	(3BF7)	B5 B
∽ra	at_tmm14	8585	B5B5		B5B5	( 3AF7 )		8585	( 3BF7 )	B5 B
∽ra	t_tmm15	8585	8585		8585	( 3AF7 )		8585	(38F7)	B5 B
	at_tmm16		BSBS	BS	585	( 3AF7 )	B5 B5		(3BF7)	B5B5
	at_tmm17		B5B5		8585	(3AF7)		35.85	( 3BF7 )	8585
	at_tmm18		B5B5		8585		( BAF7 )	8585		X 38F7 X
_	at_tmm19	-	B5B5	8585	X 39F7 X		B5B5	( 3AF7	B5	B5
	at_tmm20		B5B5	<u> 39F7 X</u>		8585	( 3AF7.)		B5B5	
	at_tmm21		B5B5		8585	( 3AF7		8585	X 38F7 X	
	at_tmm22		B5B5	B5B5	( 39F7 )		B5B5	( 3AF7 )	B5B5	
	at_tmm23	-	B5B5		B5B5	( 3AF7		8585	(3BF7 )	
	at_tmm24		B5B5		8585	( 3AF7 )	E	9585	X 38F7 X	8585
200	trm25	-	BSBS		B5B5	( 3AF7 )		8585	X 3BF7 X	B5 B
e- rua	at_tmm26	8585	B5B5		B5B5	( 3AF7 )		B5B5	( 3BF7 )	B5 B

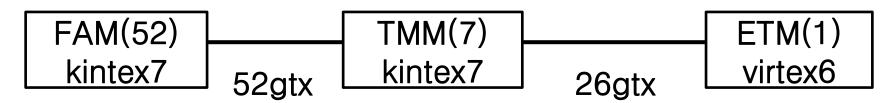
When TMM reboot after ETM up, data shifts are too bad...
Solution: Send gtxrxreset to all 26 gtx on ETM by hand.
Plan: better to implement an automatic recovery logic.

## (2)Link up instability of TMM $\rightarrow$ ETM after reboot



•Many links didn't go to up state after reboot or power-up There was a bug to do gtxtxreset & gtxrxreset Some of links were still down. Prepare pllrxreset signal •All 26 gtx links were up. •But, pllrxreset always has to be sent after rebooting. Sunghyun and SangYeol found source of this problem. •minimum unit of TMM $\rightarrow$ ETM is 40bit(32x10b/8b) Kintex7 maximum bitslip = 40 •Virtex6 maximum bitslip = 20•This problem was gone by implementing a patch to ETM Additional latency is 1clock(=8ns).

# (3)Link instability after link up



•Some links were down(and automatically recovered)

- ●8/20-21(48hour monitoring)
  - •FAM-TMM: FAM52 2down
  - •TMM-ETM: ch22 17down, ch23-26 1down
- •8/23 (12hour monitoring)
  - •FAM-TMM: FAM25 1down, FAM34 3down (b2tt down)
  - •TMM-ETM: ch13-16 2down, ch17-20 4down, ch21 2down
- •Removing and inserting QSFP mitigates the problem…
  - Planning to replace QSFP
- Preparing monitoring firmware logic to check in details
  - •How long time link is down:  $\sim 50 \mu s$
  - •Which signal in link up/down definition have a problem

# FAM b2tt down problem

•FAM b2tt down happened

•Before KEK shutdown: FAM 45

Fixed by disconnecting&connecting LAN cable(FTSW)8/18: FAM 20

Fixed by disconnecting&connecting LAN cable(FTSW)
8/20-25

●FAM 25, 34

Fixed by disconnecting&connecting LAN cable(FTSW)
 9/1~

•FAM 35

•Detail investigation is needed, but it might take time to fix…

## Link status on $ETM \rightarrow GDL$ and GRL

●YunTsung prepared designs of ETM→GDL and GRL links.
●Testing w/ single UT3 w/o actual ETM firmware by chipscope.

#### Latency check

	v1	v2
ETM→GDL	~1.1µs	0.47µs
ETM→GRL	~0.9µs	0.31µs

#### ●Data misalignment in ETM→GRL(4gth)

⊶ in_10	A035	A035	A04D	A04E	A04F	(A050)	(A051)	A052	A053
∾ in_11	A035	A035	A04D	A04E	A04F	(A050)	(A051)	A052	A053
∾ in_12	A039	A039	A051	A052	(A053)	(A054)	(A055)	(A056)	(A057
⊶ in_13	A035	A035	A04D	A04E	( A04F )	(A050)	(A051)	A052	A053
					400	ns shift			

Plan to do more check.
Logic(ETM→GDL) will be implemented to ETM as top priority after TRG/DAQ workshop.

Sep., 3-5, 2016

1 MPO, 1GTX

ETM↔GDL

ETM↔GRL

1 MPO, 4 GTH

#### Y.Unno

# Control & Monitoring system

## FAM

Sep., 3-5, 2016

0 : Quit 1 : Status 2 : Reset general monitor param 3 : R temparature	0 : Quit 1 : status 2 : general monitor reset 3 : fam data align status 10 : link down check(temporal) 20 : reboot										
4 : R pedestal 5 : R TC E threshold 6 : R TC hit rate	Select ac										
7 : R TC hit rate(maximum)	firmware	versi	ion : TMM(	27), b2tt(	(46)						
10 : R TC E/T rec. type 11 : W TC E/T rec. type	 TMM #		1	2		4	5	6	7		
12 : Set basic parameters	clock	:	1	1	1	1	1	1	1		
13 : Set LUT for fitter	clk NDwn b2tt		0	0 1	0 1	0 1	0	0	0		
20 : Reboot	b2tt NDwn		0	1	1	1	1	1	0		
21 : (X not ready)Firmware download	fam link		11111111)	(111111111)	(11111111)	(11111111)	(11111111)	(11110000)	(11111111)		
	fam NDwn		OK	OK	OK	OK	OK	OK	OK		
	etm link etm NDwn			(1111)			(1111) (0 0 0 0)	(1100) (0 0 0 1)	(1111) (0 0 0 0)		
	temp.		(28, 26)	(28, 26)			(28, 26)	(28, 26)	(28, 25)		
Select action?											
1	TCHitRate	(Hz)									
<pre>firmware version : FAM(63), b2tt(46) clock : OK</pre>	(ch #):	1	2	3 4	56	7 8	(tot)				
NClkDwn : OK	TMM 1 :	0	0	0 0	0 0	0 0	( 0)				
b2tt : OK	TMM 2 :	59		56 47	47 49	60 55					
Nb2ttDwn : OK	TMM 3 : TMM 4 :	65 54		56 40 55 48	56 49 54 52	68 60 55 66					
gtxlink : OK	TMM 5 :	54 60		55 46 59 67	54 52 51 50		( 447)				
	TMM 6 :	51	45	46 46	0 0	0 0	( 188)				
NgtxlinkDwn : OK	TMM 7 :	0	0	0 0	0 0	0 0	( 0)				

TMM

All 52FAM, 7TMM, ETM, 576TC can be controlled & monitored.
Keep updating control & monitoring system.

Y.Unno

## Monitoring system(TC hit rate/FAM)

•Total TC hit rate of each FAM.

•TC energy threshold =  $30 \text{ ADC} \sim 100 \text{MeV}$ .

#### Typical hit rate (8/22)

FAMHitRate(Hz) :

(ch #) :	1	2	3	4	5	6	7	8
TMM # 1:	0	0	0	0	0	0	0	0
TMM # 2:	59	66	66	69	73	55	65	48
TMM # 3:	68	54	61	60	66	59	57	57
TMM # 4:	66	60	58	62	52	56	70	60
TMM # 5:	60	65	50	55	68	83	56	44
TMM # 6:	42	46	46	57				J
TMM # 7:	0	0	0	0	0	0	0	0

#### Maximum hit rate in 8/20-21(48h)

FAM	Ma)	(Hi t	tRate (Hz)	:						
(ch	#)	:	1	2	3	4	5	6	7	8
TMM	#	1:	0	0	0	0	0	0	0	0
TMM	#	2:	85	89	92	976	116	88	5451	2806
TMM	#	3:	597	89	5036	172	94	88	85	84
TMM	#	4:	85	88	3871	82	224	83	83	88
TMM	#	5:	101	87	88	88	89	87	89	88
TMM	#	6:	84	87	88	413				
TMM	#	7:	0	0	0	0	0	0	0	0

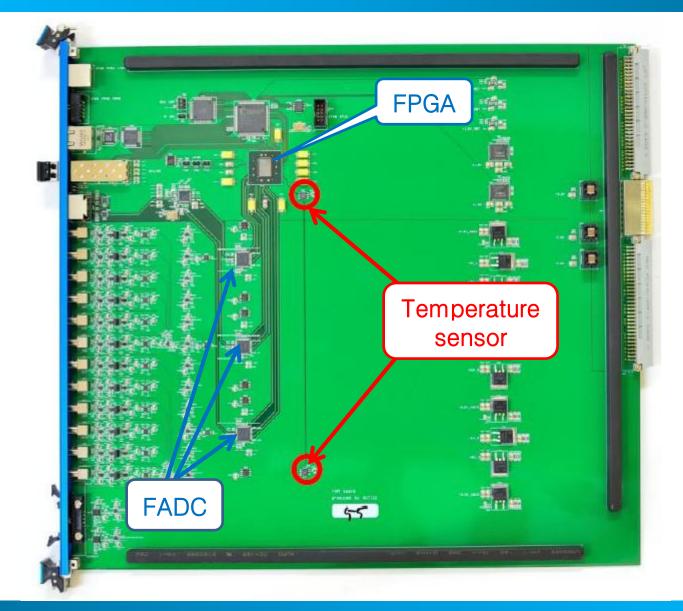
•Hit rates are very high for some FAM sometimes

•TC by TC hit rates were no monitored in this check.

Probably there were high noise sometimes(guess)

•Wonji and YungJun supervised by InSoo are preparing a program which monitors all TC noise as a function of time.

## 2 temperature sensor on FAM

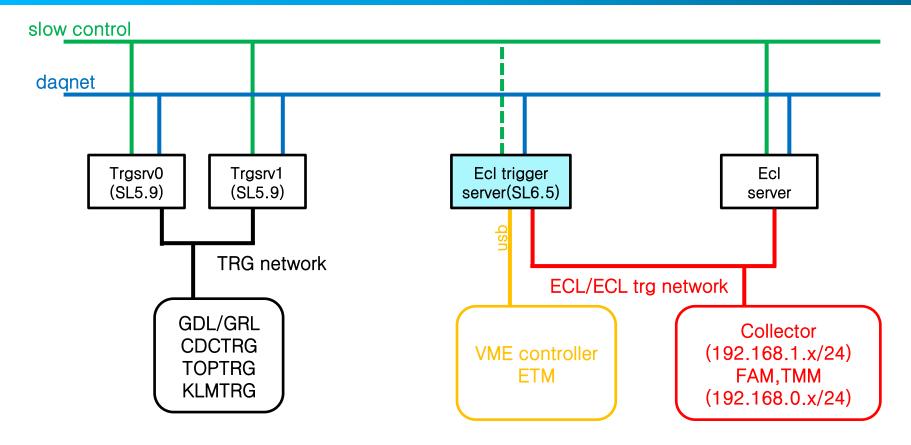


## Monitoring system(temperature on FAM)

	1	2	3	4	5	6	7	8
TMM #2 :(34, TMM #3 :(28, TMM #4 :(32,	32) 25) 29)	(32, 28) (30, 28) (32, 31)	(30, 27) (28, 26) (32, 30)	(29, 26) (30, 28) (32, 30)	(28, 26) (29, 26) (33, 29)	(29, 26) (30, 26) (33, 30)	(40, 32) (34 (28, 25) (29 (32, 27) (28 (30, 28) (31 (31, 28) (34	. 26) . 26) . 29)
TMM #6 :(31,	28) 32) 	(32, 30) (30, 27)	(36, 31) (28, 25)	(32, 30) (31, 30)	(41, 34)		(38, 32) (40	

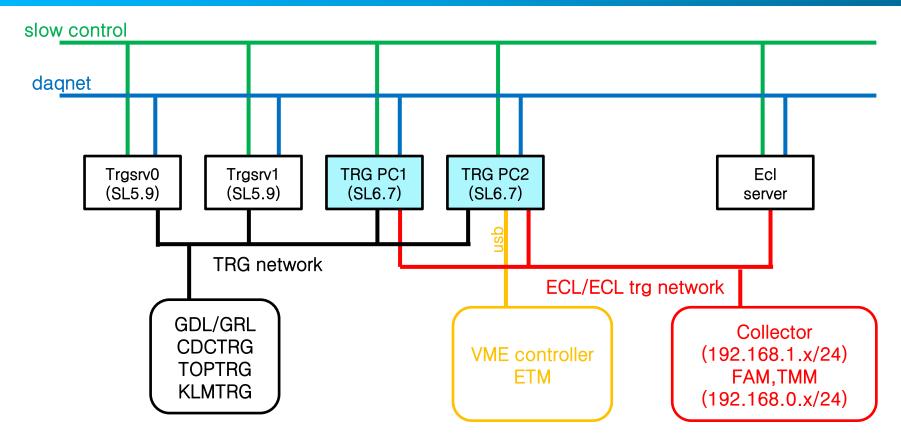
Temperatures are in rage of 30-40°C
The reason why 10°C difference appears is unknown…
Performance variation of VME fan ?
Acceptable temperature of FPGA and FADC ~80°C
(some distance between sensor and FPGA/FADC)
Wonji and YungJun with InSoo are preparing a program to monitor temperature as a function of time.
Plan to measure FPGA temp. of FAM/TMM/ETM directly.

# ecl trigger server/network(now)



Y.Unno

# ecl trigger server/network(new)



•Purpose of new TRG servers(TRG PC1 and PC2):

- •One of them is backup for another.
- •GUI server for GDL, GRL and all sub-trigger
- •ECL trigger sever

•Everything on current ecl trigger server will be moved to TRG PC1 and PC2.

# Summary

●Summary

- •All ECL trigger modules(FAM,TMM,ETM) installed.
- •Critical problems in optical links were fixed.
- ●Working on ETM→GDL/GRL link, and full ecl trigger chain (FAM→TMM→ETM→GDL/GRL) will be ready soon(in Sep.)
- •Update of control & monitoring system is ongoing.

#### ●Plan

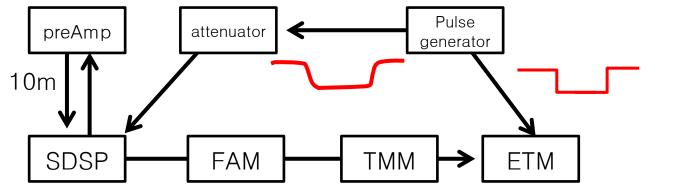
- ●ETM→GDL/GRL connection (Sep)
- Investigate optical link and FAM b2tt issues(Sep)
- Server replacement (Sep-Oct)
- •Slow control (Oct-)
- •Calibration study(TC E&T correction, fitter, pedestal, etc)
- •FAM fitter update(timing bias corr, double pulse fitter)
- •Link protocol update(to control all module by ETM)

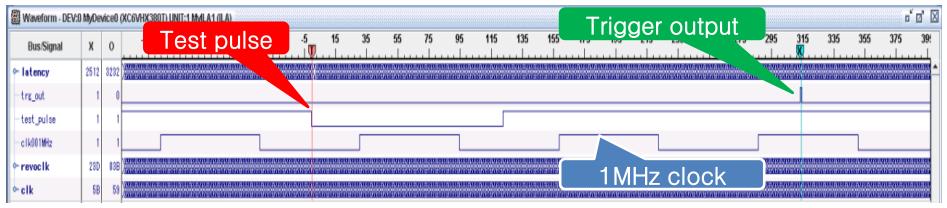
## backup



# Latency measurement

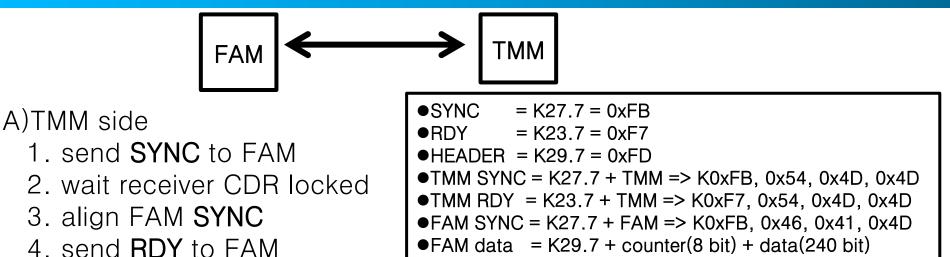
Latency at ETM output must be <u>< 3.5-3.7µs</u>
Yuriy prepared test pulse generator for us.





Latency(fit method) is measured to be ~2.5µs
 For simple method, latency was adjusted to be ~2.5µs

# Protocol (FAM↔TMM)



- 5. detect HEADER and align data
- 6. process data
- B)FAM side
  - 1. send SYNC to TMM
  - 2. wait receiver CDR locked
  - 3. align TMM SYNC or RDY (check only TMM character)
  - 4. if RDY sensed, start sending data

C)Protocol between TMM and ETM are same as FAM and TMM.

## Plan of system test after installation

- •Light yield check of all fiber using MultiFiberPro
- •Cable connection check using
  - Test pulse from FAM
  - •Test pulse from Collector
- FTSW installation for TMM
- Noise check
  - •Noise of each TC
  - Coherent noise
- •Temperature
- ●TC hit rate
- Pedestal level check and adjustment
- •Xtal by Xtal energy calibration (fast shaper on ShaperDSP)
- Latency estimation of each TC
- •Remote mcu firmware update check



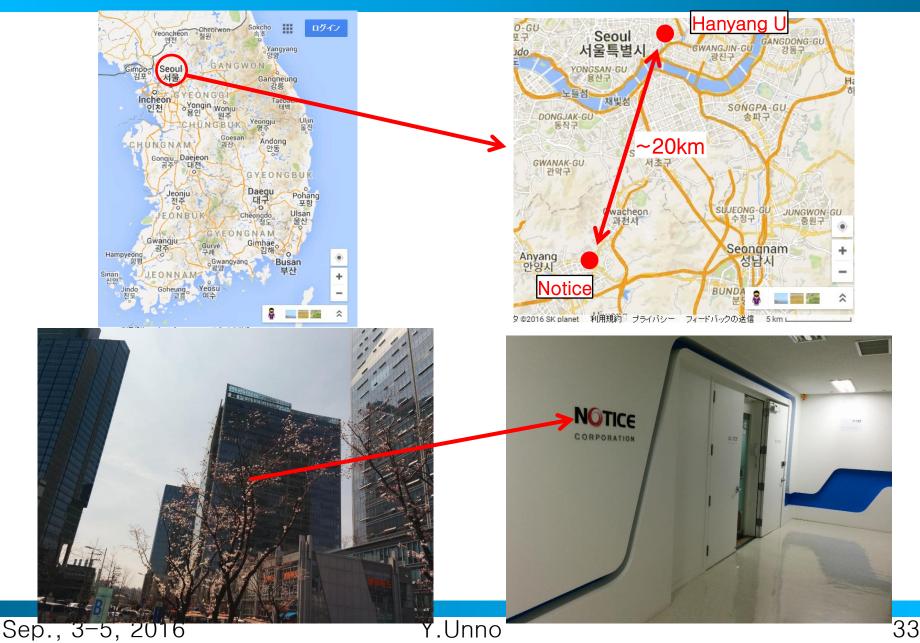
# CRT status

- Took data on 8/22.
  - •Trigger was based on only Barrel, but all Barrel TC.
  - •Trigger rate is ~1 kHz
  - •TC hit rate is ~60 Hz (TC energy threshold=30ADC~100MeV)
  - ●~30min. run and ~2M event
  - ●Data side ~6Gbyte
  - •No corrupted data was found !
  - •But, data to b2link was dummy (intentionally this time)

•ETM firmware modification is needed to take real cosmic data by b2link.

- •First, Sunghyun prepared firmware to send all TC data
  - •Too many BRAM comsumption
- •Sunghyun is modifying firmware to send only fired TC data to b2link
- •Memory resource, timing constraint, compile time problem exist
  - •those can be solved, but need more time.

## FAM and TMM test @ Notice



# FAM and TMM test @ Notice









# FAM(Check items)

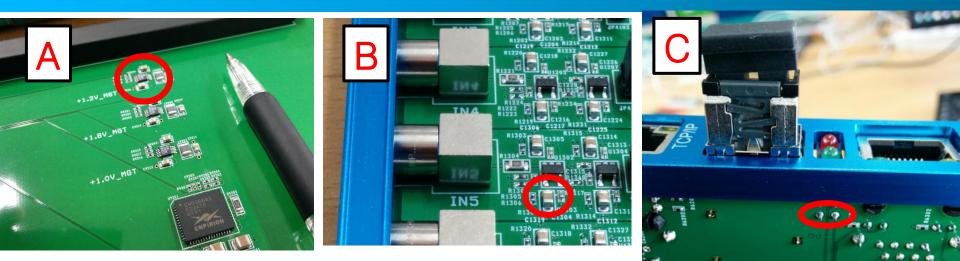
- •Firmware downloading MCU through 6 pin connector CPLD though 10 pin connector FPGA though 10 pin connector MGT and SFP check with ibert ●**RJ**45 TCP/IP communication •FTSW (all 4pins: ack, trg, rsv, clk) •LEDs nearby RJ45 and SFP •2 temperature sensors Noise of FADC output w/ and w/o ShaperDSP
- •TC E linearity and  $\sigma(E)$  using fitter
- TC analog sum output: linearity test

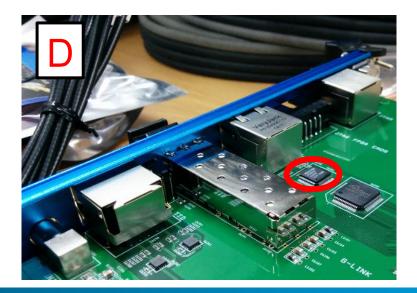
# TMM(check items)

# Firmware downloading MCU through 6 pin connector CPLD though 10 pin connector FPGA though 10 pin connector Optical transceiver check with ibert

- •RJ45
  - •TCP/IP communication
    - FTSW (all 4pins: ack, trg, rsv, clk)
- LEDs nearby RJ45 and SFP/QSFP
- •2 temperature sensors
- Lemo(127MHz) input

## FAM hardware problems









## FAM problem/update after mass production

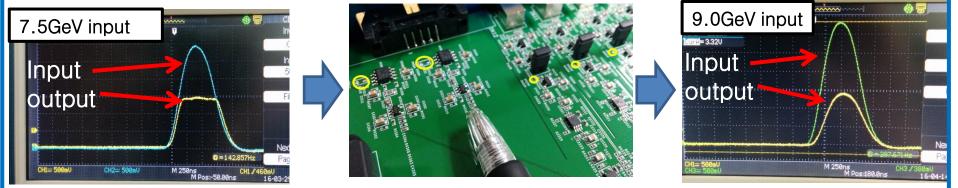
#### •FADC alignment problems were observed in 7 out of 60 FAMs



•OpAmp were from not reliable supplier because N (OpAmp) < less than MOQ.

●All OpAmp(3x60=180) are replaced to texas instruments products.

•Saturation of TC analog sum output



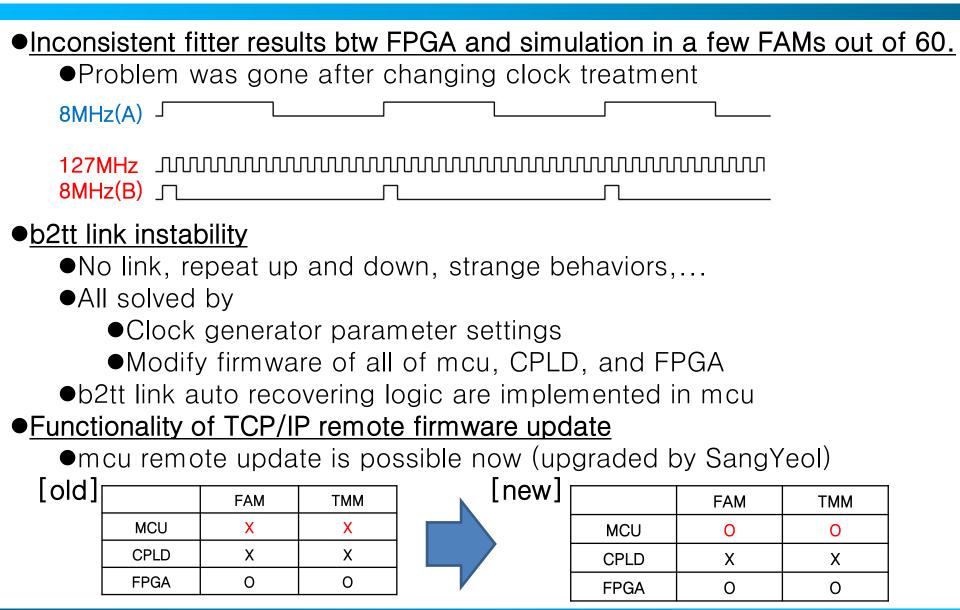
•2 registers(50 $\Omega$ ) and 12 registers(160 $\Omega$ ) / 1 FAM changed to 100 $\Omega$  and 910 $\Omega$ 

- •Gain change from 1.0 to 0.46
- •Took 2 days to replace 14x57=798 registers for all FAMs by SangYeol and SeungJun

Sep., 3-5, 2016

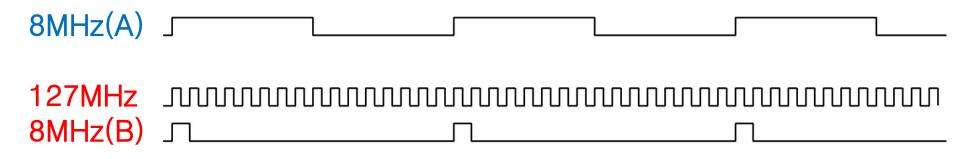
#### Y.Unno

## FAM problem/update after mass production



# FAM

- •Fitter results between FPGA and simulator were inconsistent in a few FAMs.
- •The problem was solved by following SangYeol's suggestion.



# (old) 8MHz(A) was used for 8MHz data timing (new) 8MHz(B) with 127MHz is used for 8MHz data timing

 Much less possibility to have signal timing shift due to each signal latency.

# TMM(ibert)

#### ~10min run for each TMM

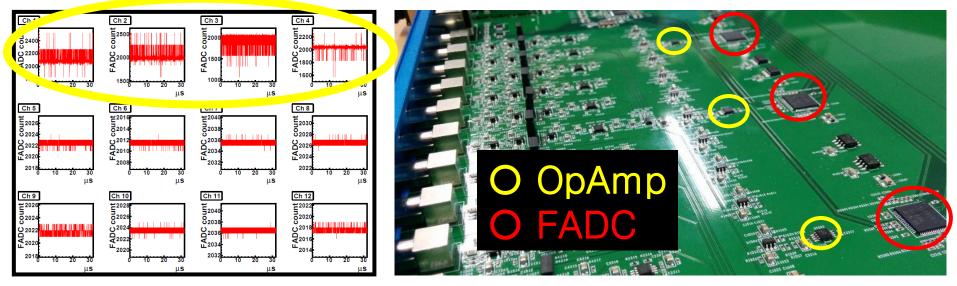
#### 1QSFP(TMM↔ETM)

#### 8 SFP(TMM↔FAM)

<b>ا</b> ه	IBER?	T Console - DEV	W MyDevice0 (XC7K325	5T) UNIT:1_0 MyIBERT	K7 GTX1_0 (BERT K	7 GTX)								
М	IGT/F	/BERT Settings	DRP Settings Port Set	ttings RX Margin A	malysis									
			GTX_X0Y0	GTX_X0Y1	GTX_X0Y2	GTX_X0Y3	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
۴	MG	GT Settings												
	- 1	MGT Alias	GTX0_115	GTX1_115	GTX2_115	GTX3_115	GTX0_117	GTX1_117	GTX2_117	GTX3_117	GTX0_118	GTX1_118	GTX2_118	GTX3_118
	E.	Tile Location	GTX_X0Y0	GTX_X0Y1	GTX_X0Y2	GTX_X0Y3	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
	- 1	MGT Link Status	6.25 Gbps	6.25 Gbps	6.25 Gbps	6.25 Gbps	3.125 Gbps	3.125 Gbps	3.125 Gbps	3.125 Gbps	3.125 Gbps	3.125 Gbps	3.125 Gbps	3.125 Gbps
	E /	PLL Status	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED
	- 1	Loopback Mode	None 💌	None	None 💌	None 💌	I one 💌	None	None	None	None	None 💌	None	None
	E_ /	Channel Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset
	- 7	TX/RX Reset	TX Reset RX Reset	TX Reset RX Reset	TX Reset RX Reset	TX Reset RX Reset	1 ( Reset   RX Reset	TX Reset RX Reset	TX Reset RX Reset	TX Reset RX Reset	TX Reset RX Reset	TX Reset RX Reset	t TX Reset RX Reset	TX Reset RX Rese
	E.	TX Polarity Inven												
	- 1	TX Error Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject
	E 1	TX Diff Output	850 mV (1100) 💌	850 mV (1100) 💌	850 mV (1100) 💌	850 mV (1100) 💌	850 mV (1100) 💌	850 mV (1100) 💌	850 mV (1100) 🔻	850 mV (1100) 💌	850 mV (1100)			
	F 7	TX Pre-Cursor	1.67 dB (00111) 💌	1.67 dB (001 🔻	1.67 dB (001 🔻	1.67 dB (001 🔻	: 67 dB (001 🔻	1.67 dB (001 🔻	1.67 dB (001 🔻	1.67 dB (001 🔻	1.67 dB (001 🔻	1.67 dB (001 🔻	1.67 dB (001 🔻	1.67 dB (001 🔻
	F. *	TX Post-Cursor	0.68 dB (00011) 💌	0.68 dB (000 💌	0.68 dB (000 💌	0.68 dB (000 💌	68 dB (000 💌	0.68 dB (000 💌	0.68 dB (000 💌	0.68 dB (000 💌	0.68 dB (000 💌	0.68 dB (000 💌	0.68 dB (000 💌	0.68 dB (000 💌
	- 1	RX Polarity Inven												
	E.*	Termination Vo	Programmable 💌	Programmable 💌	Programmable 💌	Programmable 💌	Foorammable 💌	Programmable 🔽	Programmable 🔽	Programmable 🔻	Programmable 🔽	Programmable 🔽	Programmable 💌	Programmable
	L 7	RX Common M	900 mV 💌	900 mV 💌	900 mV 💌	900 mV 💌	200 mV 💌	900 mV 💌	900 mV 💌	900 mV 💌	900 mV 💌	900 mV 💌	900 mV 💌	900 mV
٩	BEP	RT Settings												
	- 1	TX Data Pattern	PRBS 31-bit	PRBS 31-bit 💌	PRBS 31-bit 💌	PRBS 31-bit 💌	F RBS 31-bit 💌	PRBS 31-bit 💌	PRBS 31-bit 💌	PRBS 31-bit 💌	PRBS 31-bit 💌	PRBS 31-bit 💌	PRBS 31-bit 💌	PRBS 31-bit
	E /	RX Data Pattern	PRBS 31-bit 💌	PRBS 31-bit 💌	PRBS 31-bit 💌	PRBS 31-bit 💌	F RBS 31-bit 💌	PRBS 31-bit 💌	PRBS 31-bit 💌	PRBS 31-bit 💌	PRBS 31-bit 👻	PRBS 31-bit 👻	PRBS 31-bit 💌	PRBS 31-bit
	- 1	RX Bit Error Ratio	2.124E-013	2.124E-013	2.128E-013	2.128E-013	4.259E-013	4.260E-013	4.261E-013	4.265E-013	4.266E-013	4.270E-013	4.271E-013	4.279E-013
P	<u> </u>	RX Received Bit.	4.709E012	4.708E012	4.700E012	4.699E012	2.348E012	2.348E012	2.347E012	2.345E012	2.344E012	2.342E012	2.341E012	2.337E012
U	F /	RX Bit Error Co	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000
1	- 1	BERT Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset
9	Clo	ocking Settings												
	<u>F_</u> 7	TXUSRCLK Freq.	156.31	156.31	156.31	156.31	78.16	78.16	78.16	78.16	78.16	78.16	78.16	78.16
	- 7	TXUSRCLK2 Fre.	156.31	156.31	156.31	156.31	78.16	78.16	78.16	78.16	78.16	78.16	78.16	78.16
	- 1	RXUSRCLK Freq.	156.28	156.28	156.31	156.31	78.16	78.16	78.16	78.16	78.16	78.16	78.16	78.16
	L 7	RXUSRCLK2 Fre	156.28	156.28	156.28	156.28	78.16	78.16	78.16	78.16	78.16	78.16	78.16	78.16

# FADC alignment problem

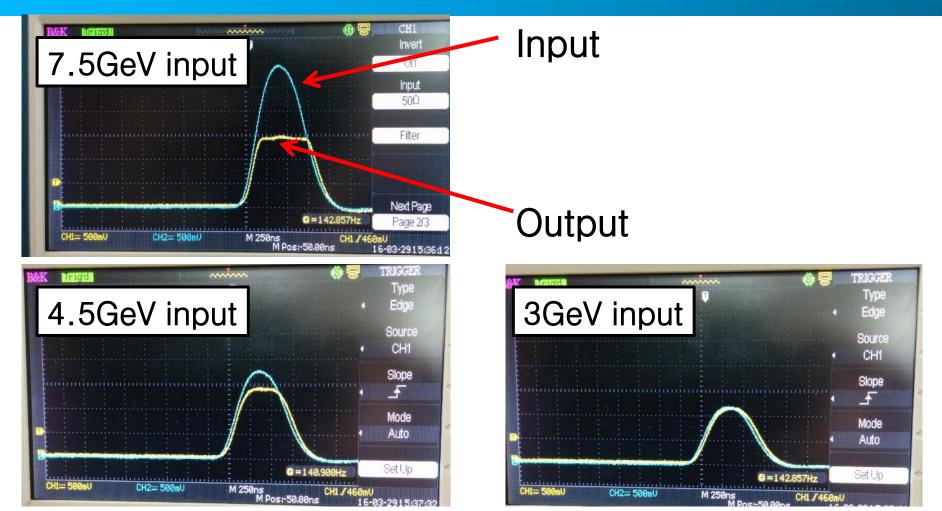
#### •FADC alignment problems were observed in 7 out of 60 FAMs



 OpAmp were from not very reliable supplier because # of OpAmp needed was less than MOQ.

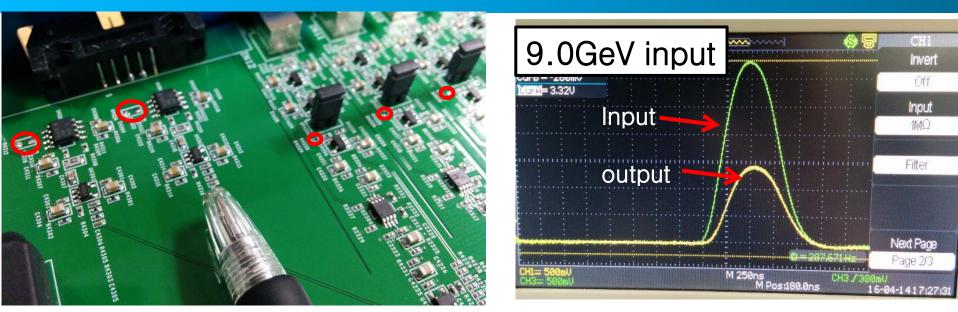
- •SangYeol got reliable ones(texas instruments)
- •All OpAmp(3x60=180) are replaced to reliable ones.
- •The problem was gone.

## Saturation of TC analog sum output



 In addition, register in V→I convertor for analog sum output on FAM was designed to be 50Ω by assuming 50Ω register on luminosity monitor, but it's 100Ω...

## Saturation of TC analog sum output

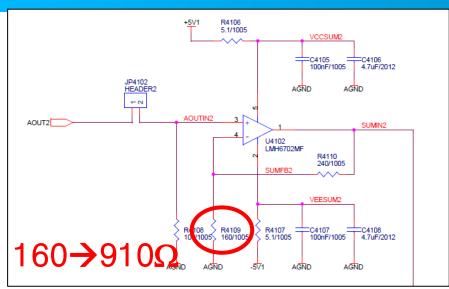


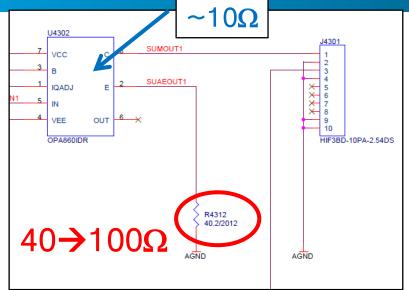
2 registers(50Ω) / 1 FAM were replaced to 100Ω
12 registers(160Ω) / 1 FAM were replaced to 910Ω
Gain:

- •Original ~1.0
- •New ~ 0.46

 It took 2 days to replace 14x57=798 registers in total by SangYeol and SeungJun

## Register replacement for analog sum





Original gain =

 [10/(10+40)] x [(240+240)/240] x
 [(240+160)/160] x [50/(10+40)] = ~1.0
 (assuming 50Ω register at luminosity monitor)

•New gain =

 $[10/(10+40)] \times [(240+240)/240] \times$ 

 $[(240+910)/910] \times [100/(10+100)] = -0.46$ 

(assuming  $100\Omega$  register at luminosity monitor)

# Clock chip(cdce62005) problem

•b2tt link was often not up for 3 FAMs.

- Sometimes it is up after VME power recycle, but in most cases, it does not goes up state.
- Problem appears when;
  - •FTSW and FAM are on at same time
  - •FTSW is on after FAM is on.
- •Reason:
  - •Parameters of PLL in clock chip was not optimized well.
  - •Many parameters and combinations, not easy to optimize

### Solution:

- Change the parameters back to default ones in data sheet (by assuming the default ones are optimized).
- •Change clock frequency of input clocks to PLL to use default parameter setting to PLL.