# *Trigger Timing Distribution*

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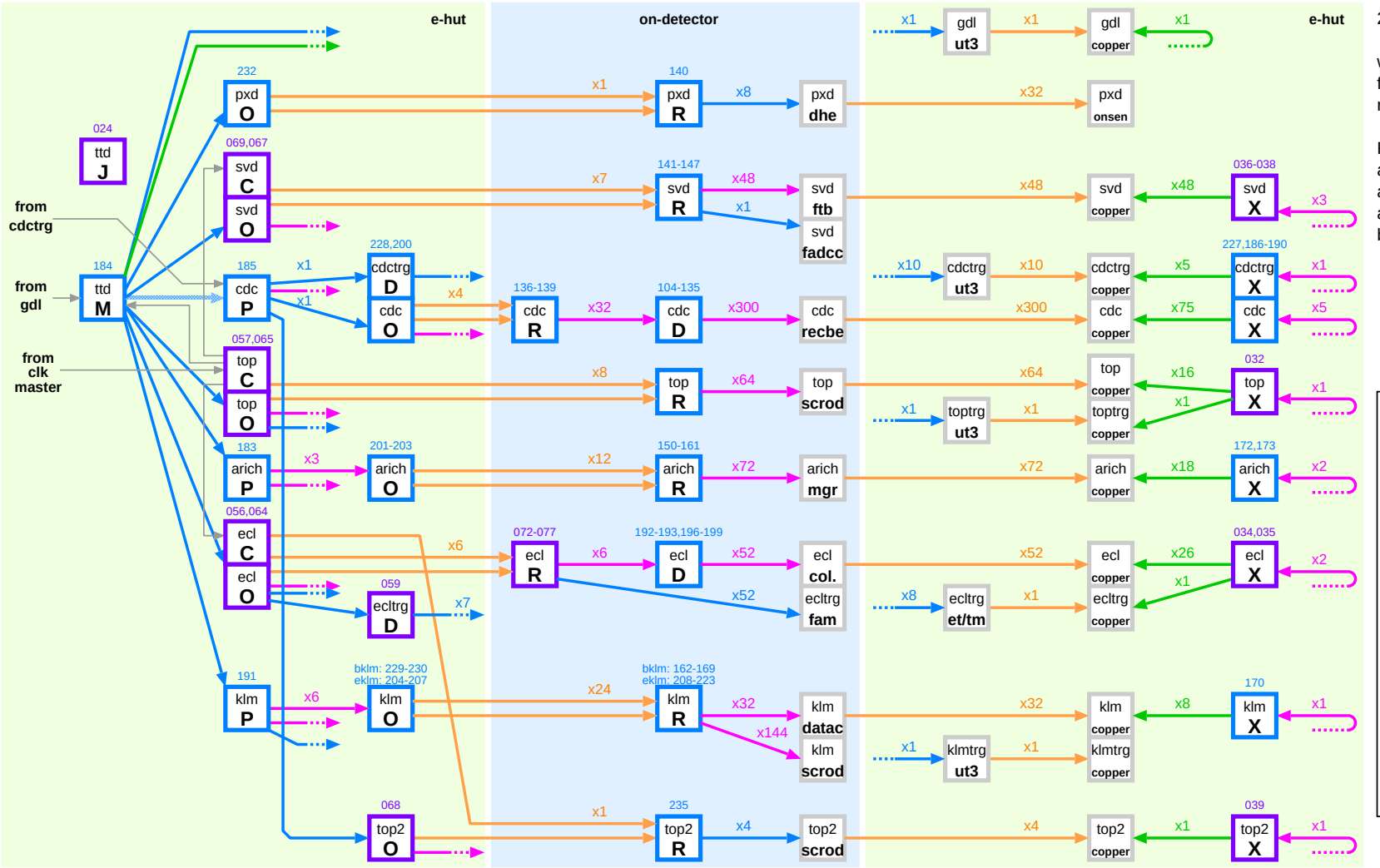
# Topics

- **E-hut/B4 status and near term connection plan**
- **FTSW module got broken**
- **Bug fixes**
  - Event number shift problem
  - Broken header problem
  - hslb 0.54 problem
- **JTAG-over-b2tt**
  - firmware readback
  - ZYNQ processor programming
- **New major revision**
  - Motivation
  - New features

# TTD tree




2016.06.20 version

with second TOP2 for CDC+TOP readout at B4

For beast phase2, a second master and PXD2 are added, and TOP2 becomes SVD2

**Glossary**

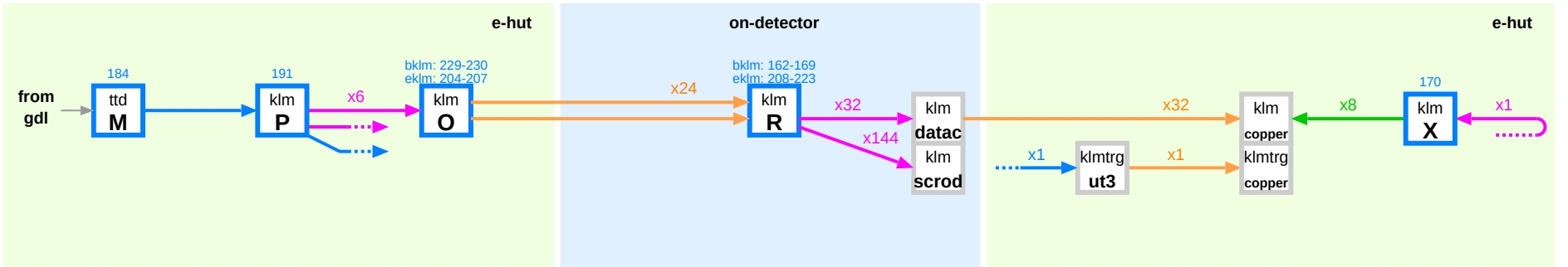
**FTSW nodes**
- M: master
- P: primary
- O: optical
- R: receiver
- D: distributor
- X: copper/ttrx
- J: jtag

- b2tt on CAT7
- b2tt/B2L optical
- b2tt+JTAG
- ttrxlink
- clock

- No change since 2016.6 B2GM

# Near term plan for KLM

- **Full Barrel connection scheduled in 2016.9.12–19 with Isar**
- **ft3o firmware problem**
  - ft3o is in a crate with no VME CPU
  - ft3p to ft3o connection had a problem in the default setup (CDC's ft3p is controlled by a VME CPU)
  - ft3p firmware has been intensively updated in 2016.6–7
  - KLM configuration is now tested in B2
- **Optical fiber problem**
  - fiber from patch panel to FTSW on the detector had no light output
  - it should be fixed now



# FTSW module got broken

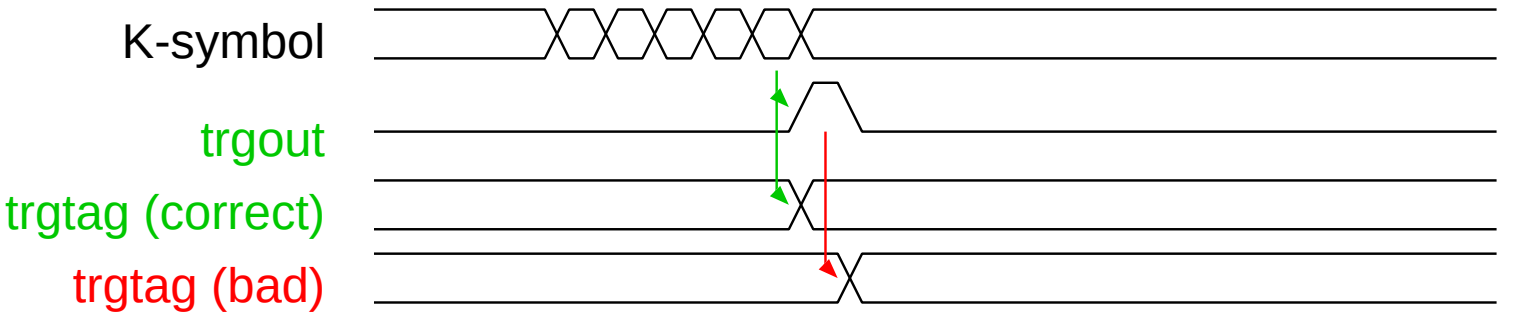
- **FTSW #058 used by ARICH group around end of 2016.6**
  - This module has been heavily used by the TOP group
  - Virtex 5 FPGA could not be accessible by JTAG at all
  - Rest of the JTAG chain was confirmed to work
  - Could not apply +2.5V voltage to VCCAUX/VCCIO
  - No help by replacing regulator / 2.5 V from elsewhere
  - No way for any partial use if Virtex 5 cannot be programmed
- **FTSW #025 used by ARICH group around end of 2016.8**
  - This module has also been heavily used by the TOP group
  - So far probably only OUT-6 and OUT-8 RJ-45 ports are affected: these cannot be used for JTAG programming
  - ARICH group will keep using the other ports
- **Reason: static electric shock (?) large current draw (?)**
- **Action plan:** since FTSW2 spare is getting short, make more FTSW3 and replace **six** FTSW2 in COPPER crates with FTSW3.

# Event number shift problem

- Two event tags from b2tt:

```
trgtag   : out std_logic_vector (31 downto 0);
fifodata : out std_logic_vector (95 downto 0);
```

- The latter for Belle2link header, the former for users
- They have to be available at the next clock upon `trgout`
- While trying to simplify the code, the event tag was incremented after seeing trgout, i.e., it was not incremented at the next clock of `trgout`
- It was okay in b2tt-0.40 (2015.05.28), both were wrong in b2tt-0.45 (2016.04.07), I noticed and fixed but only in the fifodata in b2tt-0.46 (2016.04.07) and used in DESY test
- Now it's fixed in b2tt-0.48 (2016.06.29)



# Broken Belle2link header problem

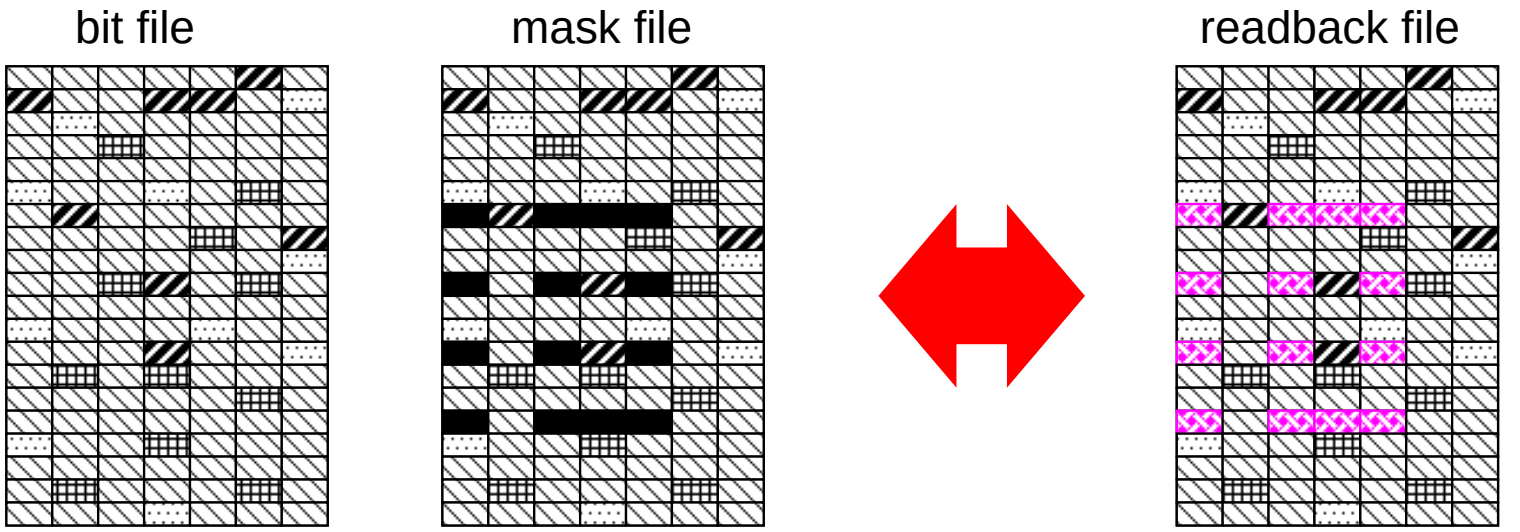
- There was a long standing broken header problem in the ECLTRG Belle2link:
  `0xffffffff 0xffffffff 0xfffffff2` (`fifodata` is simply bad).
- Sunghyun Kim identified that it happens when the trigger interval is just around the end of a Belle2link event transaction.
- Bug was in the `ttnext` (belle2link out) $\rightarrow$ `fifonext` (b2tt in) signal timing.
- `ttnext` should be issued when the belle2link header is filled, but it was deferred to the end of the event. Mishap might have happened when the belle2link state machine was revised.
- This bug is in belle2link 0.16, fixed in **belle2link 0.18** together with **b2tt 0.48**.
- I thank and apologize Sunghyun for reporting this and taking such a long time to fix.

# hslb 0.54 problem

- **hslb 0.54** was released together with **belle2link 0.16** to fix the long-standing parameter read problem
- It meant to clean up the state machine including some suspicious piece of code in **hslb 0.52**
- However, it was reported that **parameter read sometimes fails** with "Timer expired" message with hslb 0.54 + belle2link 0.16, while it does not happen with hslb 0.52 + belle2link 0.16
- First reported by TOP, also found by ECL, and I could also reproduce in B2
- So far no further investigation has been made (lower priority), and **hslb 0.52 is recommended**.

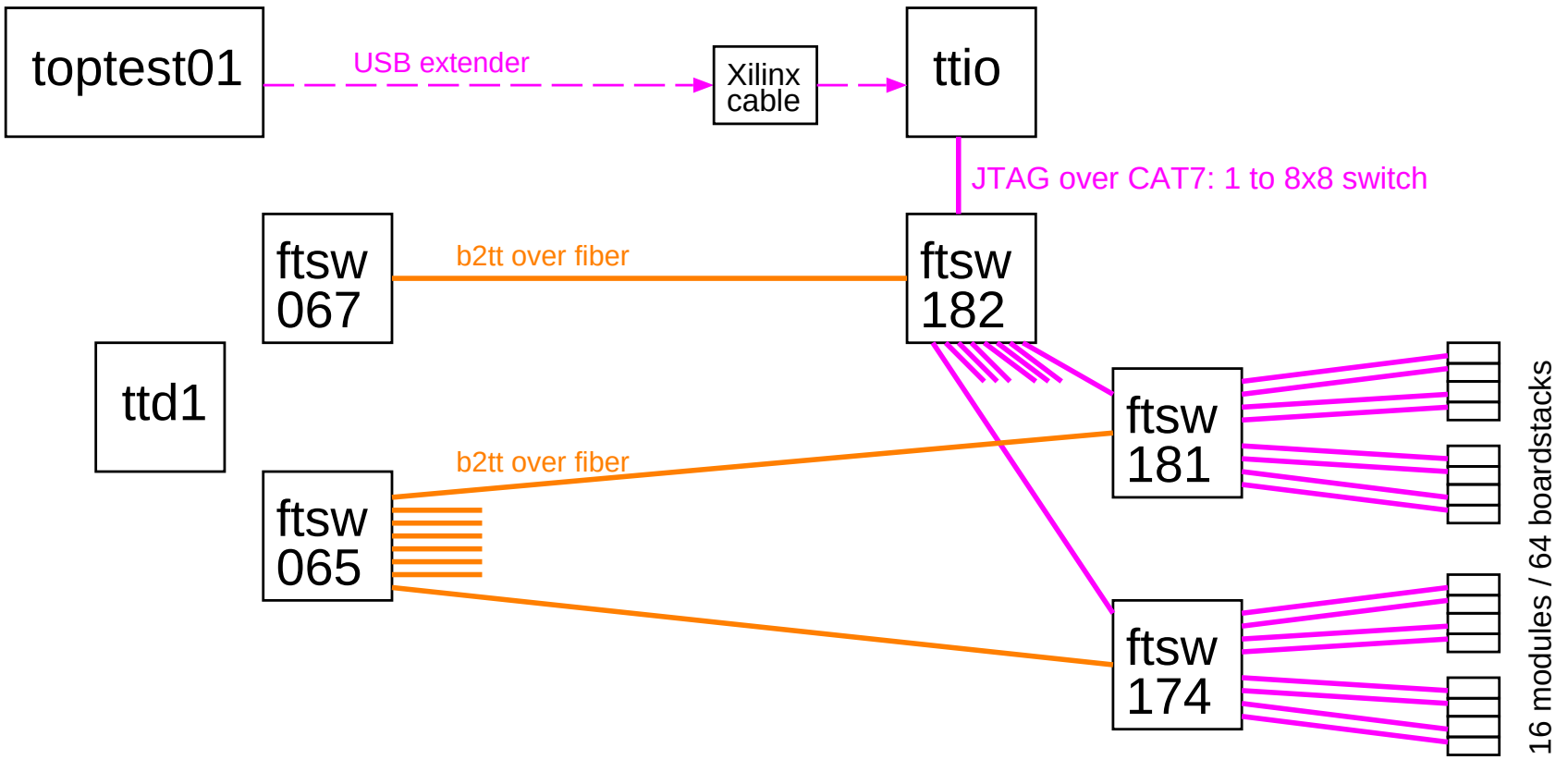
# JTAG readback

- **jtagft** can readback the bit stream of Virtex 5
- Then programmed bit file can be verified with a mask file
- There was some bit error when it was reported at 2016.6 B2GM
- Then Hanjin Kim (Yonsei) fixed the bug in TDO read timing
- It should be usable for Virtex 5 of CDC and ARICH
- Implementating it for other Xilinx FPGA should not be difficult



# ZYNQ processor programming

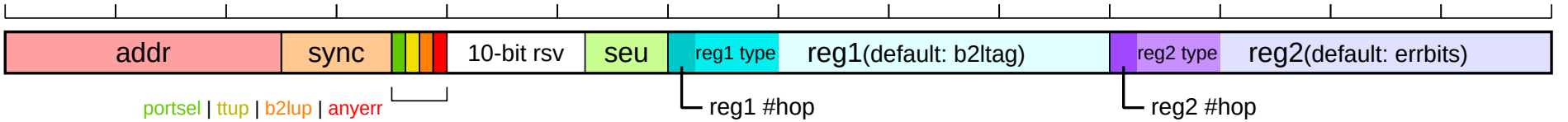
- Not much progress in programming ARM processor
- Youngmin Yook is still working remotely from Yonsei
  (he cannot visit KEK due to military obligation)
- TOP is operated with this temporary configuration for a while
  (if not forever…)



# New major b2tt revision — motivations

- **FEE/FTSW status only through 112-bit payload per b2tt link**
  - Many FTSWs and FEEs are cascaded behind the link, not easy to collect all needed info
  - Current b2tt is already packing bits and switching banks, but many of them are not accessible without breaking links and generating errors
  - More info to be added, but no more space in the current format
- **Wishlist examples**
  - Multi-bit info to tell the **source of busy / error**, e.g., which FEE (FTSW port), whether DHH or ONSEN, …
  - Reading back the result of ttaddr mask list
  - Version of b2tt, utime info (when the FPGA was programmed), …
- **Code and format cleanup**
  - Current format is the result of many adhoc additions…

# New b2tt ACK-payload format




- 20-bit address **to identify the source of the payload**
  - Address is assigned by `ttaddr`
  - Usually the directly connected FTSW/FEE is visible
  - It could be the hops behind by selecting port (selport=1)
- 3 Error bits **are persistent regardless the selport**
- SEU count **to collect the sum of the number of SEUs**
- Two registers **as window to access more bits**
  - 2-bit #hop, 6-bit type, 24-bit data
  - reg1 is state dependent, to tell error source upon error
  - If no error, b2ltag to tell how many events are written to belle2link
  - reg2 is user controlable to access more info

# Merging / selecting registers

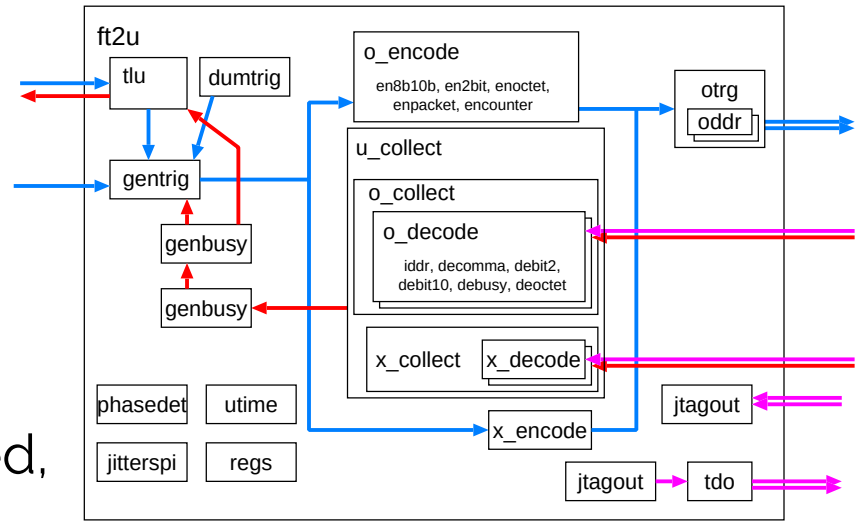
- **How to decide what to report**
  - If error occurs locally, the error is reported to upstream
  - If error occurs in the downstream, error bits are merged, and a bit pattern of errorneous port is reported to upstream
  - If multiple types of error occurs, the higher priority one is reported
  - If port selection is requested, the specified port is just transfered
  - These different cases are identified from data itself
- **List of registers**

```
subtype ttreg_t  is std_logic_vector (4 downto 0);
constant TTREG_CKLOST : ttreg_t := "10111"; - 23
constant TTREG_TTDOWN : ttreg_t := "10110"; - 22
constant TTREG_TTLOST : ttreg_t := "10101"; - 21
constant TTREG_TTERR  : ttreg_t := "10100"; - 20
constant TTREG_FEEEON : ttreg_t := "10011"; - 19
constant TTREG_FEEERR : ttreg_t := "10010"; - 18
constant TTREG_LKDOWN : ttreg_t := "10001"; - 17
constant TTREG_LKLOST : ttreg_t := "10000"; - 16
constant TTREG_IDELAY : ttreg_t := "01111"; - 15
constant TTREG_RDELAY : ttreg_t := "01110"; - 14
constant TTREG_BUSY   : ttreg_t := "01101"; - 13
constant TTREG_ERRBIT : ttreg_t := "01100"; - 12
  .
```

Work in progress
not a final list

# How to proceed

- **Originally "Target date is** (hopefully) **September DAQWS"**
- **b2tt is done** 🙂 **but every FTSW firmware has to be updated** ☹
- **Pocketdaq version** (ft2u) **is the initial target**
  - Most of the components used in the other firmware are included
  - Componenents modifiied for ft2u can be used elsewhere with no change
  - About 60% of code writing is done




- **Backward compatibility**
  - Location of sync counter is changed, to be able to detect whether new b2tt is connected or not
  - Current FEE firmware should work with limited status info

# Summary

- **TTD commissioning is on-going, next target is KLM**
- **Broken FTSW is worrisome, considering more production**
- **Firmware updates yet to be made**
  - b2tt to be updated for better monitoring and diagnosis
  - JTAG-over-b2tt for ZYNQ is still long way to go
  - (not discussed today) Trigger type, etc, from GDL
  - (not discussed today) Deadtime monitoring and minimization