A prototype readout ASIC for the RICH detector

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1. Background

RICH (Ring Imaging CHerenkov) detector is one of the candidates for PID (Particle Identification) at STCF (Super tau-Charm Facility). The total area of the RICH detector is 16 m^2. The requirements of the readout electronics for the RICH detector are responsible for both high-precision charge and time measurement. The detailed requirements of the readout electronics are shown in Table 1.

Table. 1. Requirements for the electronics.

Parameter	Value
Total readout channels	698,880
Range of charge	1 fC ~ 48 fC
Equivalent noise charge (ENC)	< 0.5 fC RMS @ 20 pF Cin
Time resolution	≤ 1ns RMS @ 20 pF Cin
Maximum event rate	16 kHz

As for the MPGD (Micro Pattern Gas Detector) detector, the channel number of the readout electronics is quite large. Meanwhile, it also requires high precision signal measurement. This demands that the electronics must feature high density, low noise, and low power consumption, and thus it is necessary to employ suitable ASIC (Applications Specific Integrated Circuit) to satisfy these requirements.

2. ASIC ARCHITECTURE

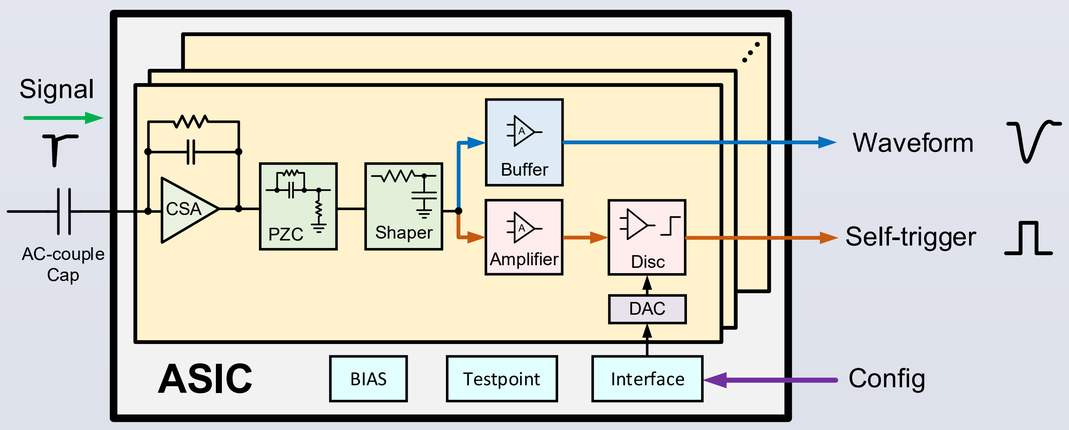

Fig. 1. Block diagram of the prototype ASIC.

Fig. 1 shows the block diagram of the ASIC. Each channel mainly consists of five parts: a Charge Sense Amplifier (CSA), a pole-zero cancellation (PZC), a shaper, a discriminator, and a 7-bits DAC.

The CSA consists of an amplifier, a feedback capacitor, and a reset circuit. The values of the feedback resistor and capacitor of the CSA can be changed through configuration, thus providing different charge measurement ranges. Due to the slow decay of the CSA output signal, a pole-zero cancellation circuit is used to make the output signal return to its baseline quickly.

The output signal of the PZC is then fed to a shaping circuit that outputs a Semi-Gaussian pulse, meanwhile enhancing the Signal-to-Noise Ratio (SNR). T-bridge filter is employed in this circuit design which achieves a 2-order low-pass filter. When using the peak value of the output waveform to calculate the charge information, it is necessary to select the appropriate shaping time to avoid a ballistic deficit. Considering the possible changes of the output signal duration from the detector in the future, five different shaping times are designed in the R&D stage.

The filtered signal is compared at the discriminator block to a programmable threshold value. This value is set by a 7-bits DAC to adapt the gain non-uniformity among channels and can be configured per channel. If the signal crosses the threshold, the discriminator outputs a self-trigger signal to the back-end signal processor.

The filtered signal is also sent to the back-end signal processor by a buffer with a class-AB structure. And we can obtain the charge information through peak detection or area calculation of the waveform. Meanwhile, time information can be obtained using a leading-edge discrimination method.

3. TEST RESULTS

A. Test Setup

The chip with a die size of 6752 μm x 5002 μm is housed in a 208-pin Ceramic Quad Flat Pack (CQFP-208) shown in Fig. 2. The test setup is shown in Fig. 3, and all the chip functionalities have been validated. The power consumption of each channel is only 9.6 mW.

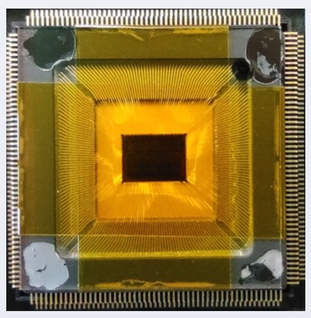

Fig. 2. Photo of the prototype chip.

Fig. 3. Test setup for the prototype chip.

B. Linearity

Fig. 4 shows the response of the chip to 5 different input charges in 48 fC dynamic range, and all of them are in good shape consistency. Fig. 5 shows the fitting result of the peak value of output versus input charge. The gain is 18.52 mV/fC and the INL (Integral Non-Linearity) is 0.97 %, satisfying the requirements.

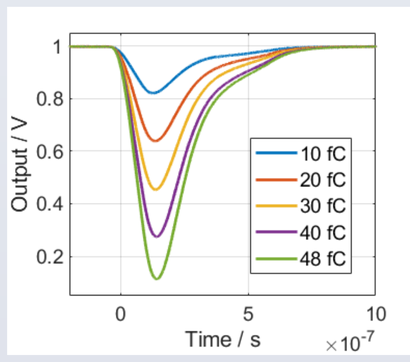

Fig. 4. Output versus input charge.

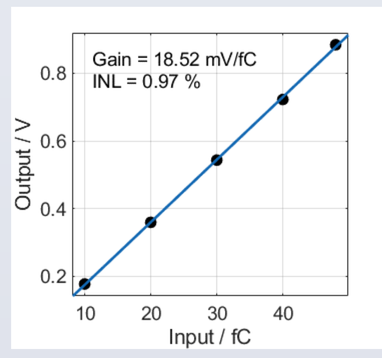

Fig. 5. Gain and INL.

C. Noise

Fig. 6-8 shows the ENC (Equivalent Noise Charge) versus dynamic range, input capacitance, and shaping time. The shaping time is defined as the time taken from 5% to 100% of the leading edge of the output. The ENC increases as the shaping time decreases or the input capacitance increases. The ENC remains to be lower than 0.5 fC in the 48 fC dynamic range even with an input capacitance up to 50 pF, meeting the requirements.

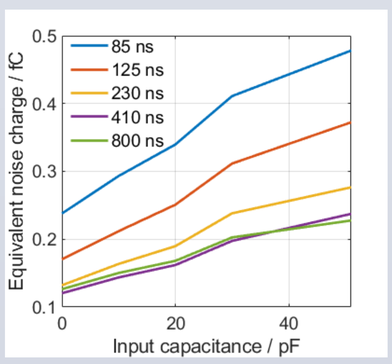

Fig. 6. ENC of 48 fC range.

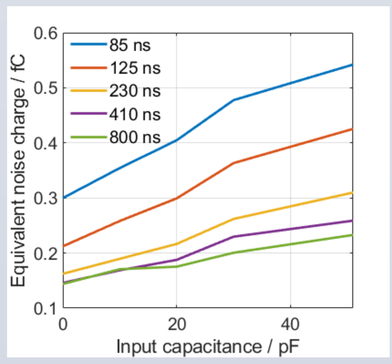

Fig. 7. ENC of 96 fC range.

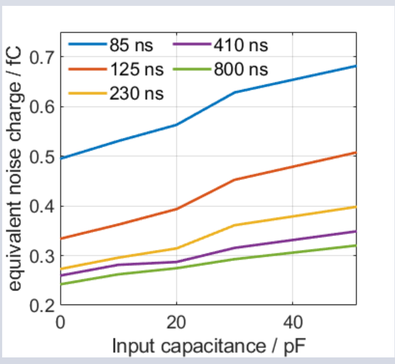

Fig. 8. ENC of 240 fC range.

4. SUMMARY AND FUTURE PLAN

A new prototype readout ASIC has been developed for the RICH detector. The chip has been under test and the test results meet the requirements. The ENC is less than 0.5 fC with an input capacitance up to 50 pF. The maximum INL equals 0.97 % and the power consumption is only 9.6 mW per channel. Modifications and improvements of the present ASIC will also be considered soon.

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