A custom readout electronics for the BESIII CGEM detector

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Instrumentation for Colliding Beam Physics (INSTR-17)
Novosibirsk, Russia
27 February - 03 March, 2017

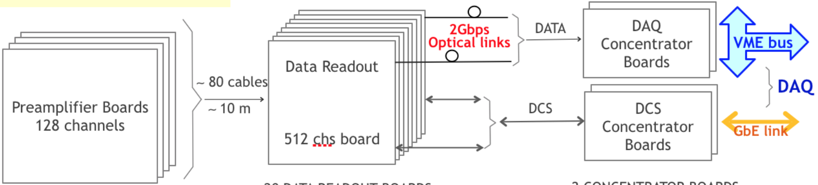
The BESIIICGEM project has been funded by European Commission within the call H2020-MSCA-RISE-2014.

Outline

1. Overview of the readout electronics for the BESIII-CGEM
2. On-detector Electronics: Design of a dedicated ASIC for CGEM Readout
3. Preliminary results from TIGER Prototype
4. On-detector Front-end Board
5. Off-detector Electronics
6. Outlook for the CGEM electronics

ON-DETECTOR ELECTRONICS
~ 10 000 CHANNELS

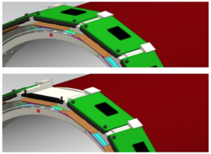
OFF-DETECTOR ELECTRONICS



160 ASIC -> 80 BOARDS

20 DATA READOUT BOARDS

2 CONCENTRATOR BOARDS



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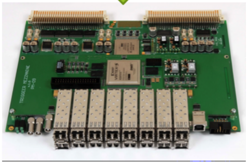

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Outline

Front End ASIC for CGEM Readout

- Analogue readout of the CGEM:[1]
  - enables the use of a charge centroid algorithm
  - improves spatial resolution to better than 130 μm, while loosening the pitch strip to 650 μm
  - total number of channels ≈ 10 000

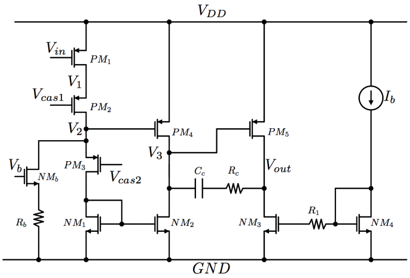
↪ 10 000 Channels in 80 Front-end Boards

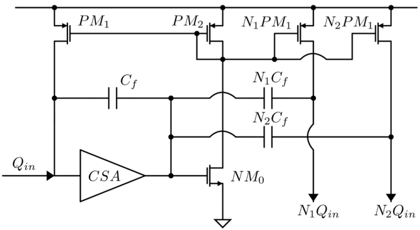
↪ 2 ASICs per FEB

↪ readout with 160 dedicated integrated 64-channel front-end ASICs

- should provide **time and charge measurement** and feature a fully-digital output
- Expected signal from CGEM: 30-50 ns Duration, 30-40 ns rising time, 10 ns falling time
  - depends on gas mixture, gain and electric field
- Input charge: 1 - 50 fC
- Up to 100 pF sensor capacitance
- 60 kHz Rate per Channel (safety factor of 4 included)
- 4-5ns Time resolution
- Power below 10 mW/channel
- SEU-tolerant

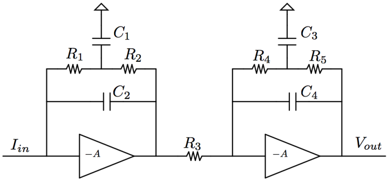
[1] *Lia Lavezzi, "The new Cylindrical GEM Inner Tracker of the BESIII experiment: test beam results of two prototypes".*

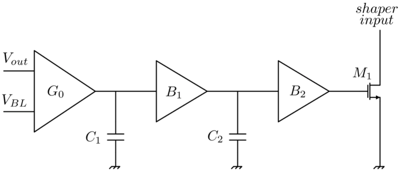


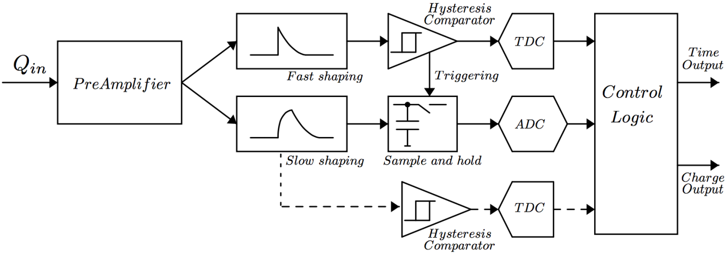


- low-noise two-stage cascode charge sensitive amplifier
- signal range Qin = 1 - 50 fC on a Cd = 100 pF detector
- target ENC 800 electrons
- up to 80 mS (4 mA bias current) on input PMOS
- Gain = 10 mV / fC
- operation in μ - TPC mode: requirement for a 5 ns time resolution
- signal split for time and charge measurement branches in two dedicated shapers

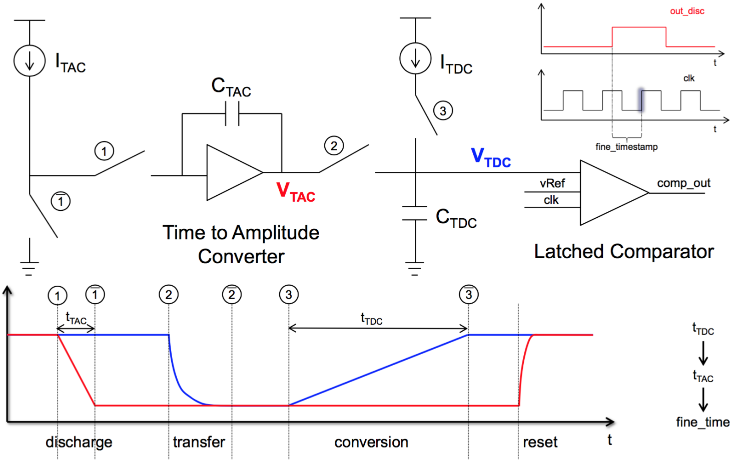
- 4 complex conjugate poles, peaking time defined by feedback loop RC
- semi-Gaussian output signal shape
- maximum signal width 1 μs on energy shaper, pile-up probability $< 1\%$ at 60 kHz
- 250 ns peaking time on energy branch, minimises ENC for charge measurement
- 60 ns peaking time for fast shaper, targets low-jitter timing measurement
- baseline DC (typ 300 mV) imposed by BLH circuit
  - transconductance function is slew-rate limited, rejects variations caused by fast signals
  - dominant time constant $\tau = 1.5$ ms generated with very small bias currents





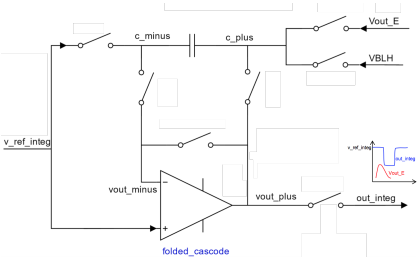


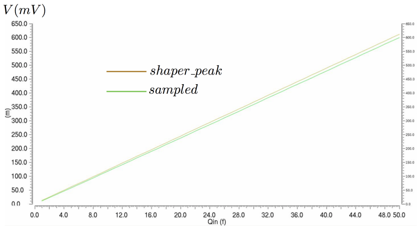
- **Time-based readout**
  - single or double threshold
  - time stamp on rising/falling edge (sub-50 ps binning quad-buffered TDC)
  - charge measurement with Time-over-Threshold
- **Time and amplitude sampling**
  - time stamp on rising edge (sub-50 ps binning quad-buffered TDC)
  - Sample-and-Hold circuit for peak amplitude sampling
  - slow shaper output voltage is sampled and digitised with a 10-bit Wilkinson ADC



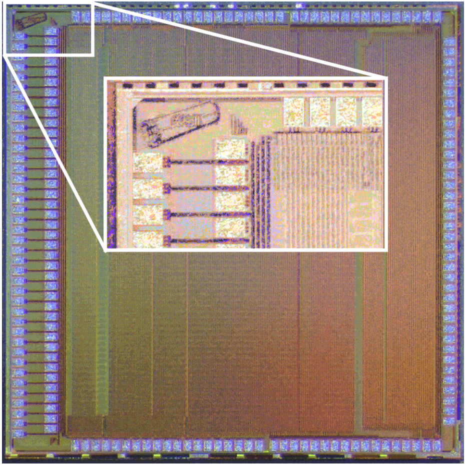
- **Low-power analogue TDC** is based on time interpolation, event de-randomization with multiple hit buffering (4x TAC)
- interpolation factor 128 : time binning $< 50ps$ with a 160 MHz clock

S/H amplitude measurement - principle of operation





- quad-buffers for voltage sampling, S/H circuit shares Wilkinson TDC for digitisation
- sampling starts at rising edge of fast (Time) or slow (Energy) shaper output
- sampling time (target equal to peaking time) **is programmable**, defined by simulation and confirmed by parameter scan in silicon
- deviation on measured amplitude *versus* peak amplitude, due to time-walk, is corrected by calibration



- 64 channels: VFE, signal conditioning, TDC/ADC, local controller
- Digital backend inherited from TOFPET2, SEU protected
- on-chip bias and power management
- on-chip calibration circuitry
- fully digital output, LVDS IO
- 4 TX SDR/DDR links, 8B/10B encoding
- SPI configuration link
- power below 10 mW per channel
- nominal 160 MHz system clock
- sustained rate per channel: above 100 kHz
- 25 mm^2 UMC110 CMOS
- tapeout of first silicon: MPW May 2016

Outline

Status of ASIC Test Activities, in a nutshell

Summary of activities

- Electrical characterisation started November 2016 - tests on 6 chips
- Preliminary tests with diodes ongoing
- Test with planar and cylindrical GEM starting in March
- Trial TID run on testboards done, high-dose TID and SEU tests planned for mid-2017

Summary of characterisation runs

✓ R/W Channel/Global configuration registers

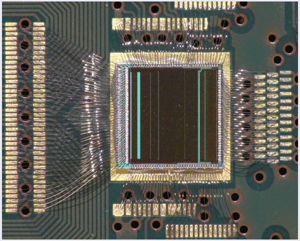
✓ Data TX and decoding

✓ (dual-) TDC operation and fine calibration
  - quantisation error lower than 40 ps r.m.s.

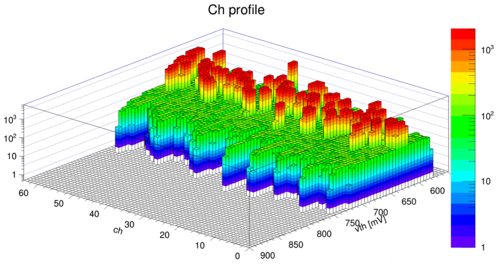
✓ Front-end performance
  - internal calibration circuitry
  - external charge injection (spy channel)
  - Charge measurement: Time-over-threshold
  - Charge measurement: S/H

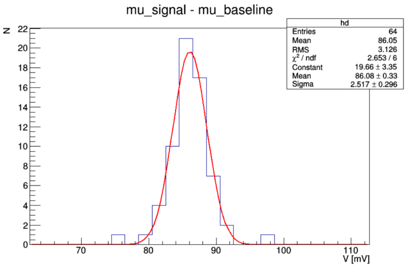
✓ Baseline and threshold equalisation

✓ Channel intrinsic noise: noise vs. Cin (ongoing)



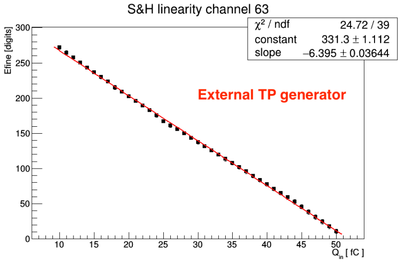
- Injection of Q=8fC with internal test-pulse
- ✓ Average gain above 10mV/fC (expected 11mV/fC from post-layout simulations)
- residual channel-to-channel dispersion (0.2 mV/fC r.m.s.)
- ✓ results after baseline equalisation: below 25 mV r.m.s. dispersion on the DC operating point

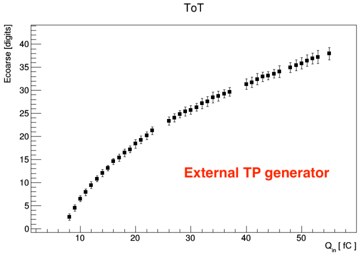


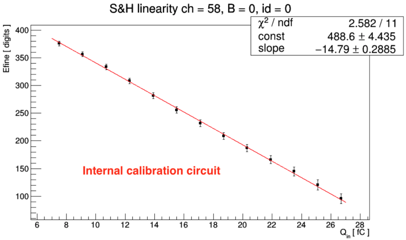


Charge Measurement - ongoing

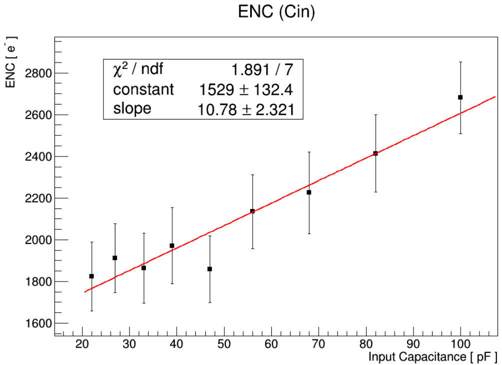
- Charge Measurement with a **Sample-and-Hold circuit** or Time-ove-threshold (single/dual Vth)
- Calibration of dynamic range with external test-pulse generator (managed by test DAQ SW)
- Back-annotation to generate a parameter space for the internal calibration circuit
- Charge measurement below 5 fC a problem with single-threshold - Next: work on double-threshold operation
- Still, Fast Branch noise higher than expected







- Threshold scan (N meas/point, typ 50) for a fixed internal calibration circuit TP
- Normalise efficiency and fit with sigmoid for noise evaluation
- Repeat M times (typ 100)
- Plot noise and std deviation of measurement
- Sweep input capacitance and repeat measurement
  - ↪ ENC @ Cin 100 pF ≈ 2500 e-
  - ↪ expecting 1700 e- from post-layout simulations at T=40C
  - PSRR, interference and grounding: under study

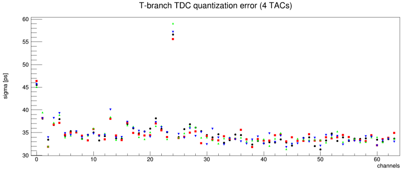


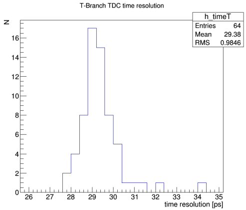
TDC Performance

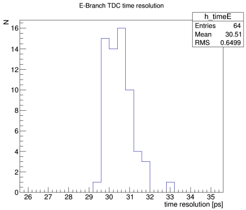
- Dual-branch TDC scanned over dynamic range (sweep TP phase)
- Create LUT with gain and offset correction for all channels

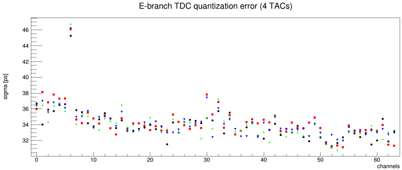
↪ Average TDC quantization error after calibration $\approx$ 30 ps r.m.s.

- Re-use method with TP injected to front-end to quantify intrinsic jitter - tbd









FEB Design for the on-detector electronics

Contact person: Marco Mignone - INFN Torino

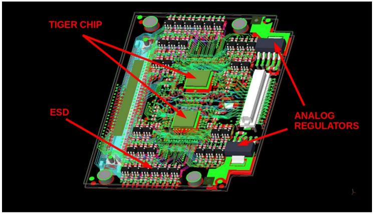
L3

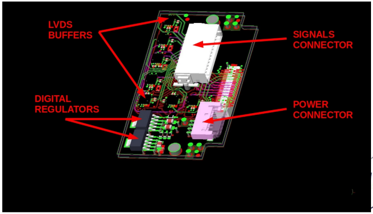
- Board FE1 (56x40mm)
  - 2 ASICs, biasing and references, filtering
  - ESD protection network for 122 channels
  - 2 Analogue domain power regulators
  - connector towards anode
  - connector towards FE2
  - ↪ Routing done, waiting confirmation on anode connector
- Board FE2 (56x30mm)
  - 2 Digital domain power regulators
  - 7 LVDS Buffers
  - connector towards FE1: power, signalling
  - ↪ Routing done

L1-L2

- Board FE1 (56x52.8mm)
- Board FE2 (56x67mm)

↪ Layout to be started, relaxed clones of L3

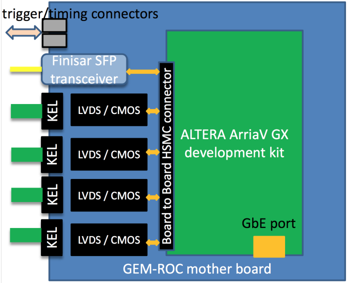


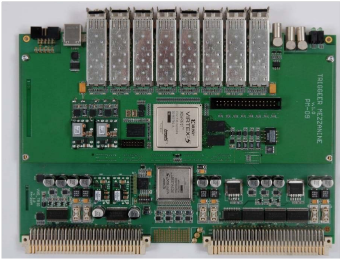


Off-detector electronics overview

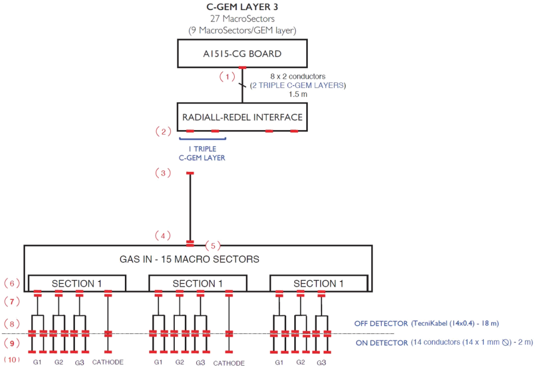
[ROC] A Cotta Ramusino (INFN Ferrara), [ATLB] Pawel Marciniewski (Uppsala Universitet)

- Each of the 20 Read-Out Cards (ROC) handles 4 ASIC PCBs (8 ASICs)
- Prototype is based on an ALTERA e-kit (ArriaVGX FPGA), coupling to motherboard through HSMC high performance connector
- Motherboard provides electrical and physical interfaces to the ASIC carrier PCBs, to the data concentrator (bi-directional fibre optic links) and the BES-III Fast Control system. Ethernet port also available for monitoring and debugging.
- 2 Advanced Trigger Logic Board (ATLB) Data Concentrators manages interface with VME based BESIII DAQ system





Contact person: Giulietto Felici - INFN LNF



CGEM LAYER	MACRO SECTORS	MICRO SECTORS	MICRO-SECTORS CAPACITANCE (nF)
1	12	120	4.6 nF
2	24	240	4.3 nF
3	36	360	4.5 nF

- each triple CGEM requires 7 voltages (range: 0-5 kV)
- each CGEM voltage must be distributed to many macro/micro sectors to reduce the section capacitance and the energy released in case of discharge
- the system allows to monitor the current dragged by each CGEM foil (nA sensitivity)
- the system allows to disconnect a single micro-sector in case of local short to minimise the system dead-zone

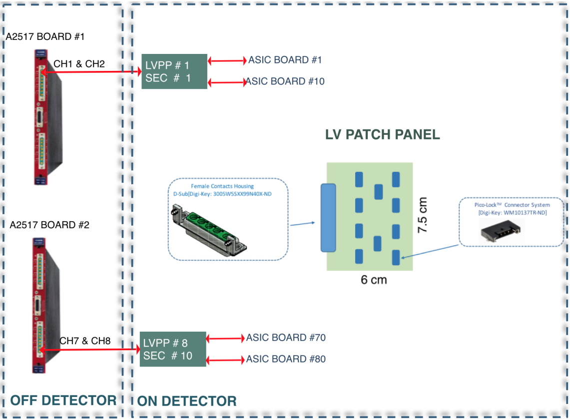
Contact person: Giulietto Felici - INFN LNF

INNER TRACKER ON DETECTOR LV REQUIREMENTS

BOARD VOLTAGE CURRENT REQUIREMENTS

1.2 V	1.4 A	ASIC analog section
2.5 V	0.4 A	ASIC digital section+ LVDS buffers
REGULATOR VOLTAGE DROP		0.5 V

LAYER	BOARDS (x side)	I [1.2V] A	I [2.5 V] A	PD [REG] W	PD [BOARD] W
1	8	11,2	3,2	7,2	21,4
2	14	19,6	5,6	12,6	37,5
3	18	25,2	7,2	16,2	48,24
TOT	40	56	16	36,0	107,2
				143,2	



- CGEM not be accessible after its insertion into the BESIII apparatus

↪ tracker services (i.e. HV and LV generation and distribution) designed with reliability as primary goal

Outlook

On-detector FEB Design

- ✓ on-schedule, space/volume criticality of L3 design overcame

Status of Readout ASIC

- ✓ Time-based readout working properly
- ✓ Charge measurement with S/H ok
- → BLH temperature/VDD sensitivity minor revision ongoing, corrected for engineering version
- → Noise and grounding sensitivity under study
- ✓ Organising SEU, TID beam tests
- ✓ First tests with planar and cylindrical GEMs in March
- ✓ Engineering run during 2017, minor fixes and design flavours

Off-detector Electronics

- ✓ First smoke tests with TIGER ongoing - data reconstruction from test-pulses

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Thank You!

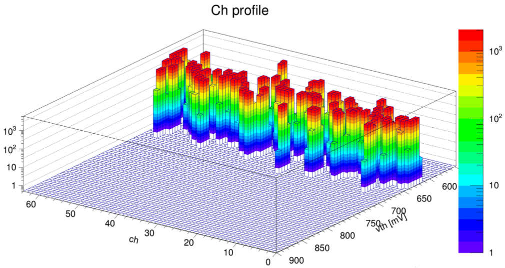
HORIZON 2020 European Commission

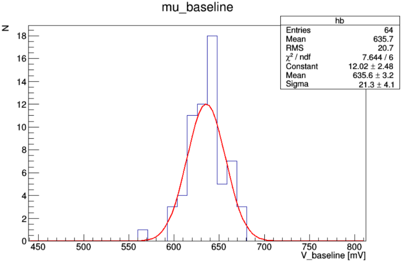
The BESIIICGEM project has been funded by European Commission within the call H2020-MSCA-RISE-2014.

Backup Slides

- Threshold scan on all channels, for T1 only (single-threshold mode)
- Baseline saved at 50% level of the sigmoid

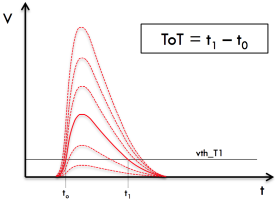
✓ below 25 mV r.m.s. dispersion



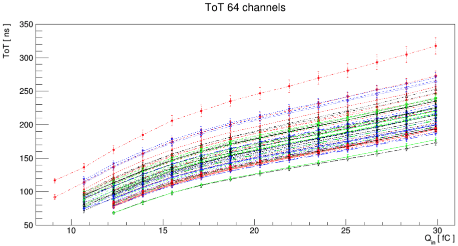


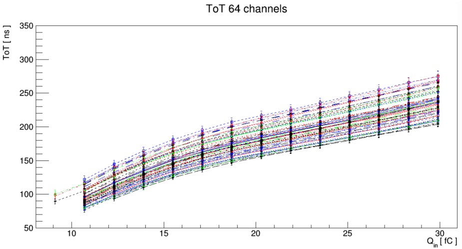
Threshold equalisation

- A 64-channel baseline scan is performed on every chip
- Threshold scan results are saved on a LUT
- The same effective threshold is set for all channels during acquisition



↪ example of a ToT charge measurement before (below, left) and after (below, right) the equalisation.





TDC/ADC - simulation of one event