Characterization of novel prototypes of monolithic HV-CMOS pixel detectors for high energy physics experiments

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In collaboration with University of Geneva

UNIVERSITÉ DE GENÈVE

FACULTÉ DES SCIENCES

INSTR17: Instrumentation for Colliding Beam Physics

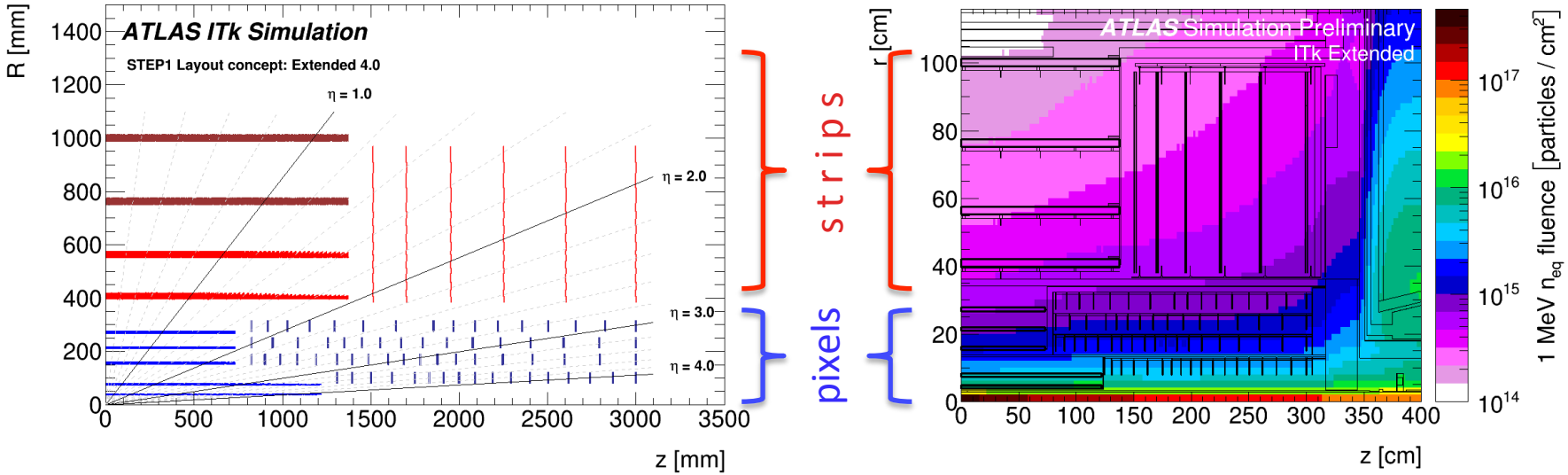
Novosibirsk, 27th February 2017

Outline

- Introduction
  - The new Inner Tracker (ITk) for ATLAS phase II upgrade at HL-LHC
  - HV-CMOS Depleted MAPS for the ITk
- The H35 large area demonstrator chip
  - Sensor characterization with Edge-TCT
  - Monolithic matrix readout at IFAE
  - Very first test beam measurement of the CMOS monolithic matrix
- Conclusions and outlook

The ITk upgrade for HL-LHC

Replace the whole ATLAS Inner Detector with a new full-silicon Inner Tracker (ITk)



- New layout with 5 pixel barrel layers & large η coverage (extended − inclined designs)
- Sensor technologies under investigation:
  - Outer pixel layers (large area to cover)
    - HR/HV-CMOS pixel detectors
    - n-in-p planar silicon sensors (150 µm thick)
  - Inner pixel layers
    - Thin n-in-p planar silicon sensors (100 µm thick)
    - 3D silicon sensors (already in IBL and AFP)

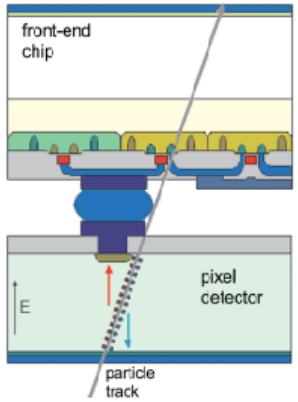
From 1e15 $n_{eq}cm^{-2}$…

…up to 2.2e16 $n_{eq}cm^{-2}$

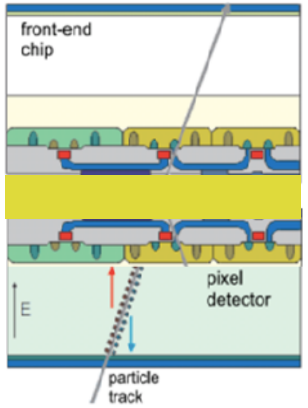
…see "The Phase II ATLAS ITk Pixel Upgrade" poster (board 16)

Possible CMOS devices

- Depleted Si sensors produced in High Resistivity/High Voltage CMOS technology
  - Charge generated in a small depleted region
  - Industrial CMOS process
    ➔ potentially cheaper to cover large areas (full ITk pixels ~14 m^2)

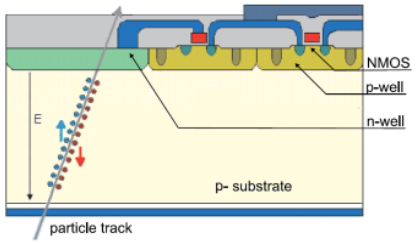


- Investigating the possibility of a 5th pixel layer of CMOS for ITk:
  - Hybrid passive pixel detectors:
    - Industrial CMOS process potentially cheaper
    - Standard interconnection to Front End chips



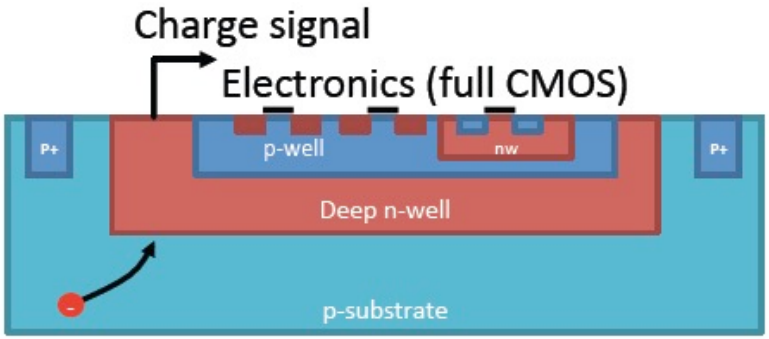
  - Hybrid Active Capacitive Coupled Pixel Detectors (CCPDs):
    - Active: in pixel amplification
    - Glue interconnection ➔ reduced costs wrt. bump bonding
    - Already proven radiation hardness:
      M. Benoit et al., arXiv:1611.02669

  - Fully Monolithic Active Pixel Sensors (MAPS):
    - On chip discriminator and digital electronics
    - No interconnection costs
    - Reduced material

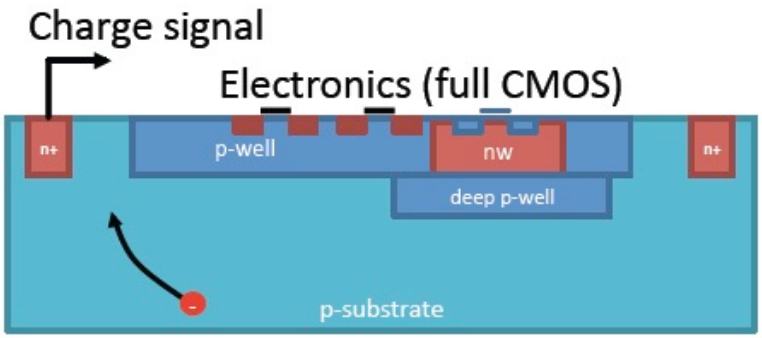


HV-CMOS Depleted MAPS

Two different philosophies:



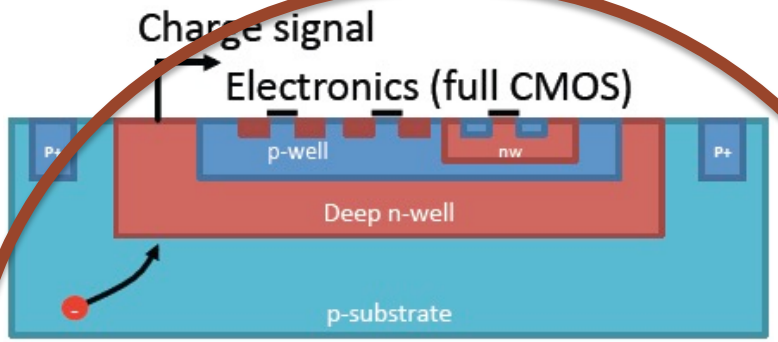
- Electronics **inside** the n-well
  - Large fill factor: isolation of p-well inside a deep n-well
    ➔ Large sensor capacitance (~100 fF)
  - More uniform electric field
  - Shorter drift distance
    ➔ Radiation hardness



- Electronics **outside** the n-well
  - Small fill factor
    ➔ Very small sensor capacitance (~5 fF)
  - Low electric field regions
  - Longer drift distance
    ➔ Radiation hard??

HV-CMOS Depleted MAPS

Two different philosophies:



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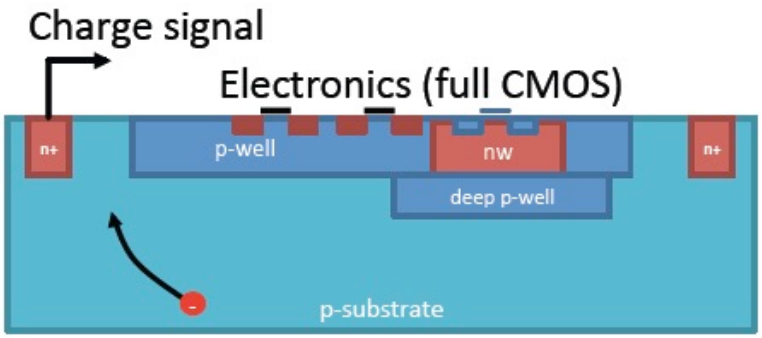

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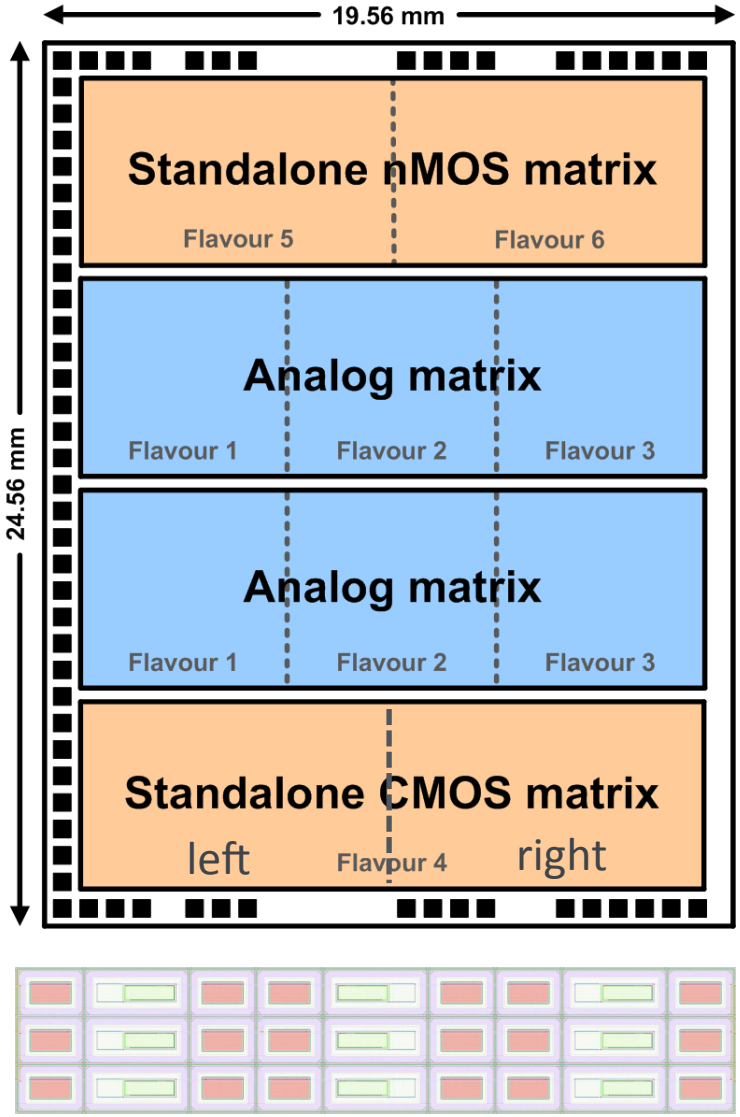
Design characterized in this presentation

The H35 Demonstrator

AMS 350 nm High Voltage CMOS: different ρ: 20–80–200–1000 Ωcm



Designed by KIT, IFAE and Univ. of Liverpool

- Monolithic nMOS matrix:
  - Digital pixels with in-pixel nMOS comparator
  - Two flavors: with and without Time Walk compensation
- Analog matrices (2 arrays):
  - Different flavors in terms of gain and speed
  - To be Capacitive Coupled (CC) to FE-I4 readout chips (pitch 50x250 μm^2)
- Monolithic CMOS matrix:
  - Analog pixels with off-pixel CMOS comparator
    - One comparator in the left sub-matrix
    - Two comparators in the right sub-matrix

\+ test structures without electronics for Transient Current Technique (TCT) studies

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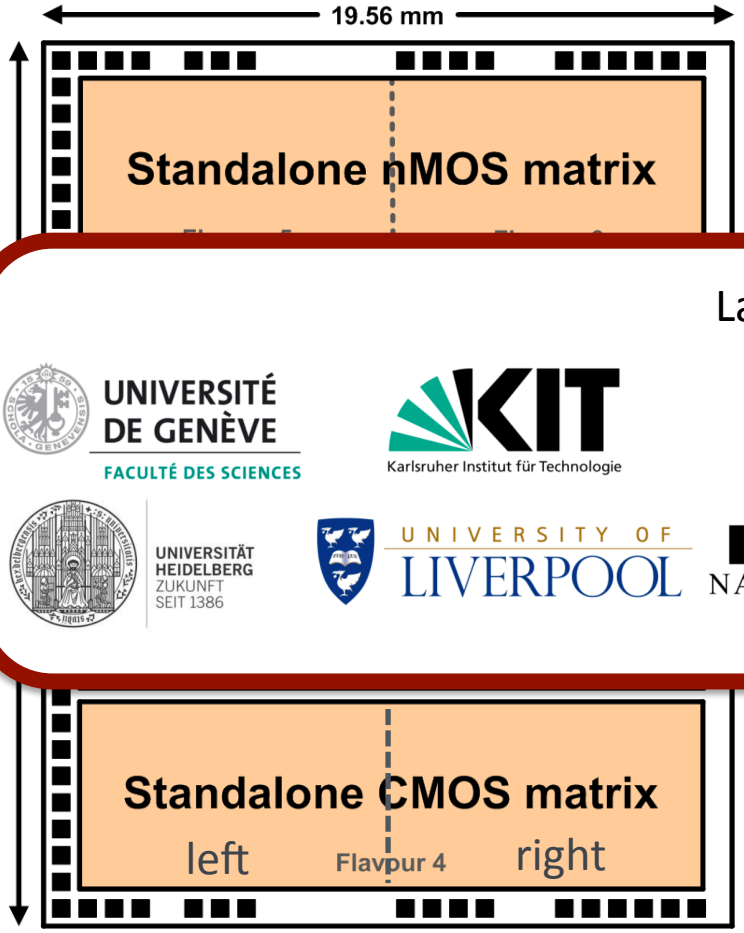

Designed by KIT, IFAE and Univ. of Liverpool

- Monolithic nMOS matrix:
  - Digital pixels with in-pixel nMOS

Large collaboration

UNIVERSITÉ DE GENÈVE – FACULTÉ DES SCIENCES
KIT Karlsruher Institut für Technologie
IFAE
u^b UNIVERSITÄT BERN – AEC ALBERT EINSTEIN CENTER FOR FUNDAMENTAL PHYSICS
筑波大学 University of Tsukuba
UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386
UNIVERSITY OF LIVERPOOL
BROOKHAVEN NATIONAL LABORATORY
CERN

- Monolithic CMOS matrix:
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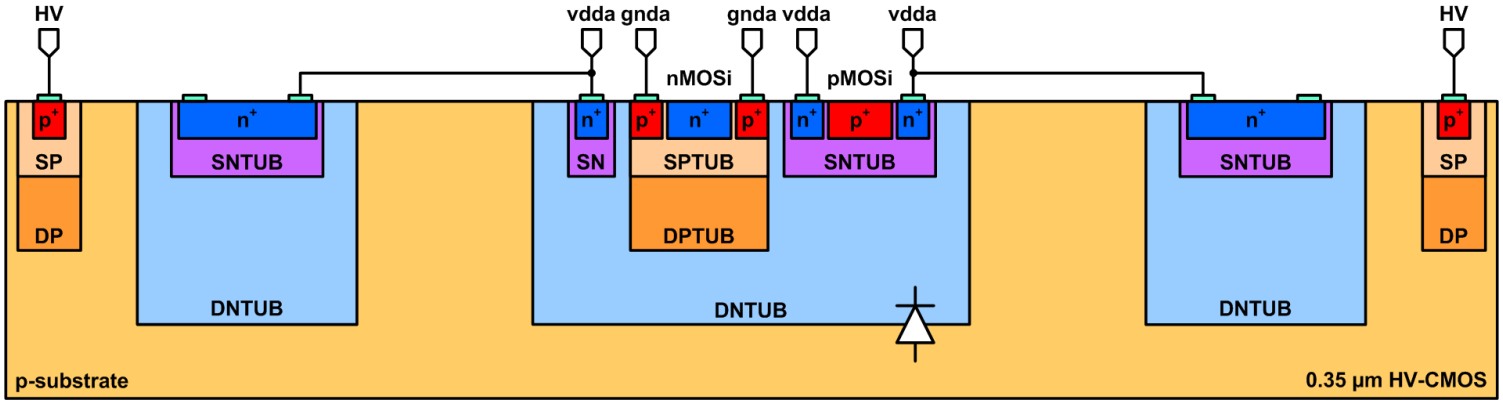
The H35 pixel structure



- Pixel size: 50x250 µm^2

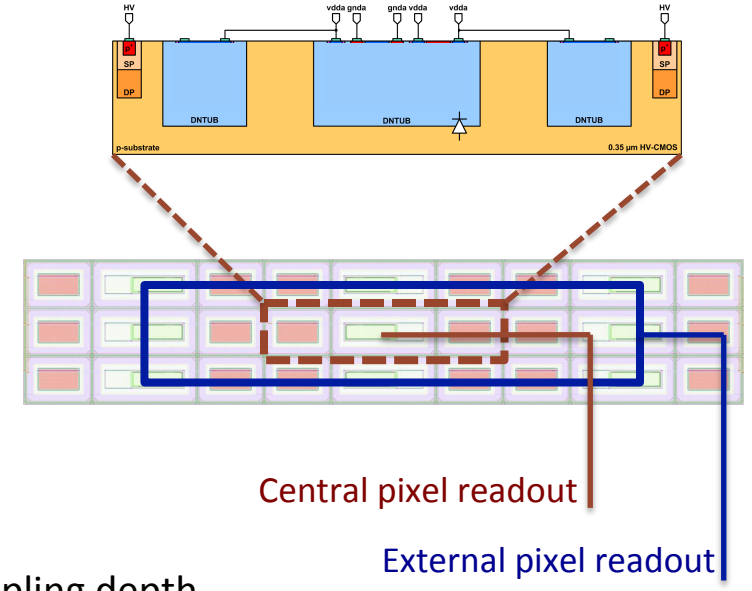
- Large fill factor: nMOS and pMOS transistors embedded in the same deep n-wells acting as collecting electrodes
  - p-substrate + 3 separate deep n-wells* to reduce the capacitance
    ➔ less noise, better timing - power consumption
  - Short charge drift ➔ reduced trapping after irradiation
  - More uniform electric field

- Bias voltage applied from the top
  - Single side processing
  - Bias voltage > 100 V

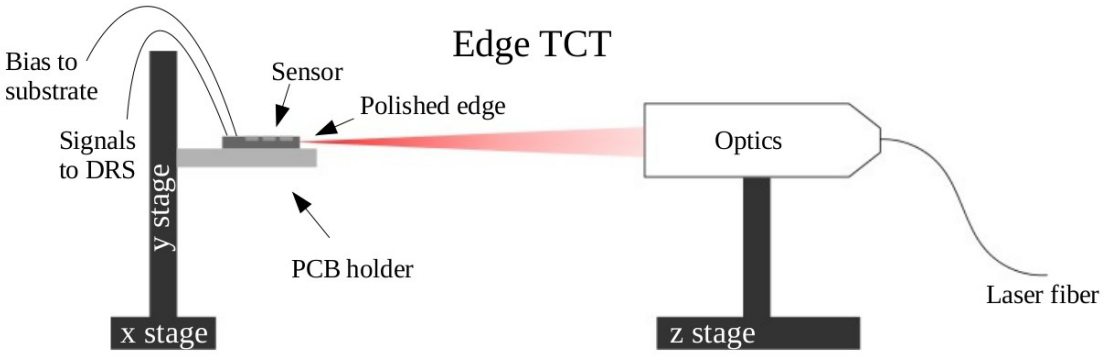
*all matrices but monolithic nMOS

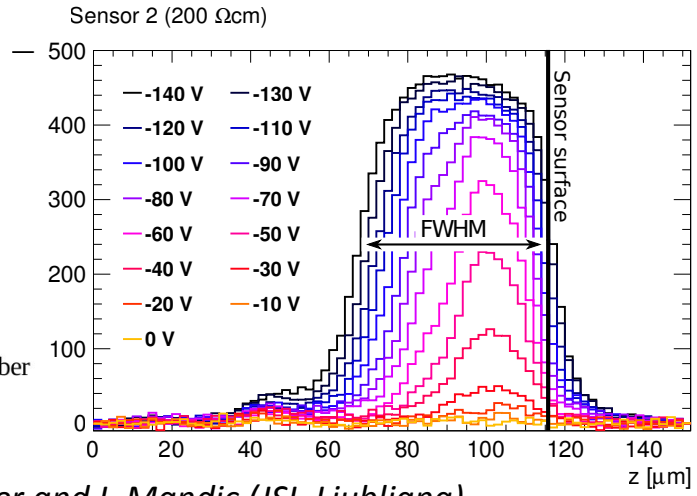
Sensor characterization

- Characterization of H35 test structures:
  - 3x3 pixel structures w/o electronics
  - External pixels shorted together
  - Separate readout of the central pixel



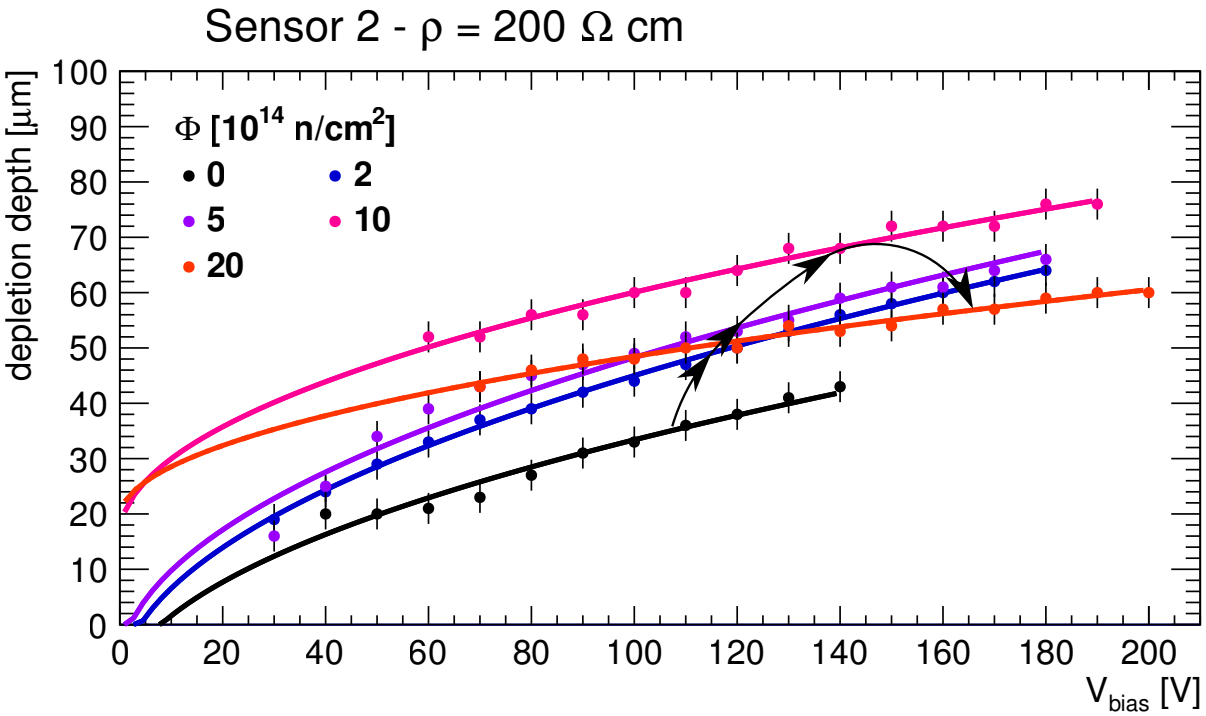
- The Edge-TCT setup:
  - Infra-red laser (1064 nm)
    - Beam spot about 10 µm FWHM
    - Pulses of about 500 ps
  - Readout: DRS4 evaluation board
    - 700 MHz bandwidth, 5 GSPS, 200 ns sampling depth
  - Illumination from the edge to study the depletion depth
    - FWHM of the charge collection profile of the central pixel is taken as measure of the depletion depth





TCT measurements and irradiations in collaboration with G. Kramberger and I. Mandic (JSI, Ljubljana)

Depletion depth



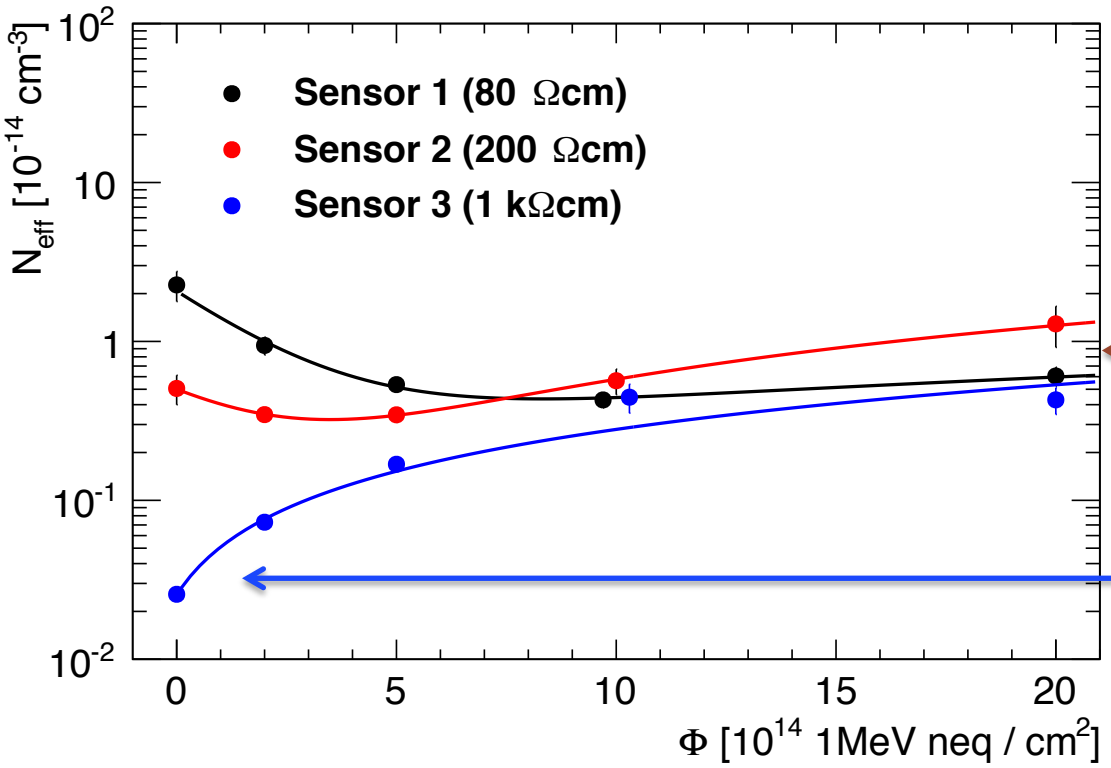
- Edge-TCT measurements on 200 Ωcm test structures:
  - Irradiated with reactor neutron at JSI (Ljubljana) up to 2e15 $n_{eq}cm^2$
  - Increase of the depletion depth with irradiations up to 1e15 $n_{eq}cm^2$
    - ➔ initial acceptor removal effect

Effective doping concentration

- Effective doping concentration obtained from:

$$d(V) = d_0 + \alpha\sqrt{\rho V} = d_0 + \sqrt{\frac{2\varepsilon\varepsilon_0}{eN_{eff}}V}$$

$$N_{eff} = \underbrace{N_{eff0}}_{\text{Initial doping}} - \underbrace{N_c \cdot (1 - exp(-c \cdot \Phi_{eq}))}_{\text{Acceptor removal}} + \underbrace{g_c \cdot \Phi_{eq}}_{\text{Acceptor introduction}}$$



After about 1e15 n_{eq}/cm^2 N_{eff} tends to the similar values for all resistivities

Initial acceptor removal effect negligible for higher resistivity at these fluences

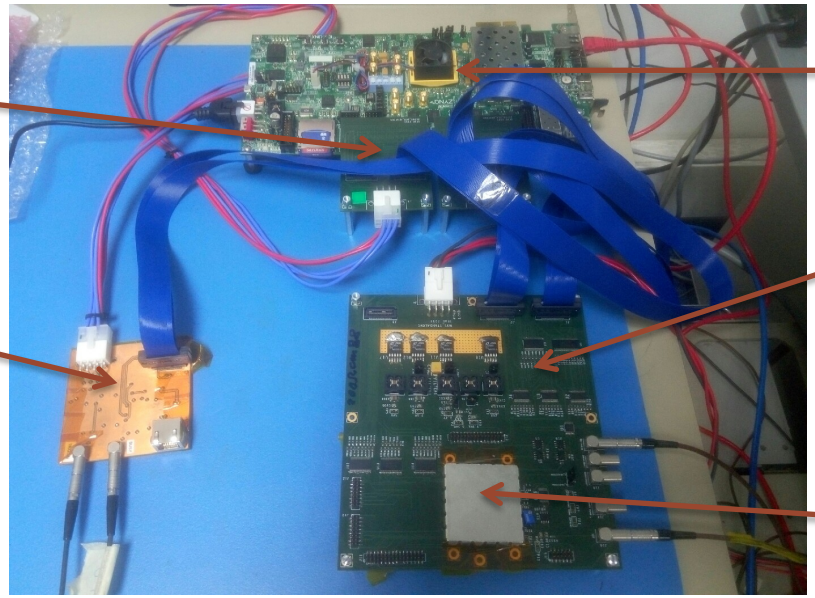
Results published in E. Cavallaro et al., JINST12, (2017) C01074

Monolithic matrix readout at IFAE

Adapter PCBs
- 1x H35 PCB
- 1x test signals
- 1x trigger board

Trigger board
- Trigger in
- Busy out
- RJ45

External pulse generator



Xilinx ZC706 FPGA board

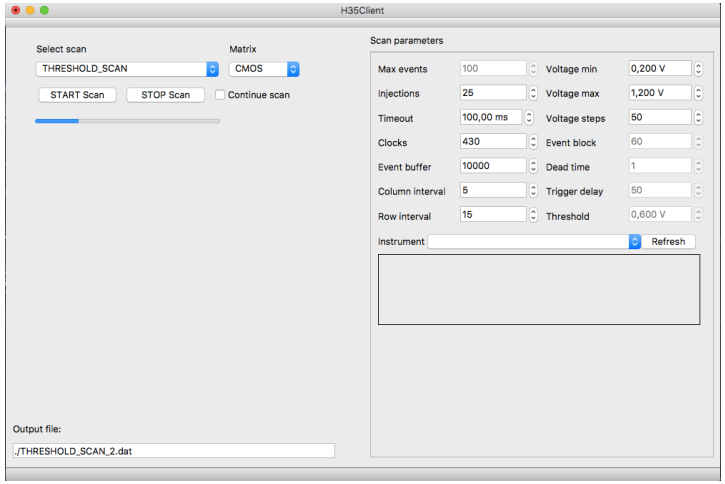
H35demo PCB
- External voltage regulators
- Sensor bias input
- Injection pulse input
- Analog signal output

H35demo chip
- Both CMOS and nMOS matrices wire-bonded

PCBs, FPGA firmware and steering software developed at IFAE

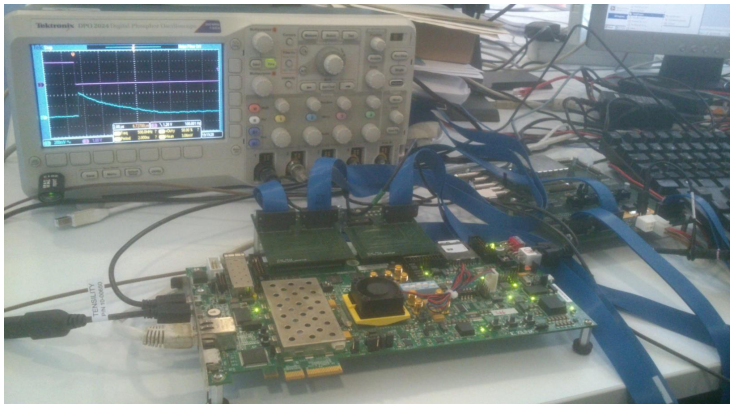
- Software with interactive GUI
  - Steering FPGA and pulse generator
  - Tuning of the DAC registers
  - Data taking and operations

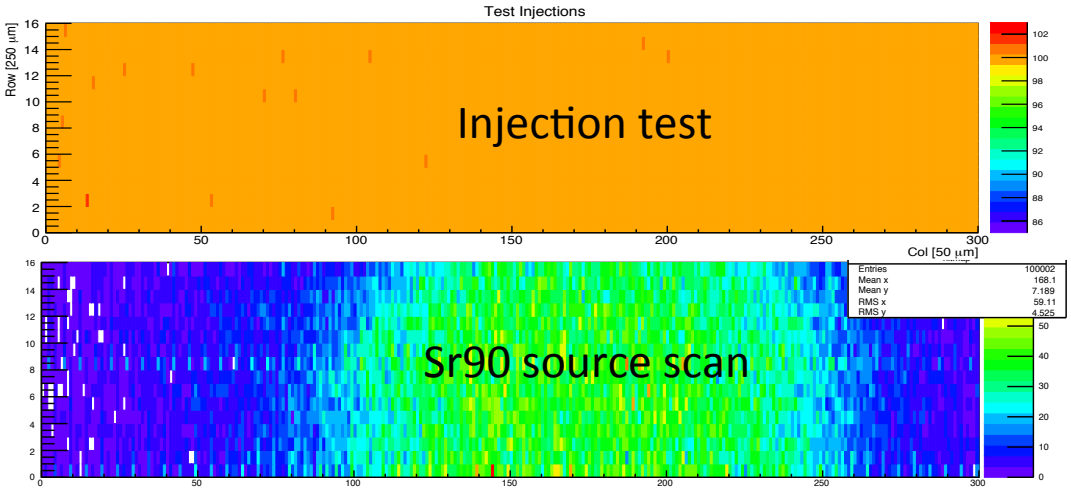
- Chip and FPGA operated at 320 MHz
  - 1 event = 25 ns (col, row, time stamp)



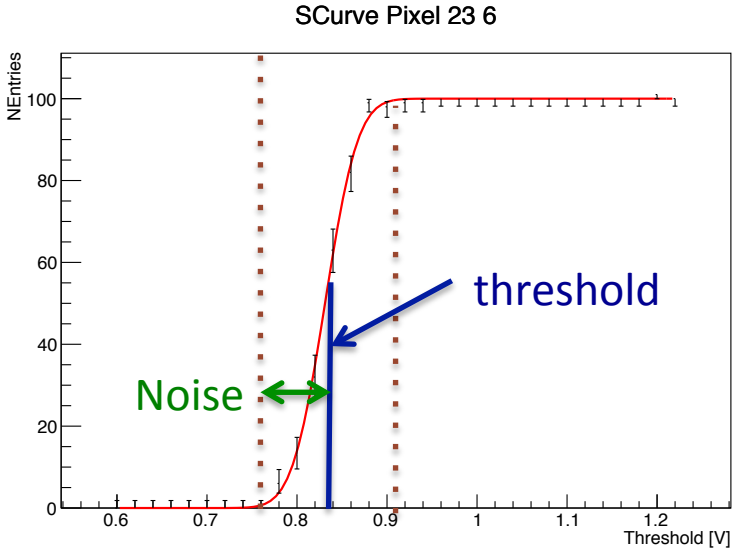
CMOS matrix readout and tests

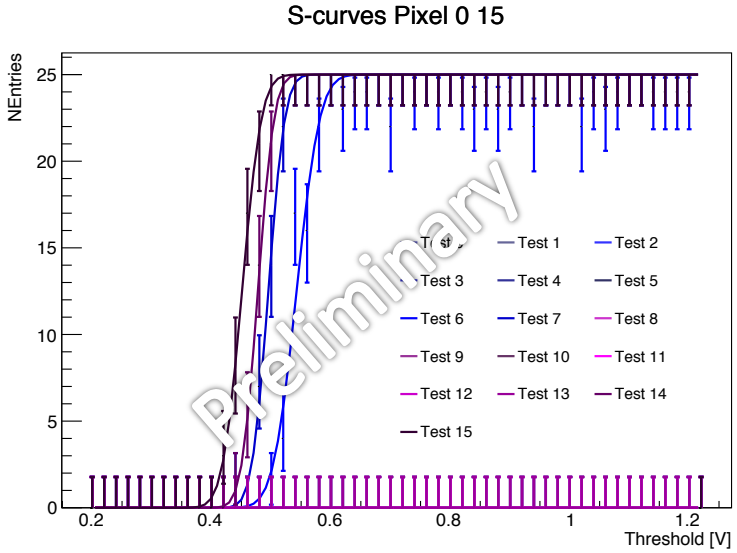
Test pulse injection and Sr-90 source scans





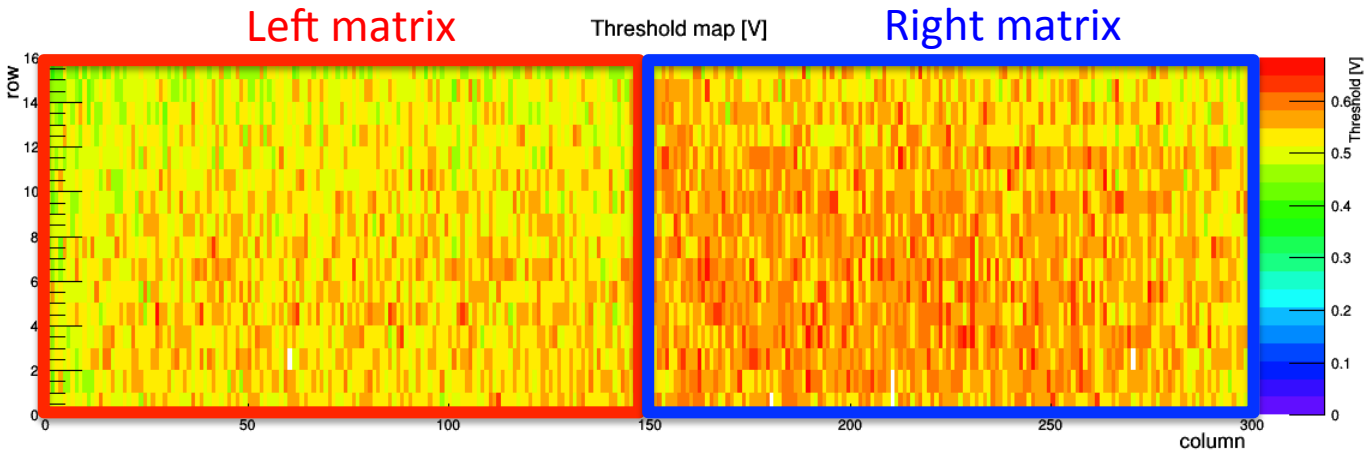
Threshold measurement and first fine tuning algorithm implemented

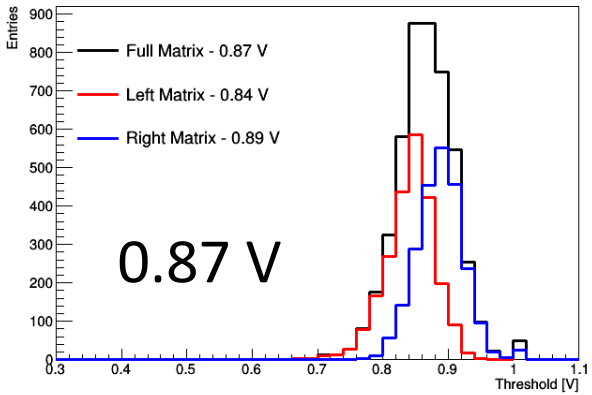


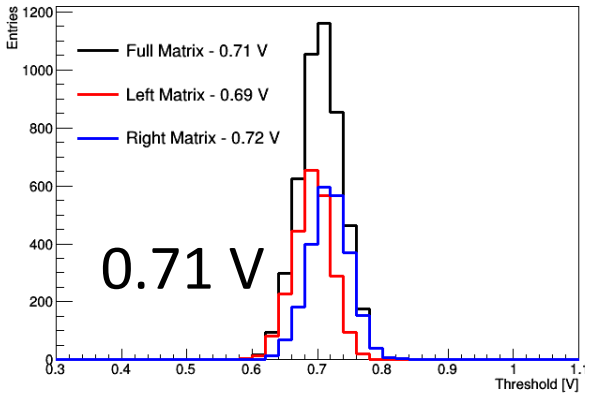


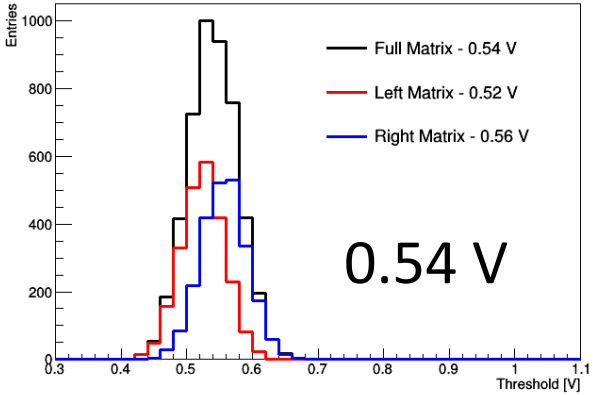
CMOS matrix: threshold tuning

- Three different global tunings of the threshold:
  - The chip is tuned just with the global registers fine tuning was still not implemented
  - Input pulse amplitude: 0.54 V – 0.7 V – 0.87 V
  - Average threshold in the right matrix is always higher than in the left matrix









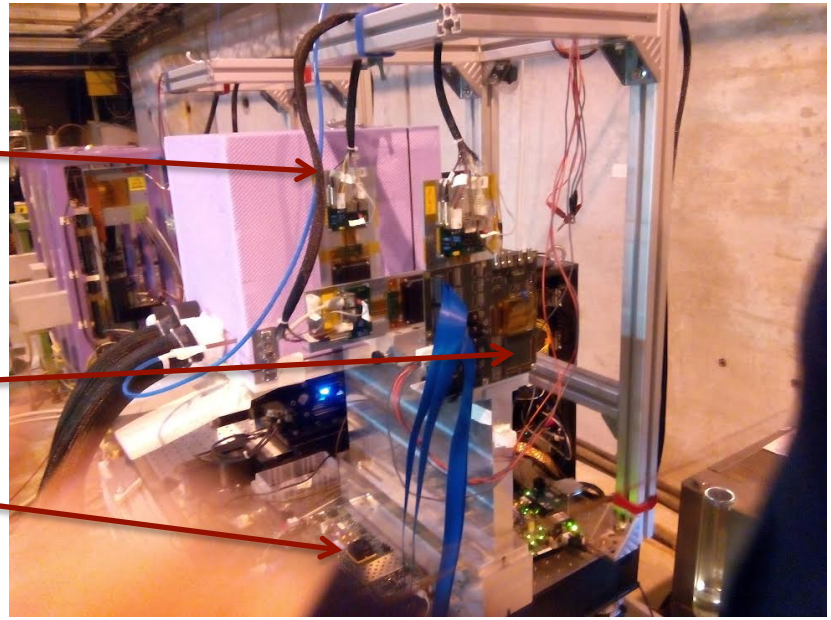
Test beam setup at CERN SpS

UniGe FE-I4 Telescope*
- 6 ATLAS FE-I4 planes (pitch: 50x250 μm^2)
- 2 planes rotated 90 degrees to increase resolution in Y
- RCE readout system**

H35demo PCB
- CMOS matrix aligned in the beam

IFAE Readout system

180 GeV π beam



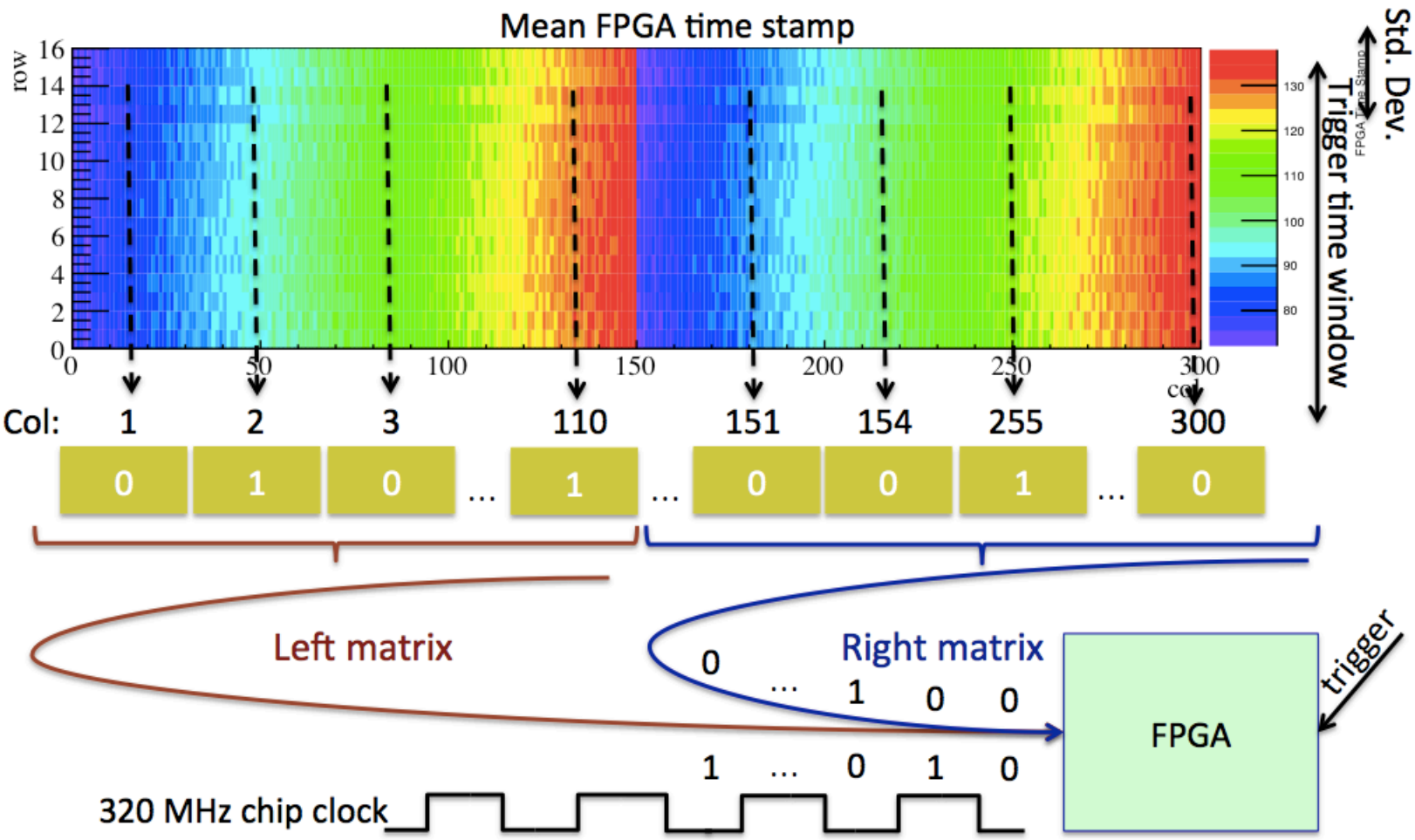
- Integration with the UniGe FE-I4 telescope (trigger−busy scheme)
  - Triggers from the telescope (RCE − HSIO based) reach the Xilinx FPGA board
  - Busy signal from the FPGA stops telescope DAQ until the H35 chip is ready
  - Triggers (events) are written sequentially by the separate DAQs
  - System running at 25 ns with >2 kHz trigger rate

  - Re-synchronization of the data based on the trigger time stamp difference
  - Track reconstruction and analysis with the Judith software

In collaboration with University of Geneva (UniGe)

*DOI: 10.1088/1748-0221/11/07/P07003
**DOI: 10.1109/NSSMIC.2014.7431254

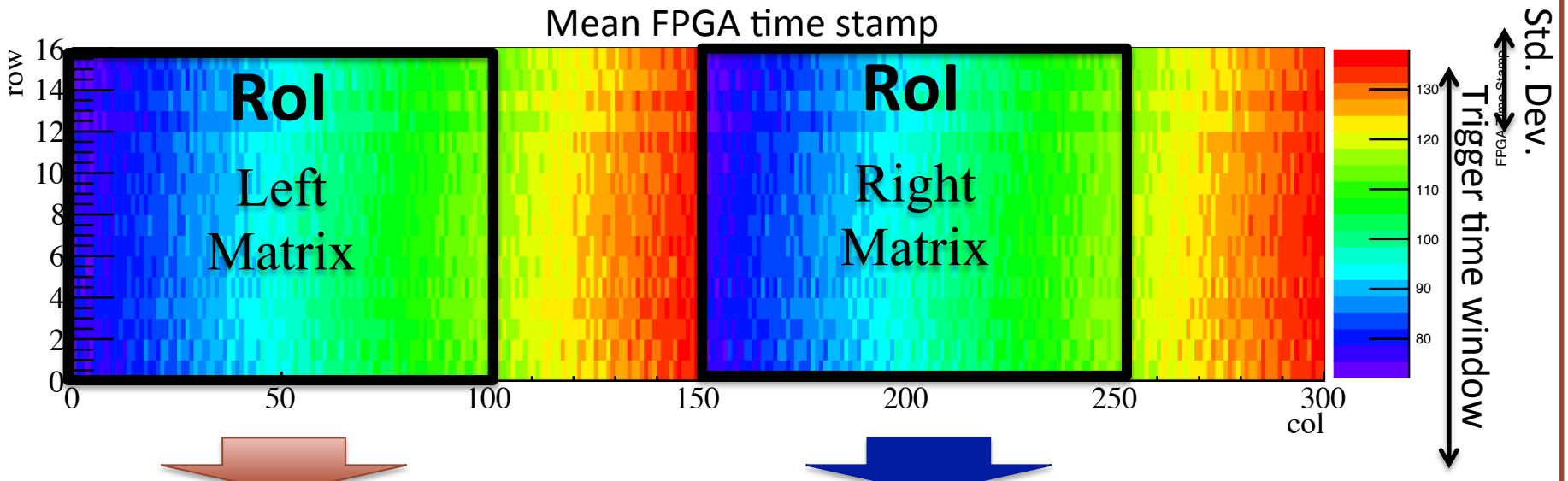
Readout and trigger



- Column drain architecture with priority encoding (same as ATLAS FE-I3 chip)
- Limitations of the H35 demonstrator chip
  - Un-triggered readout → trigger logic implemented in the FPGA
  - No zero suppression → also performed at the FPGA level

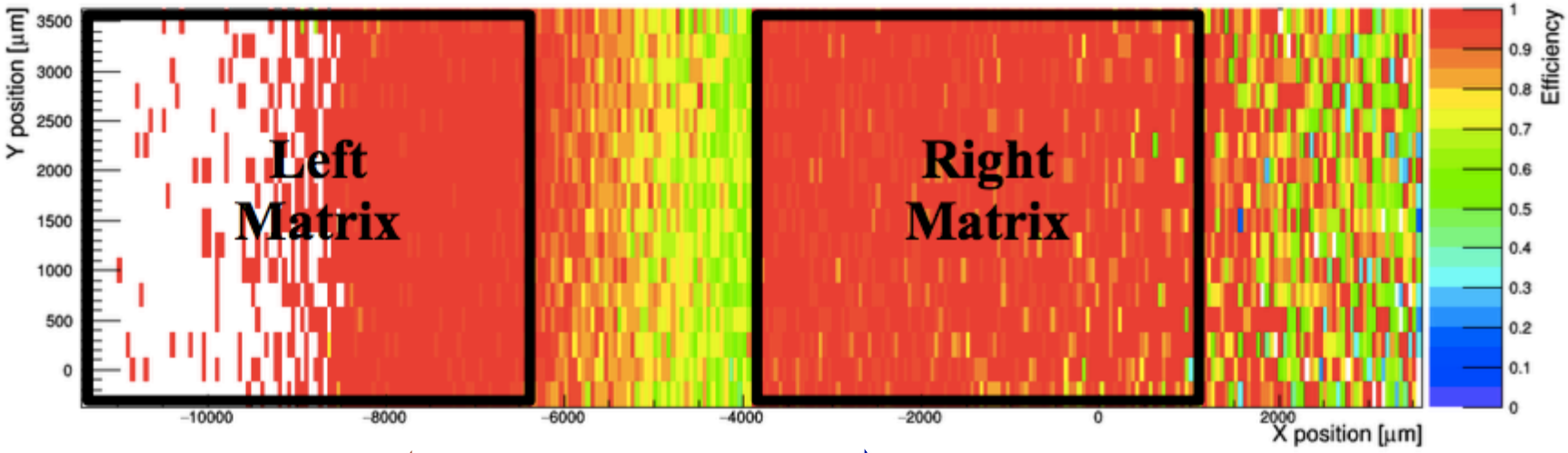
} Long readout time (>1 µs)

Region of Interest (RoI)



Threshold 0.54 V, V_{bias} = 120 V

Efficiency map: CMOS matrix - 200 Ωcm



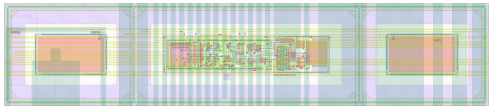
98.1% ⇦ Efficiency in the RoI ⇨ **96.3%**

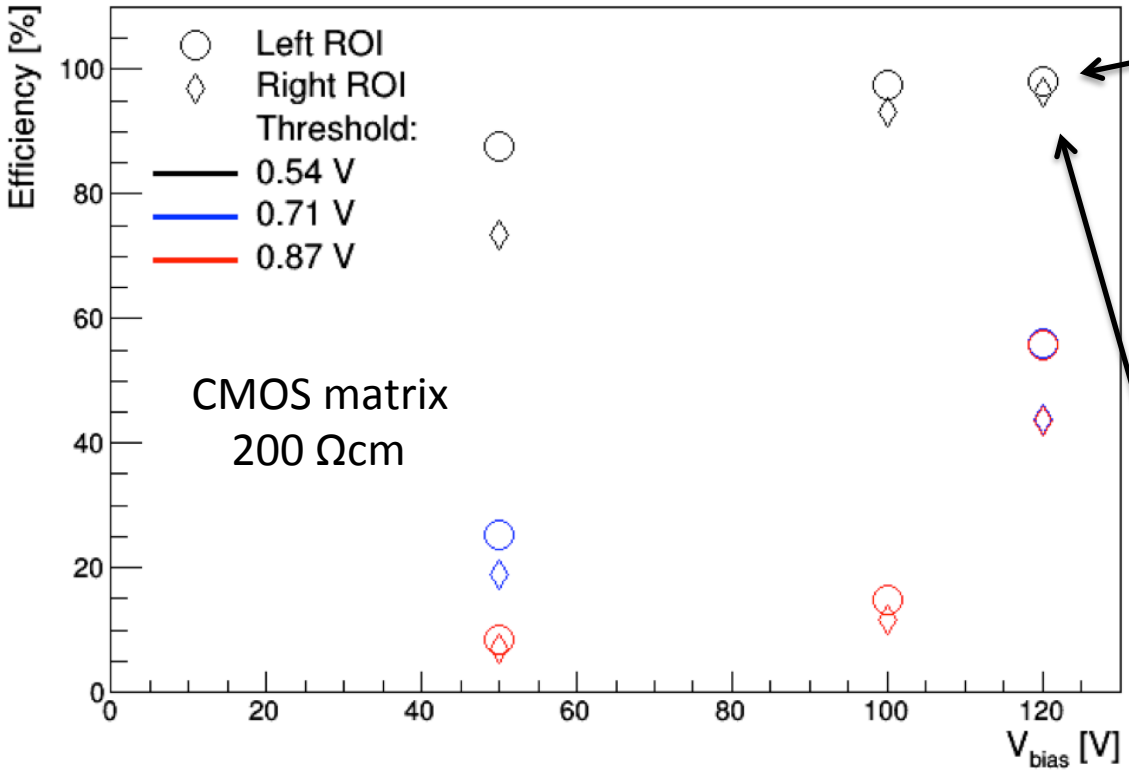
Hit efficiency summary

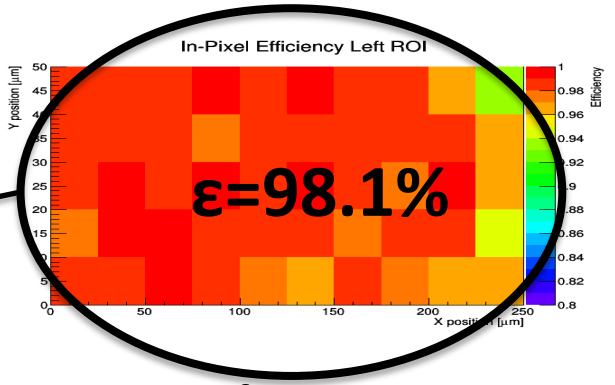
- Efficiency saturation depends on the threshold
  - Higher threshold requires more bias
    ➔ increase the depletion depth

- Higher efficiency in the left matrix
  - Mean threshold right > mean threshold left
  - Right matrix: efficiency lost close to pixel edges

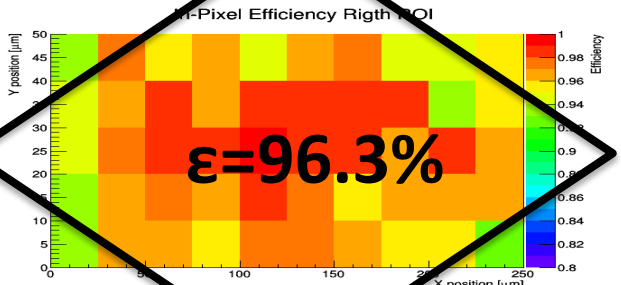
In-pixel efficiency maps
at 120 V and thr: 0.54 V







Left matrix



Right matrix

Conclusions & outlook

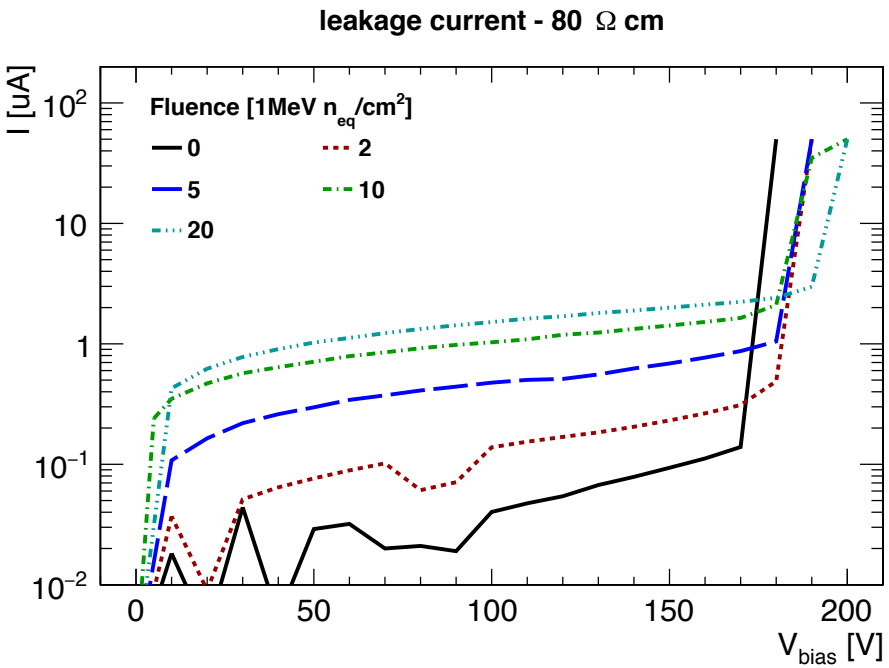
- Characterization of the H35Demo chip at IFAE
  - Edge-TCT measurements of irradiated sensor test structures
    - ➢ Acceptor removal effect observed for low resistivity after irradiation
  - New readout system developed for the H35Demo monolithic matrices
    - ➢ Tuning and readout at 320 MHz clock (25 ns events)

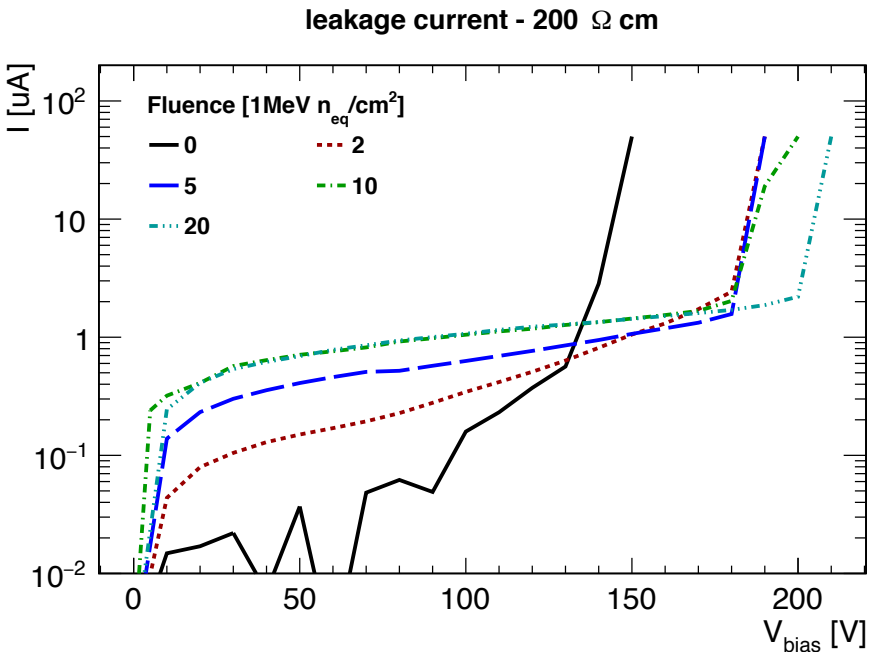
- Very first time of the H35 monolithic CMOS matrix in a test beam
  - New readout system developed at IFAE + Geneva FE-I4 telescope at CERN SpS
  - Measured hit efficiency for 200 Ωcm samples before irradiation
    up to 98% at 120 V even with a partially tuned chip

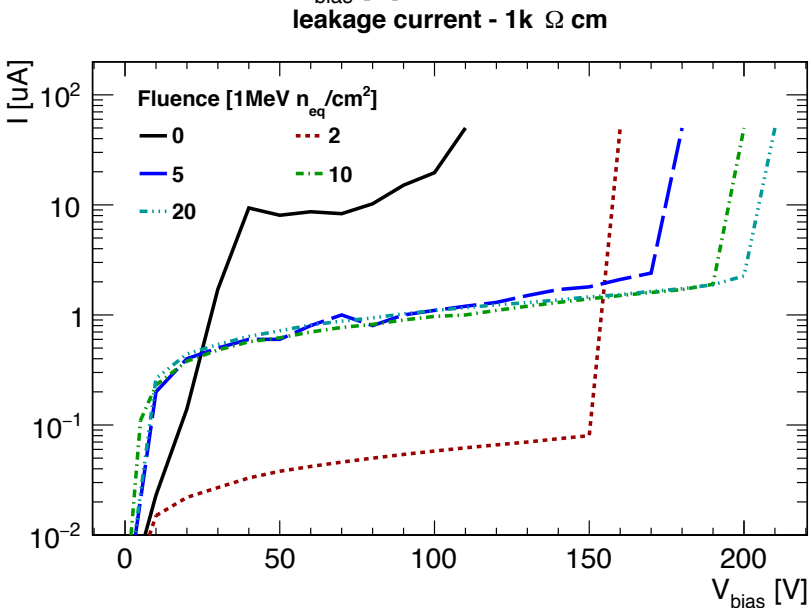
- What's next:
  - 200 Ωcm sensors sent for irradiation up to the HL-LHC fluences expected for the fifth pixel layer of ATLAS ITk
    - In Ljubljana with neutrons: from 2 to 20e14 $n_{eq}cm^{-2}$
    - At KIT with protons: 1 and 10e14 $n_{eq}cm^{-2}$
  - New test beam at Fermilab in April this year
    - Irradiated samples & un-irradiated with different resistivities (20−80−200−100 Ωcm)
    - Readout system improved: no re-synch needed, larger trigger window, better tuning with low thresholds

Backup slides

Test structure IV curves





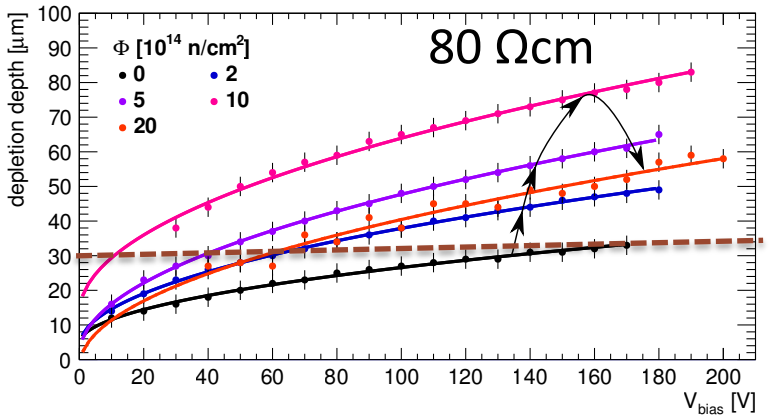


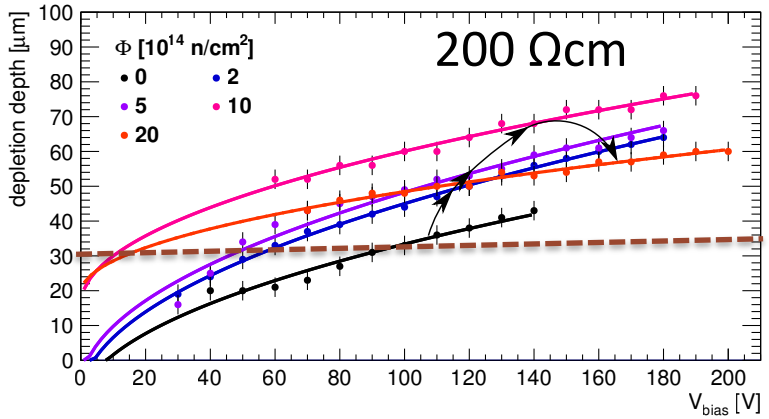
Depletion: after irradiation

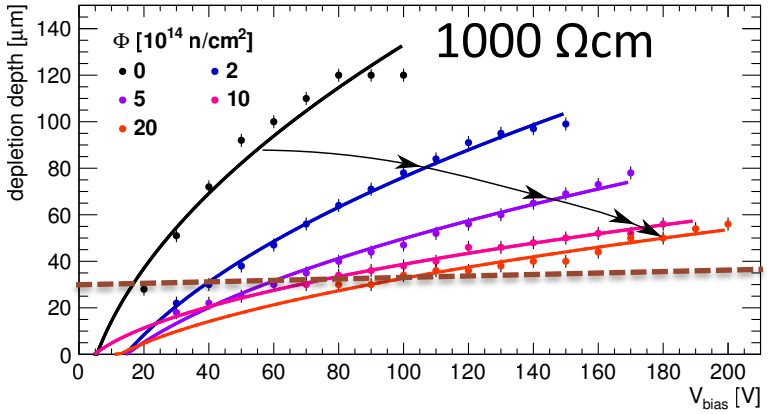
- Irradiation at the TRIGA neutron reactor at JSI, Ljubljana:
  - Now: **2e14, 5e14, 10e14, 20e14** $n_{eq}cm^{-2}$
  - Next steps: 5e15 and 1e16 $n_{eq}cm^{-2}$

- Acceptor removal effect visible for lower substrate resistivities which leads to an increase of the depletion depth after irradiation up to 2e15 $n_{eq}cm^{-2}$

- Due to the low initial acceptor concentration in the 1000 Ωcm sample the creation of stable acceptors dominates and the depletion depth decreases after irradiation

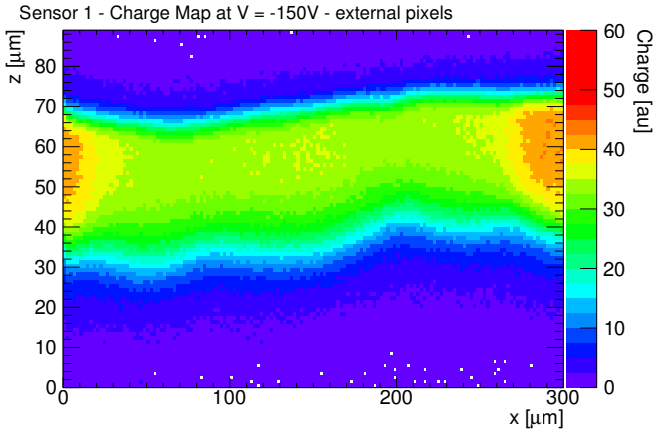


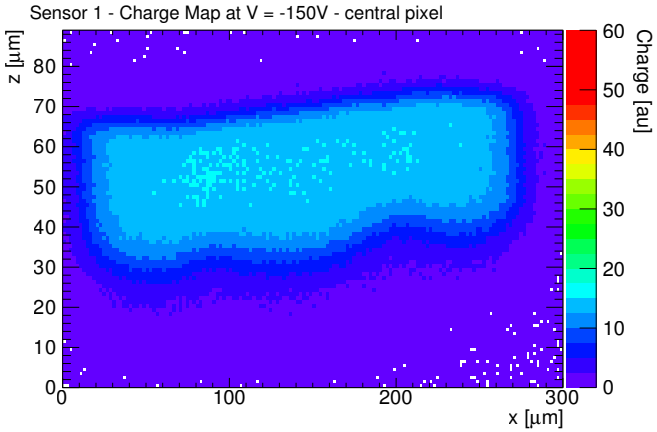


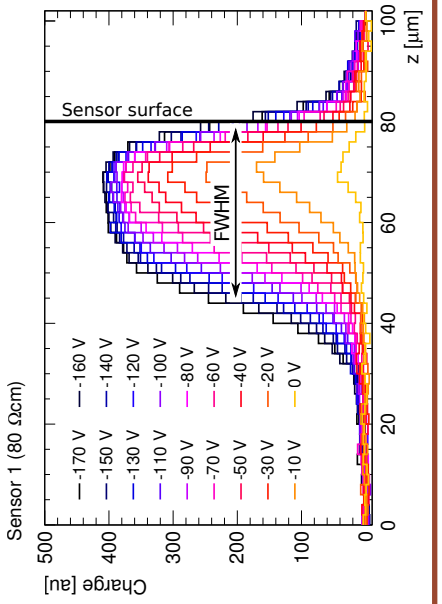


Depletion: before irradiation

80 Ωcm



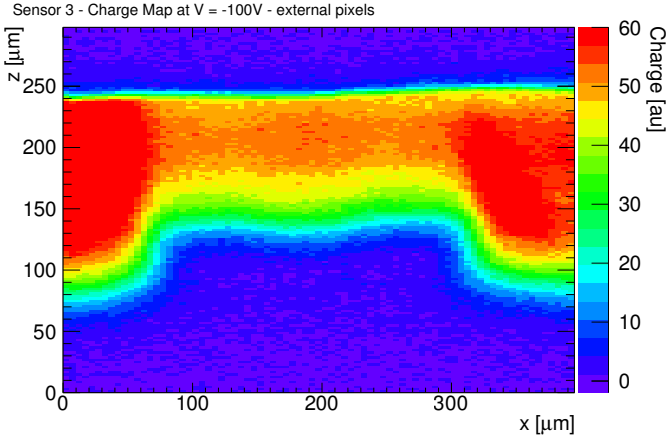


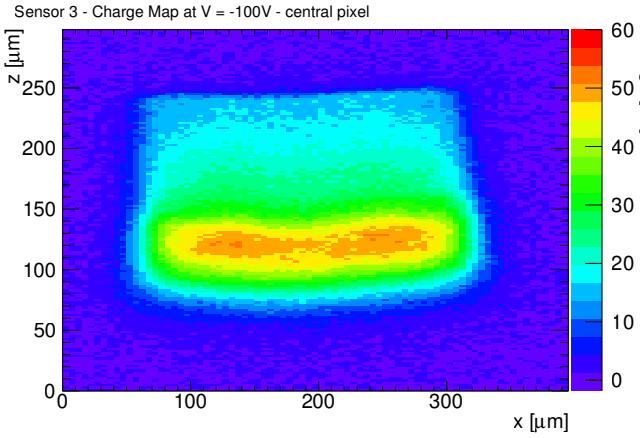


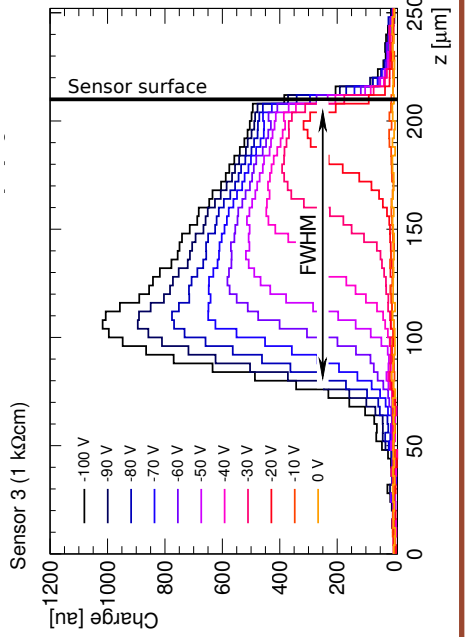
External pixels

Central pixel

1000 Ωcm



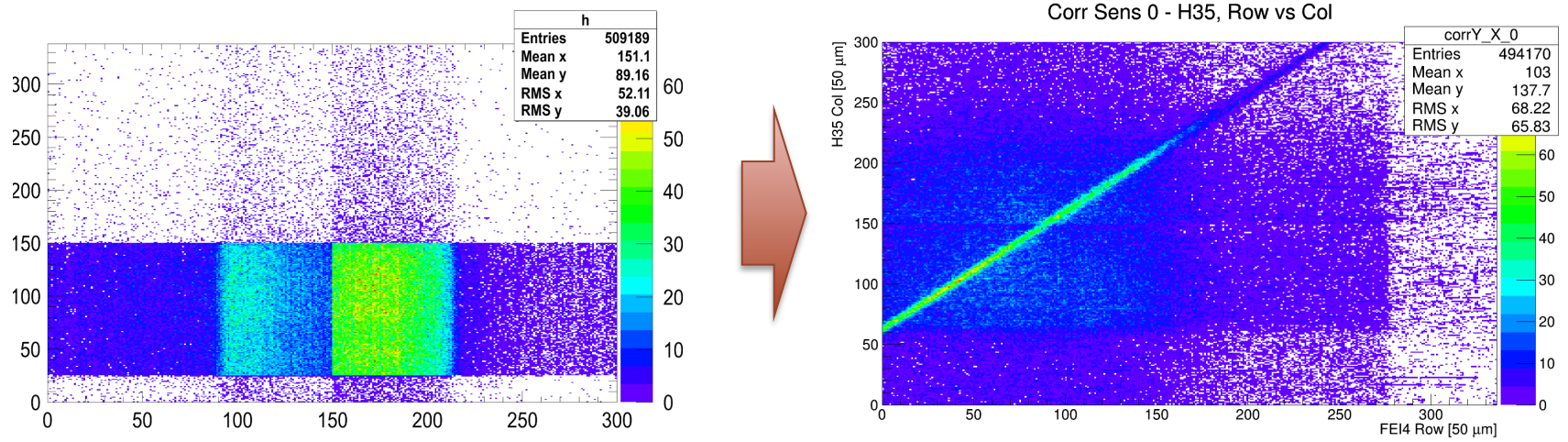




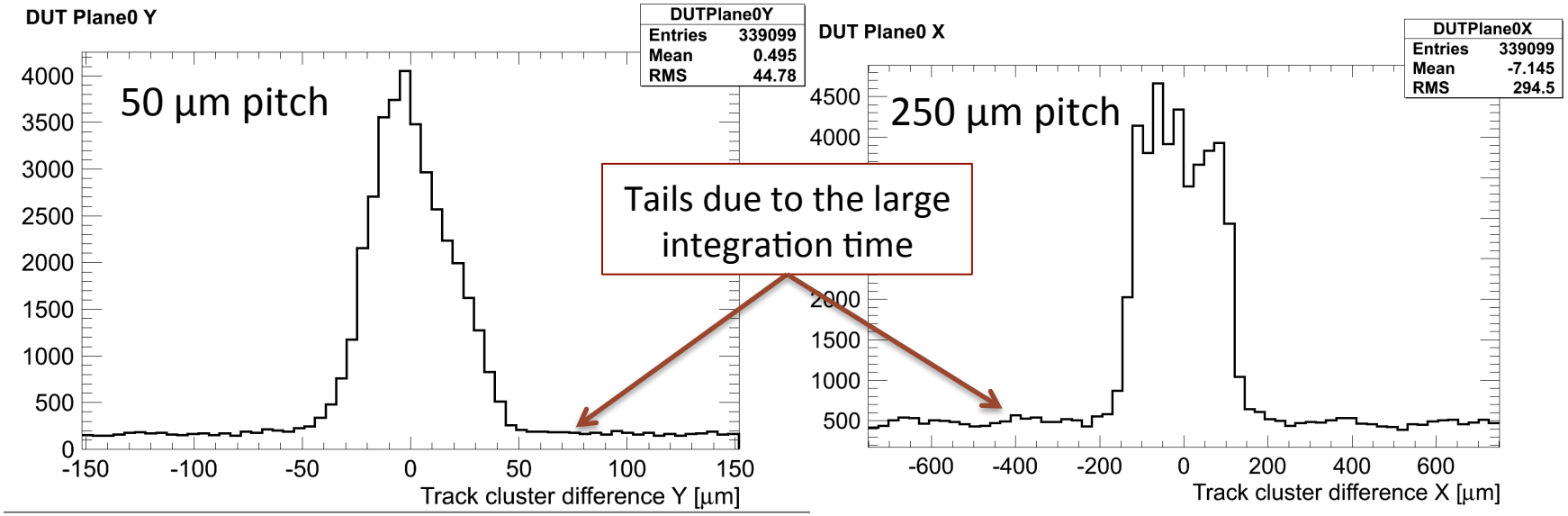
When depletion gets larger of 100 µm the central pixel starts to collect charge from the neighboring pixels

Synchronization and alignment

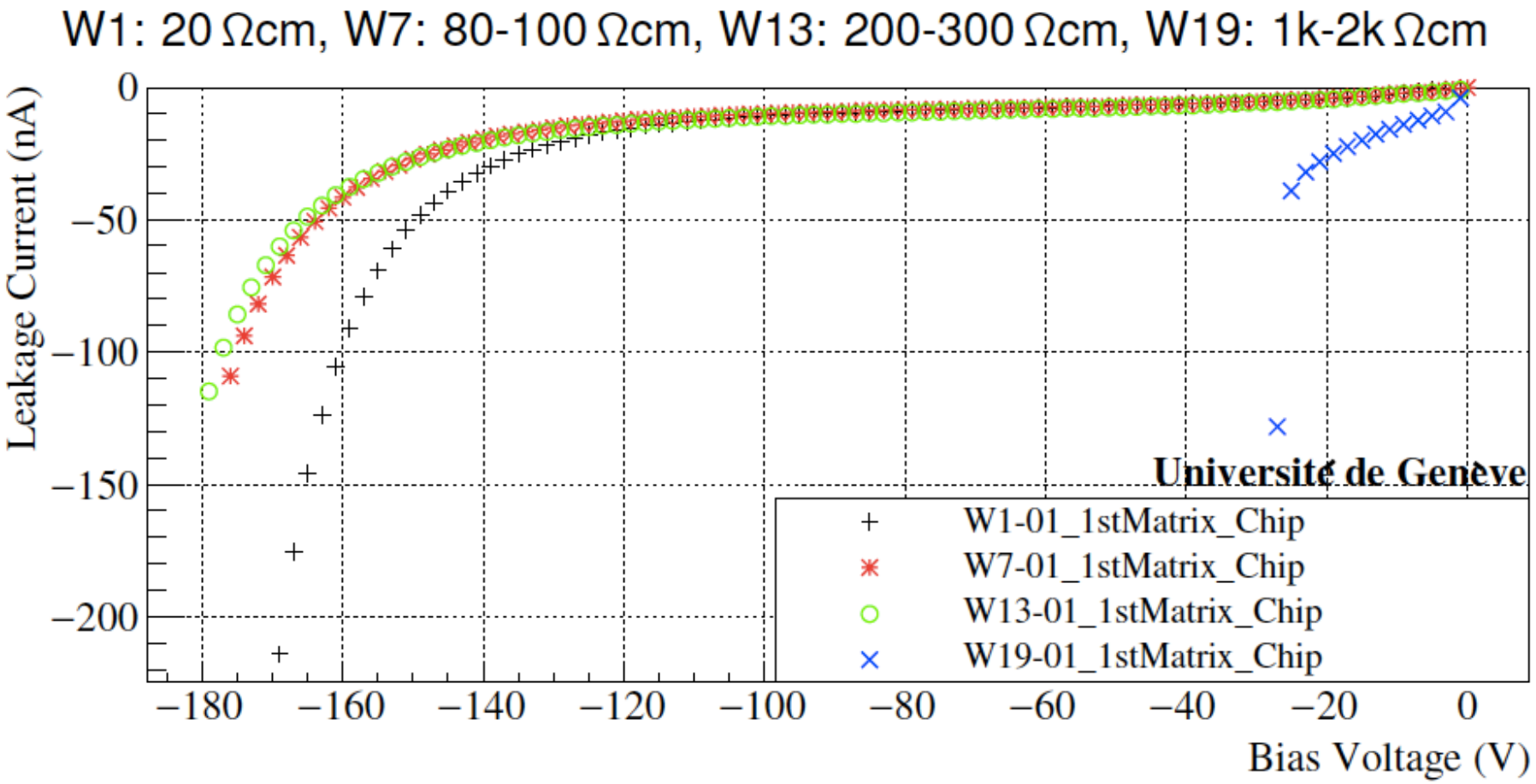
- Correlations between the hits in the H35 CMOS matrix and a telescope plane show the successful synchronization of the data



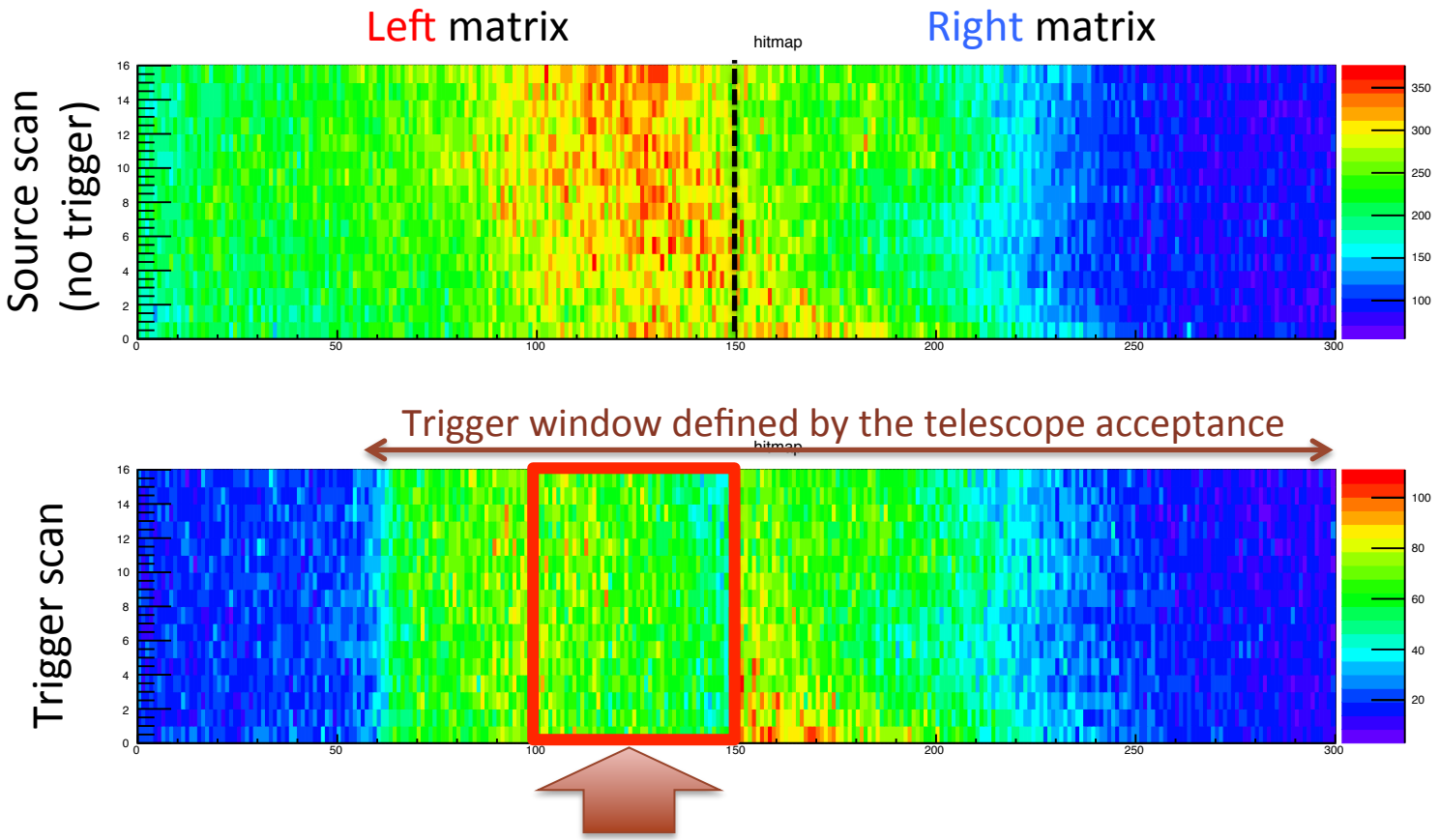
- Consistent residual shape and width after alignment and tracking with Judith



H35 – matrix IVs

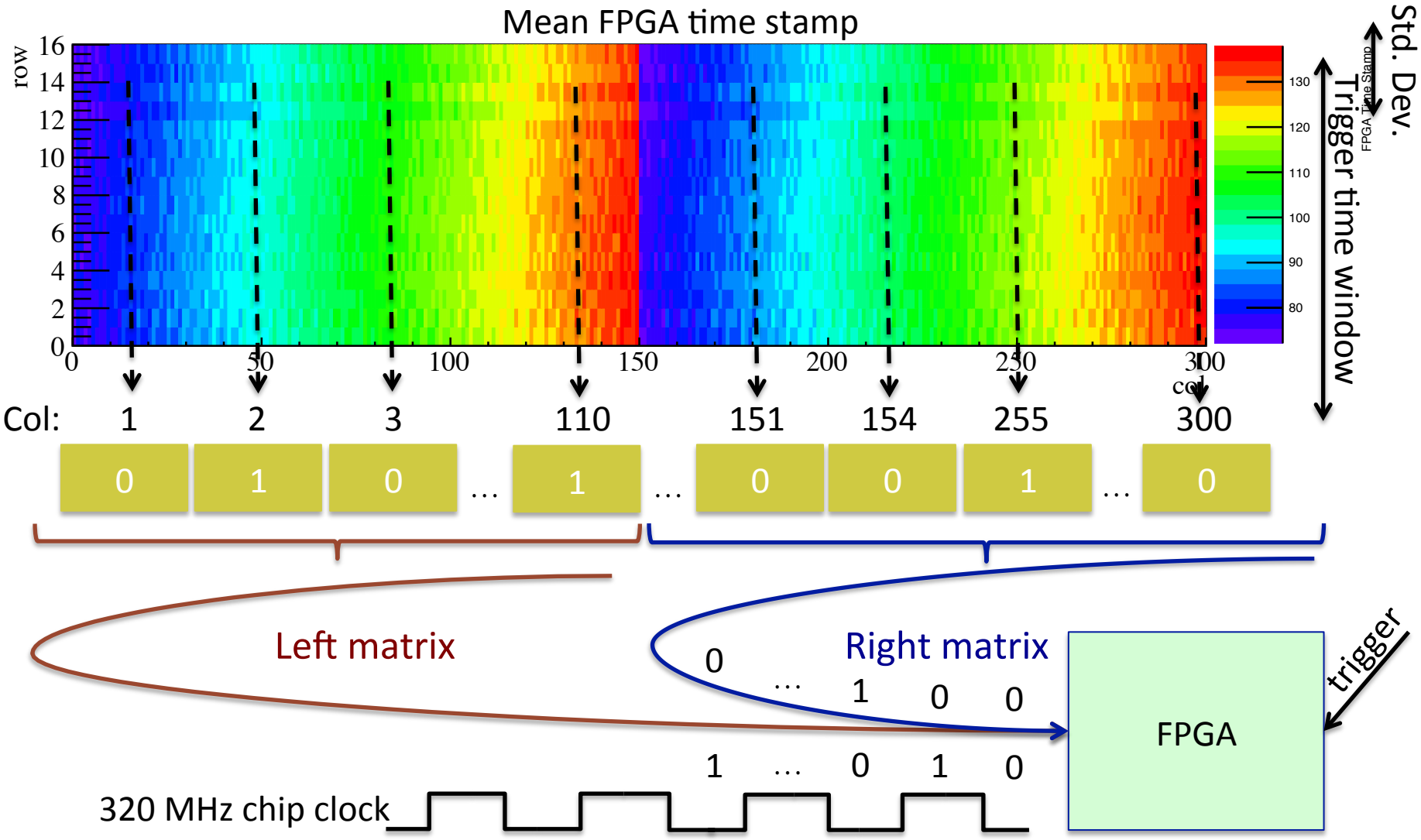


Hitmap



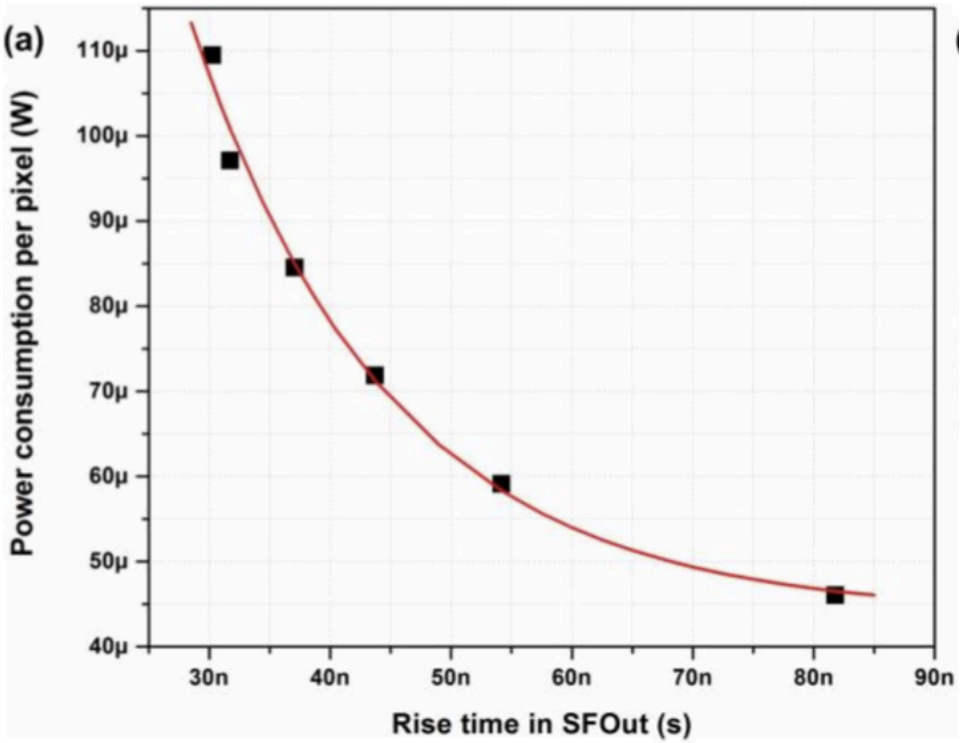
Hit loss because of limited trigger time window

Trigger readout



N.B: FPGA time-stamp != chip time-stamp: it is not the time of the hit recorded by the chip, but just the time when the hit reach the FPGA

Power vs. rise time



- Simulation of the power consumption as a function of the rise time for analog pixels with high gain
- For low gain pixels (-p-tub +extra capacitor) the rise time can go down to 20 ns with aggressive settings

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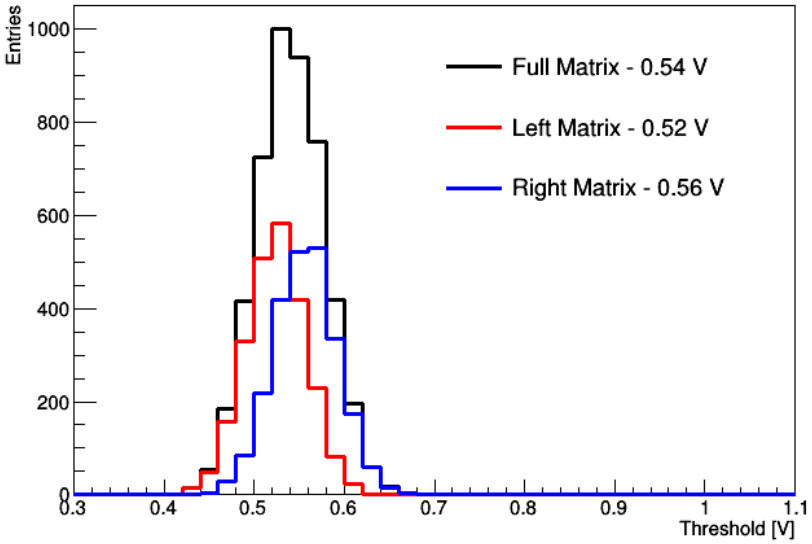
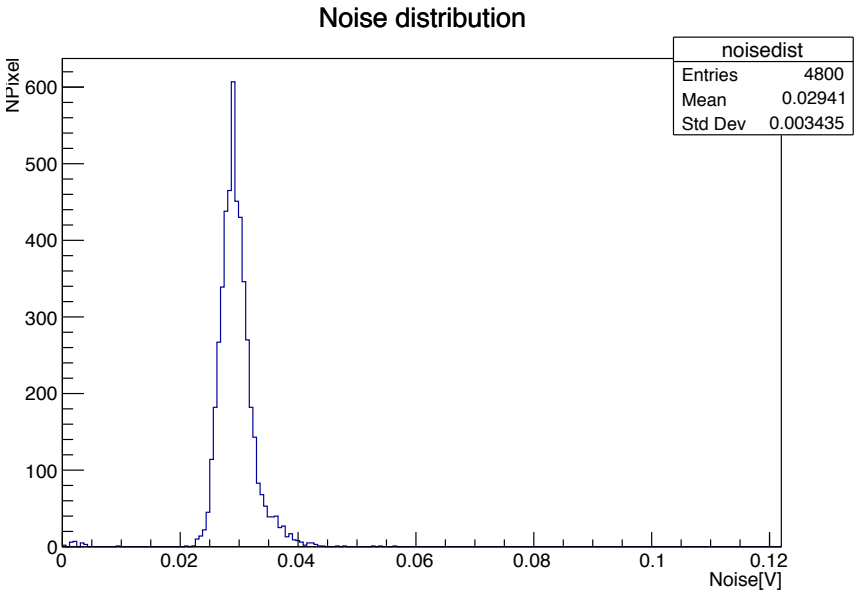
Threshold noise





- Threshold:
  - Mean = 0.54 V
  - Std. Dev. = 0.04 V

- Noise:
  - Mean < 0.03 V
  - Std. Dev. ~0.003 V