



Development of ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

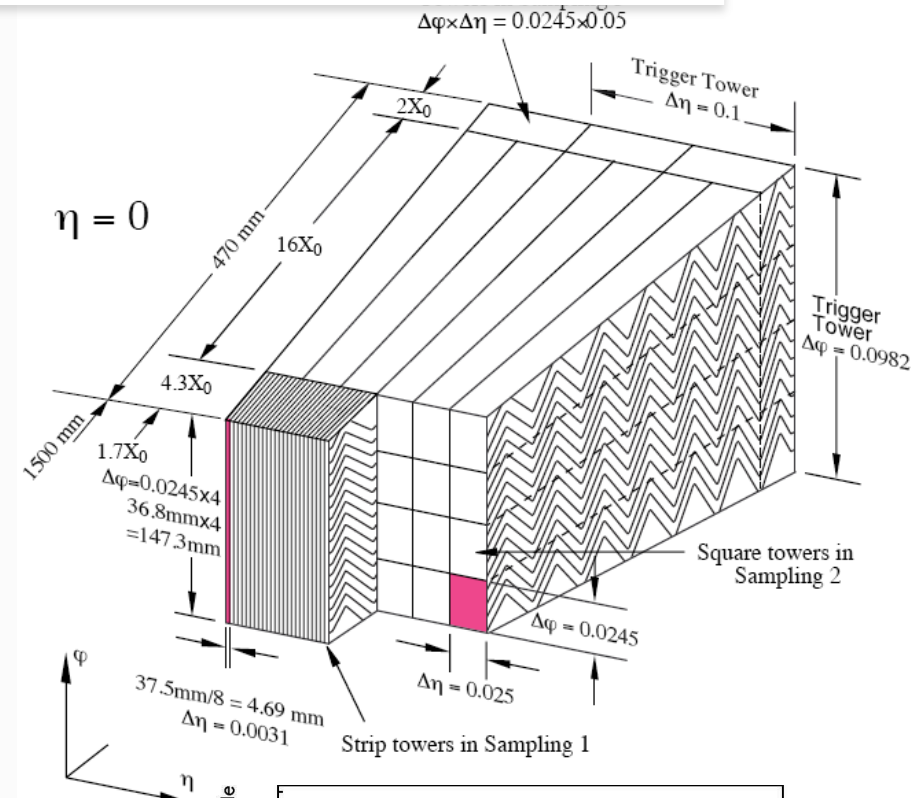
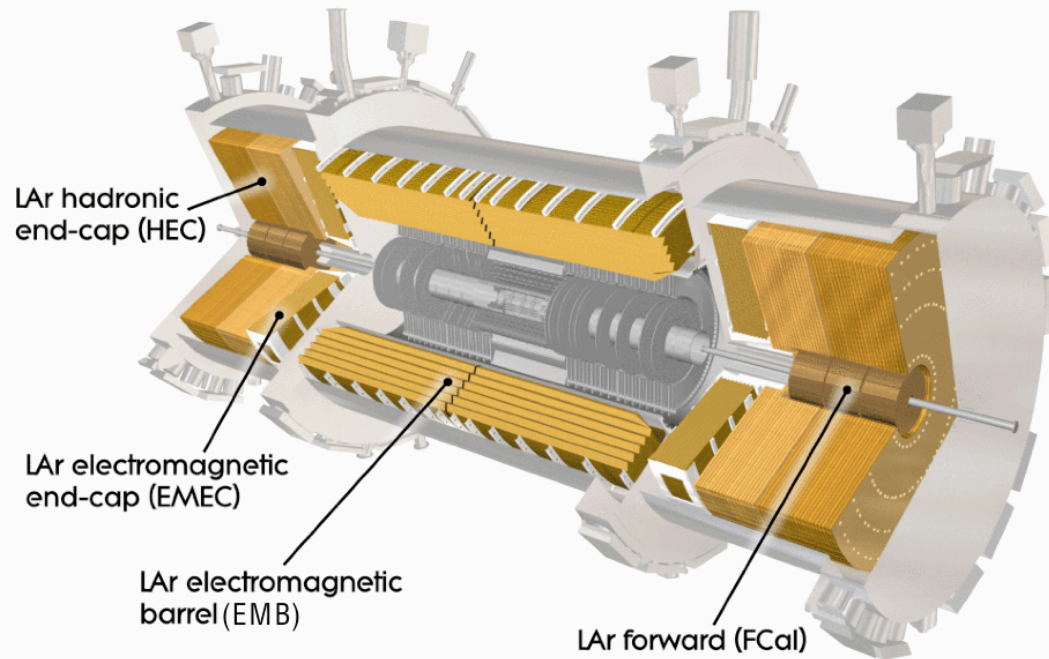
Gustaaf Brooijmans



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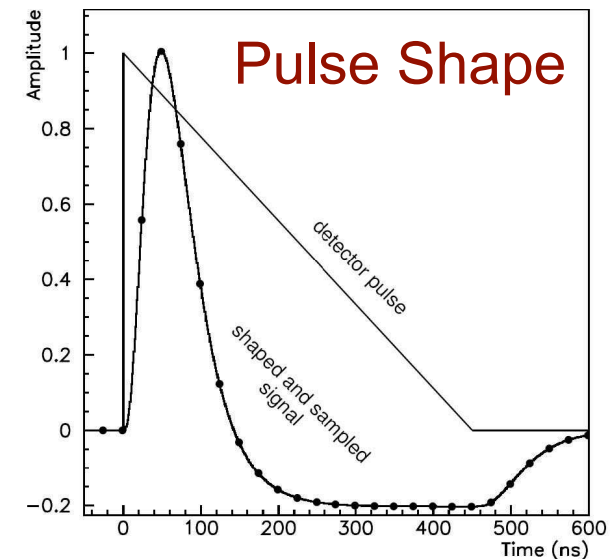
on behalf of the ATLAS Liquid Argon Calorimeter Group

The ATLAS Liquid Argon Calorimeters



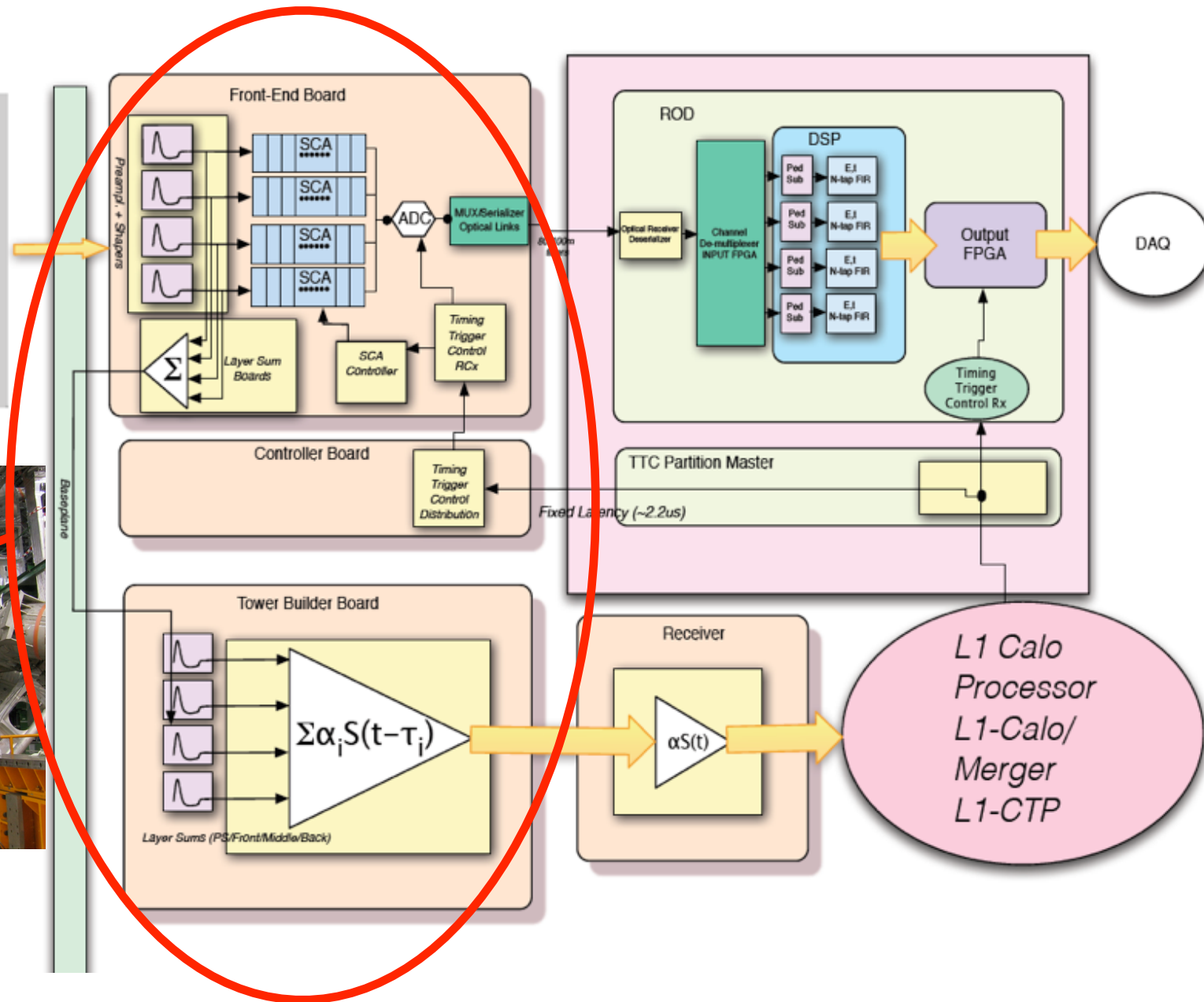
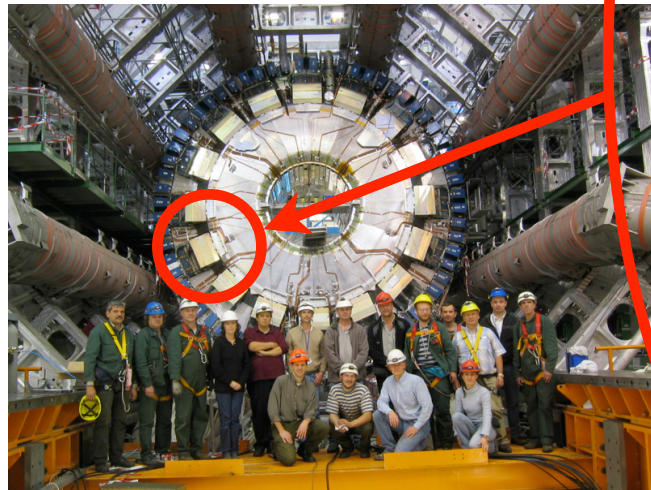
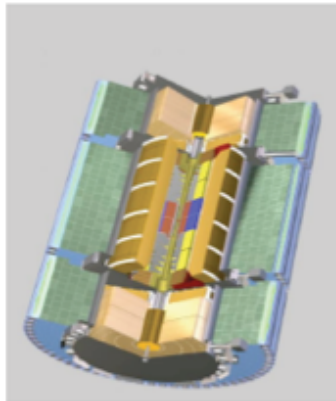
❖ Fine-grained lead (EM)/copper (HEC & FCal)/tungsten (FCal) - liquid argon sampling calorimeter

- At shower maximum (“middle layer”), $\Delta\eta \times \Delta\phi = 0.025 \times 0.025$
- ~180,000 cells





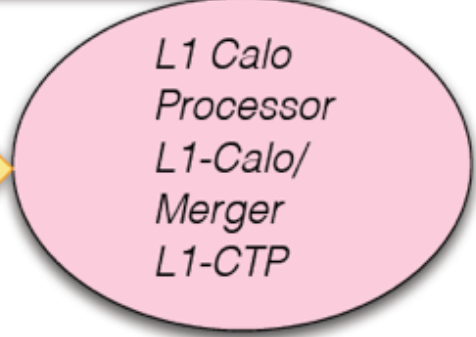
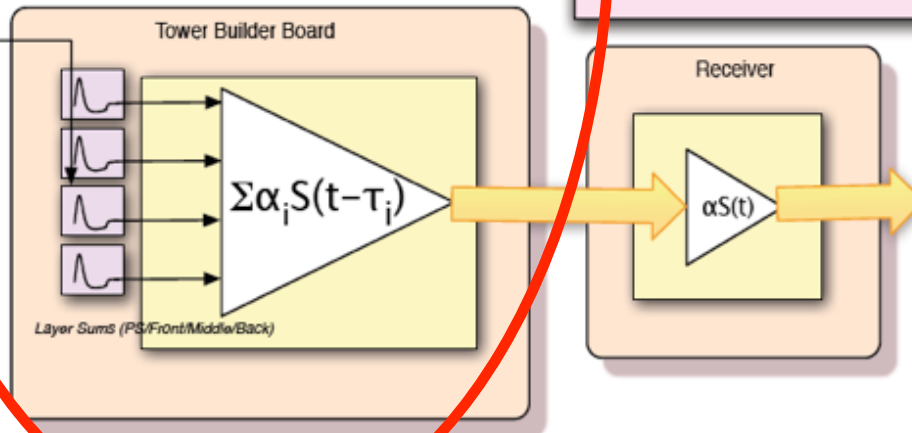
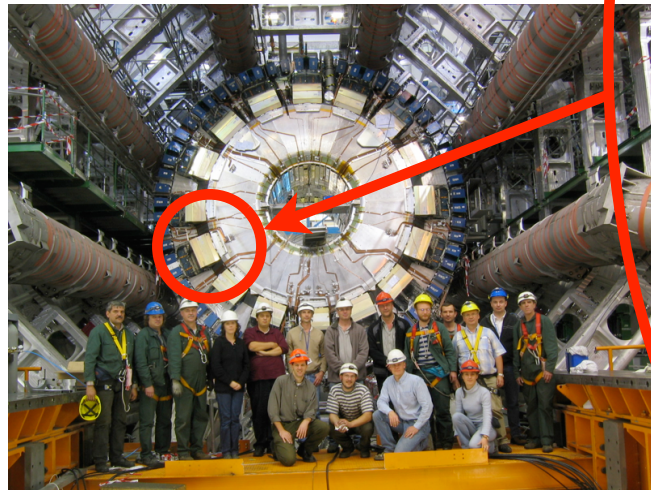
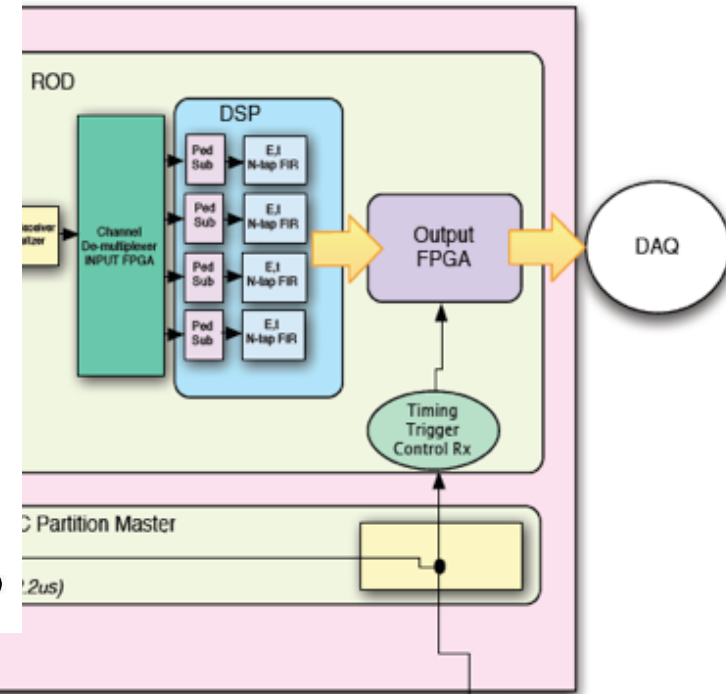
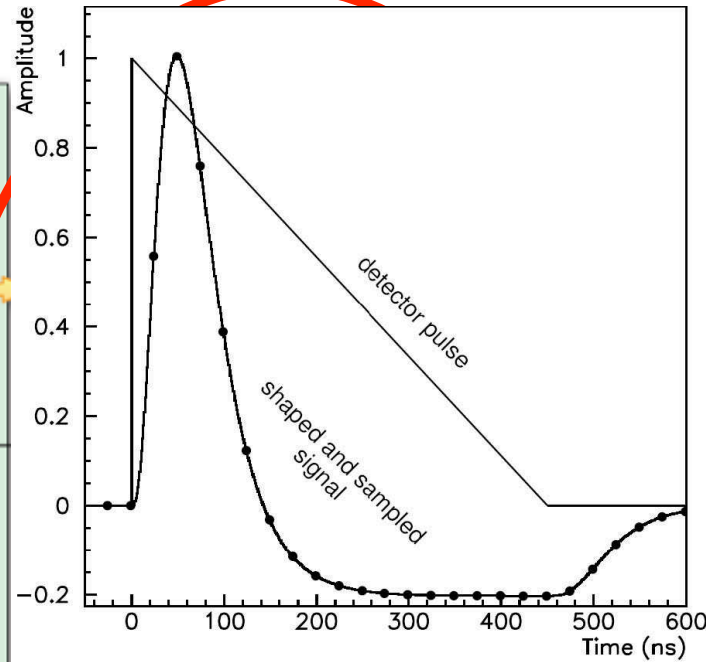
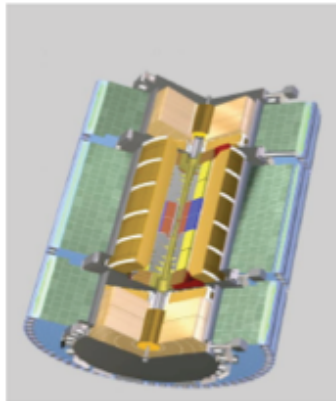
Today's Readout



L1 Calo Processor
L1-Calo/
Merger
L1-CTP



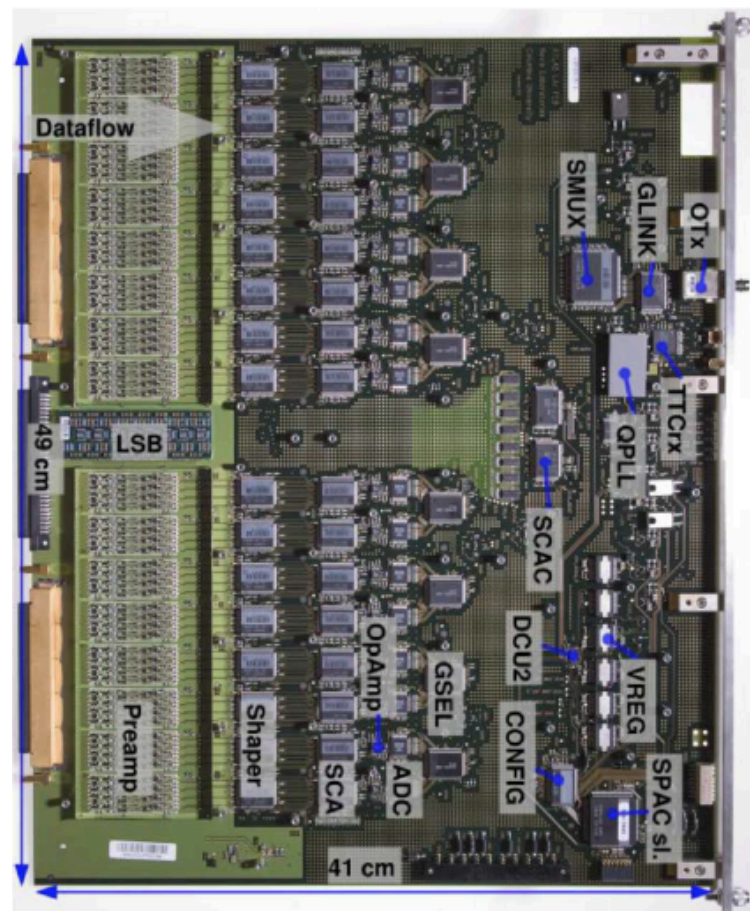
Today's Readout



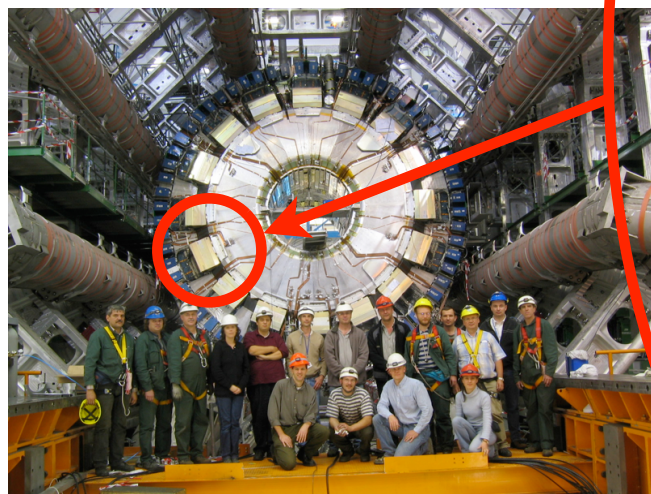
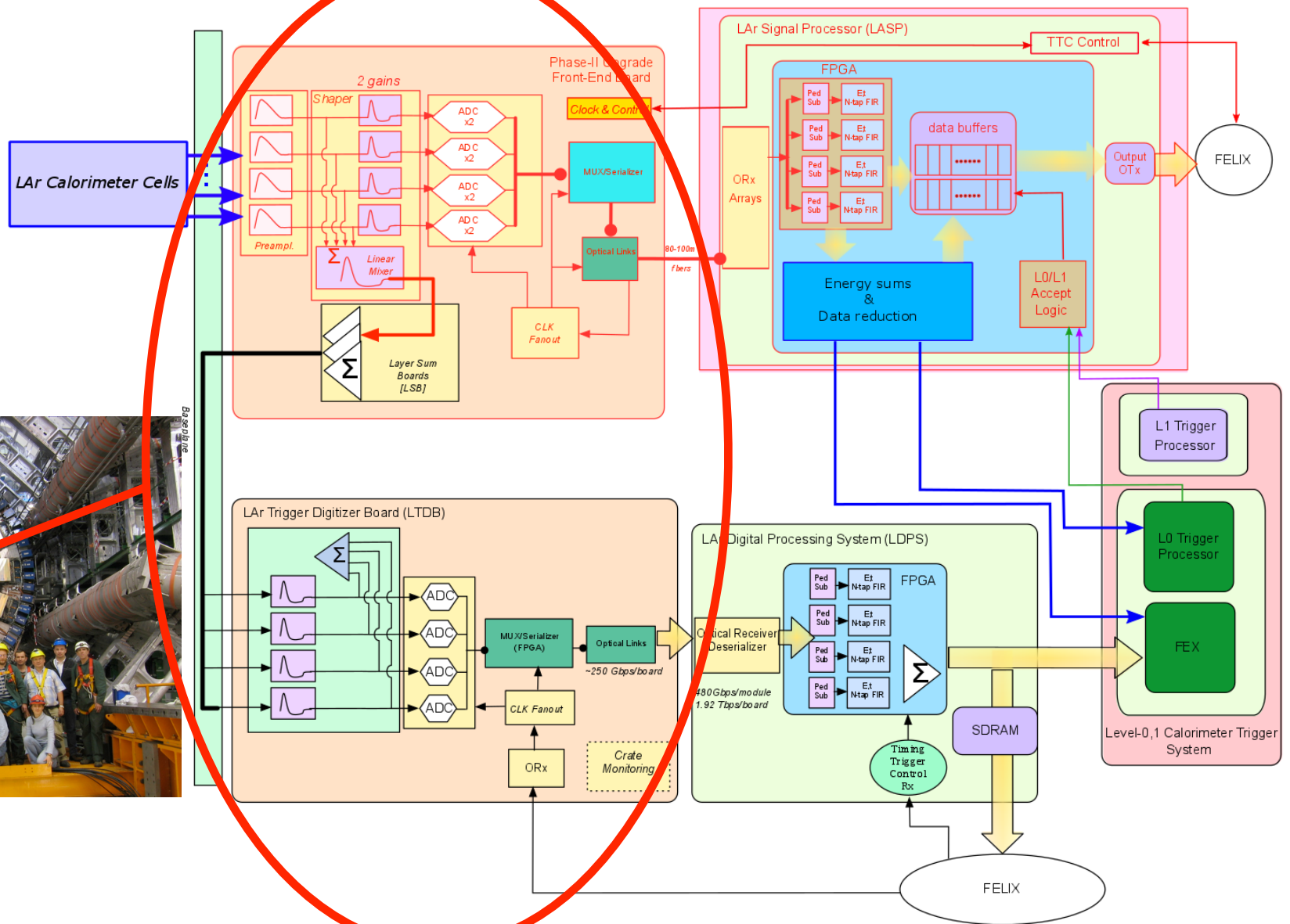
Upgrade?

❖ Front-end electronics installed on cryostat

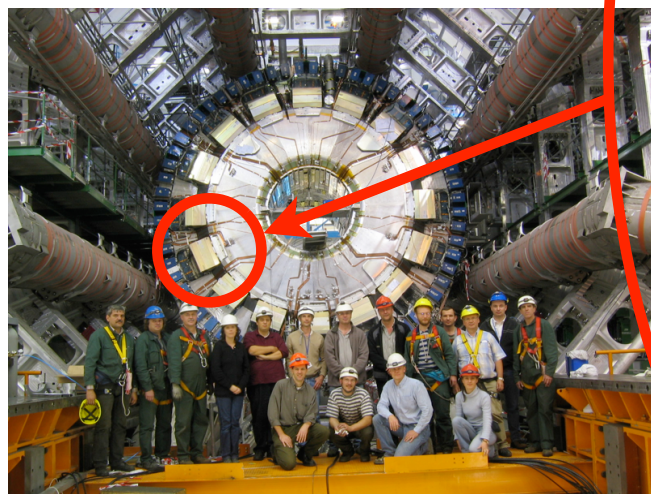
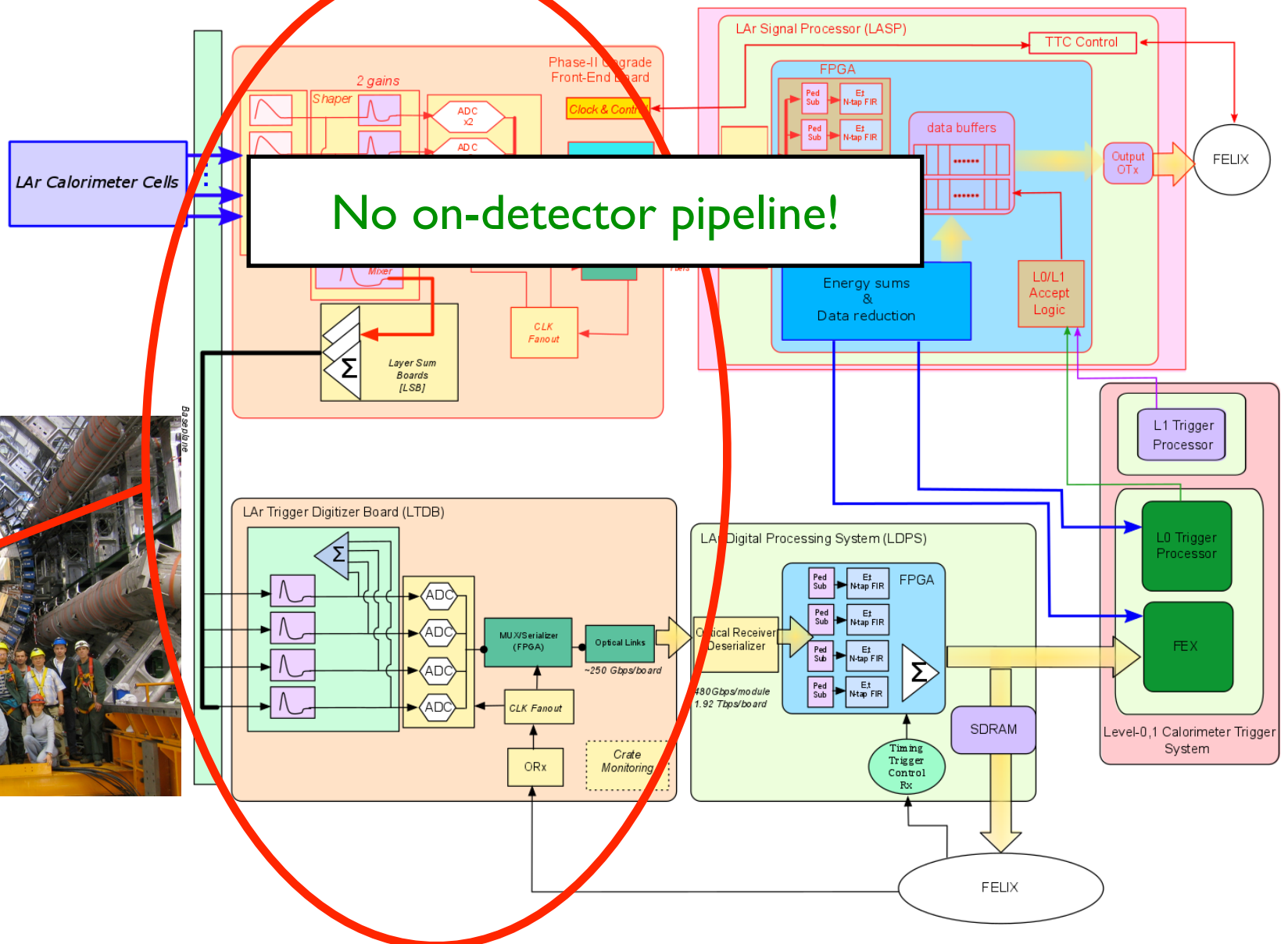
- Required to maintain analog precision
- Moderate radiation tolerance requirement (by LHC standards) for ASICs
 - 1 kGy (= 100 kRad)
 - $2.7 \cdot 10^{13} \text{ n/cm}^2$
- Current version incompatible with Trigger upgrade
 - Limited to 2.5 μs latency, 100 kHz read-out
 - Want 60 μs , 1 MHz
- Partial upgrade not possible
 - Rebuild all 1524 front-end boards (FEB)
 - And 120 calibration boards
 - And, therefore, off-detector electronics



2026 Readout



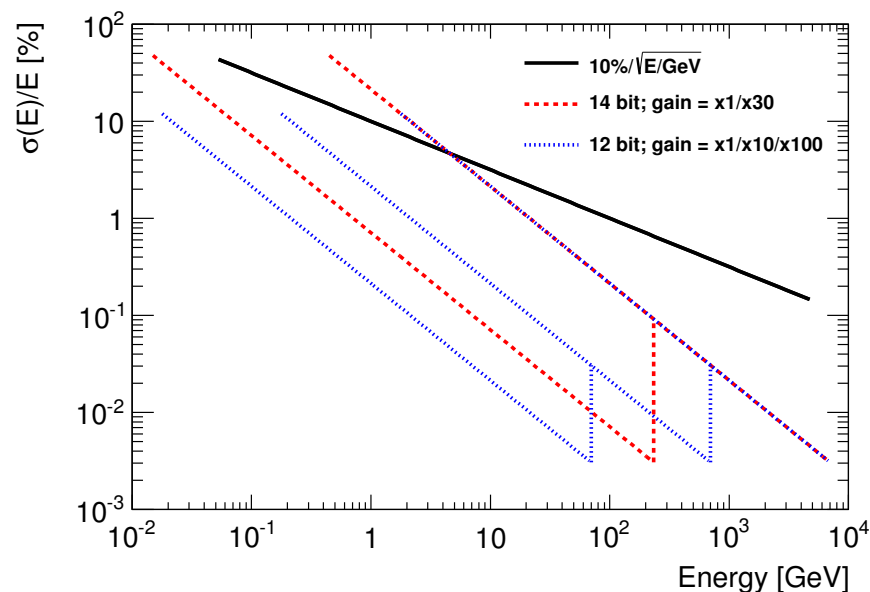
2026 Readout





Key Front-End Specifications

- ❖ Cover full energy range from electronics noise level to highest possible energy deposited in a single cell: 50 MeV to 3 TeV
 - Approximately 16-bit dynamic range, achieved using multiple gains
- ❖ Linearity of 0.1% up to $\sim 10\%$ of the dynamic range, somewhat looser at higher energies
- ❖ Keep electronics noise well below intrinsic calorimeter resolution
 - Effectively need ~ 11 -bit precision at high energy
 - Equivalent noise levels in analog signal shaping
- ❖ Ship all data off-detector
 - No future issues with TDAQ latencies/rates
 - ~ 1.3 Gbps per channel if send two gains
 - ~ 180 Gbps per front-end board
 - ~ 275 Tbps for the full LAr calorimeter
- ❖ Key ASICs:
 - Preamplifier+shaper
 - ADC
 - Serializer

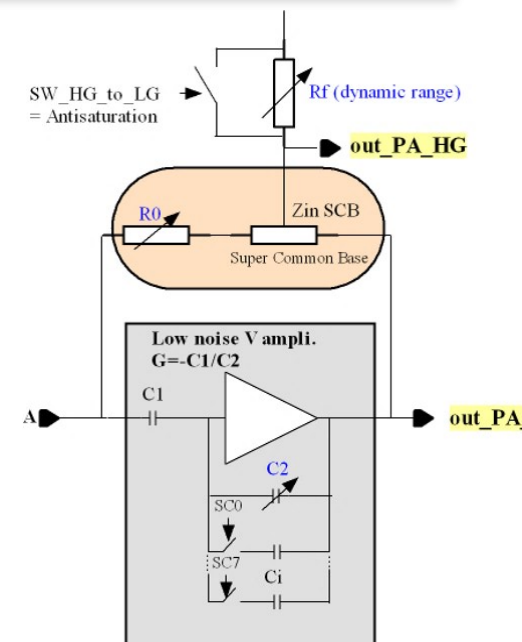


R&D mainly 65 and 130 nm CMOS:
Benefit from other HL-LHC work,
incl. radiation tolerant developments

Preamp+Shaper

❖ Test chip in 130 nm CMOS (TSMC)

- New line terminating preamp with dual range output and electronically cooled resistor
- Test chip (with various transistor sizes, capacitor types, protection diodes) undergoing first tests

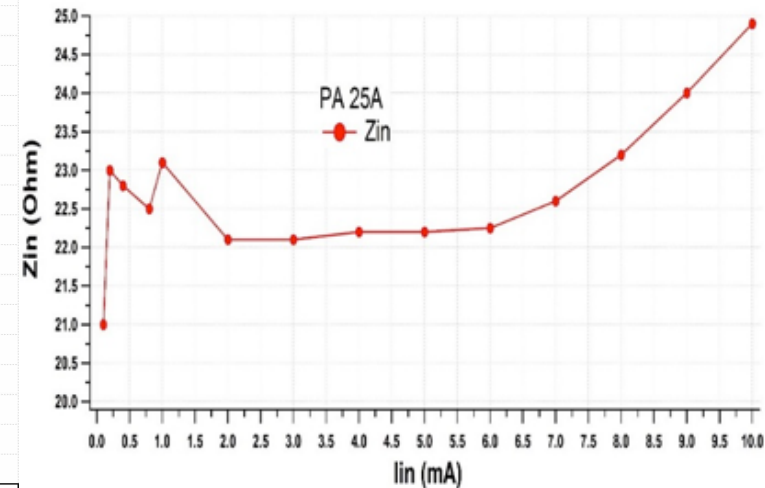
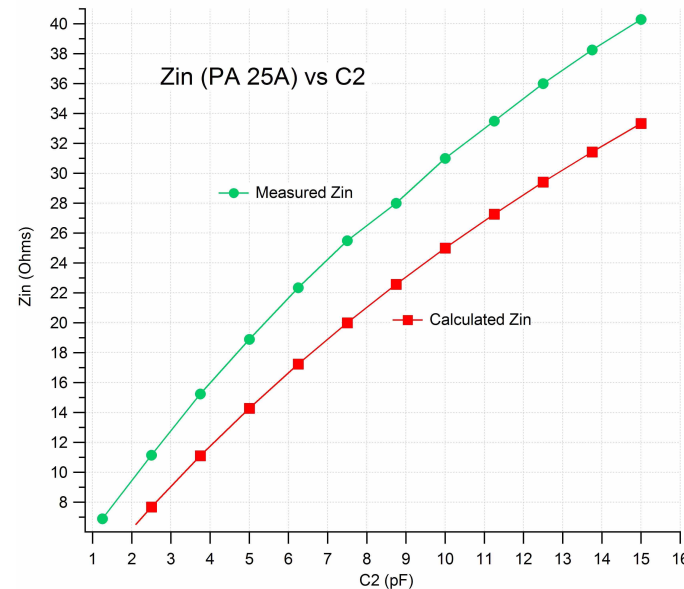
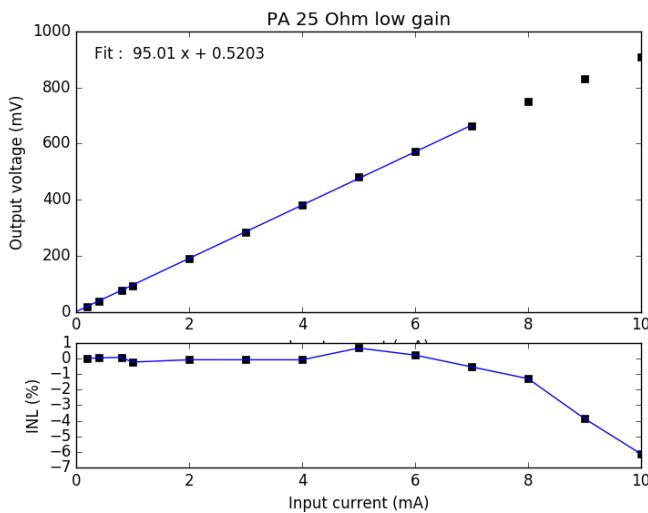


R0, C2 tunable to set absolute value of Z_{in}
 Ci: 8-bit fine adjustment of Z_{in} ($\pm 5\%$)
 using Slow Control parameters



Preamp-Shaper Test Chip

❖ Measurements on 130 nm CMOS test chip



Linearity $\sim 0.1\%$ at high gain,
within 1% up to 7 mA
(larger than max signal from
 $m=5$ TeV $Z' \rightarrow ee$)

Input impedance vs C_2

Input impedance vs
input current



Preamp+Shaper

❖ Test chip in 130 nm CMOS (TSMC)

- New line terminating preamp with dual range output and electronically cooled resistor
- Test chip (with various transistor sizes, capacitor types, protection diodes) undergoing first tests

❖ Pre-prototype in 65 nm CMOS (TSMC)

- Programmable peaking time, ADC driving capability, sum x4 and sum x8 outputs, programmable pulse generator, configuration logic and registers

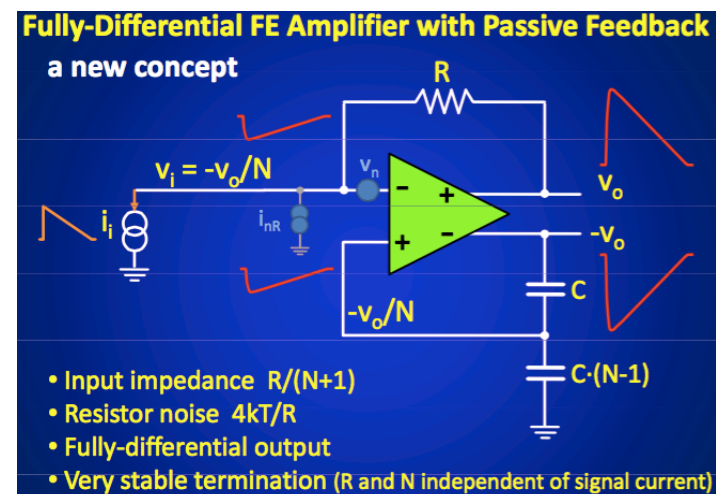
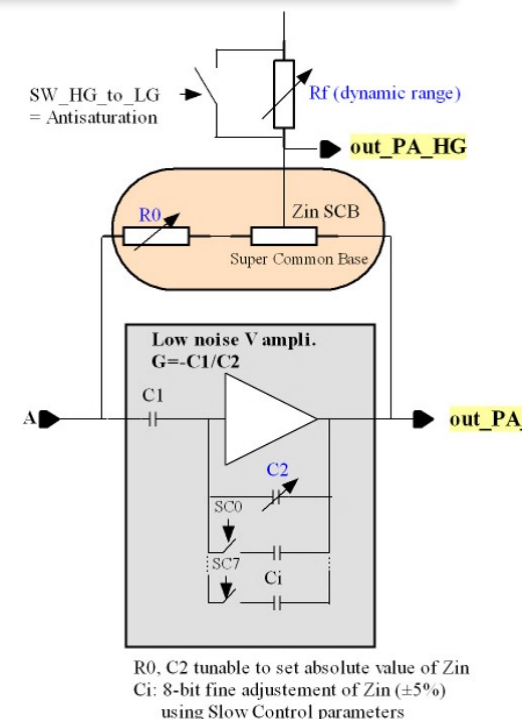
▪ Low noise:

- Fully differential, passive feedback

- Low power ~ 110 mW/channel
- Aim to submit 8-channel version in April 2017

❖ Test boards/benches common to both efforts

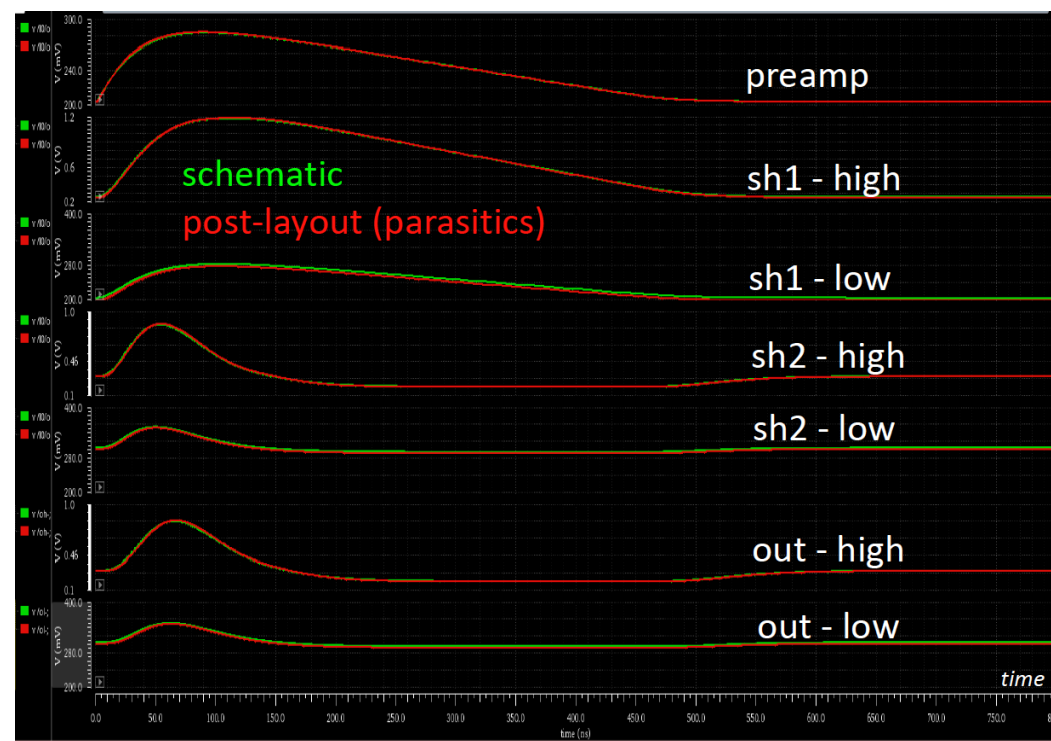
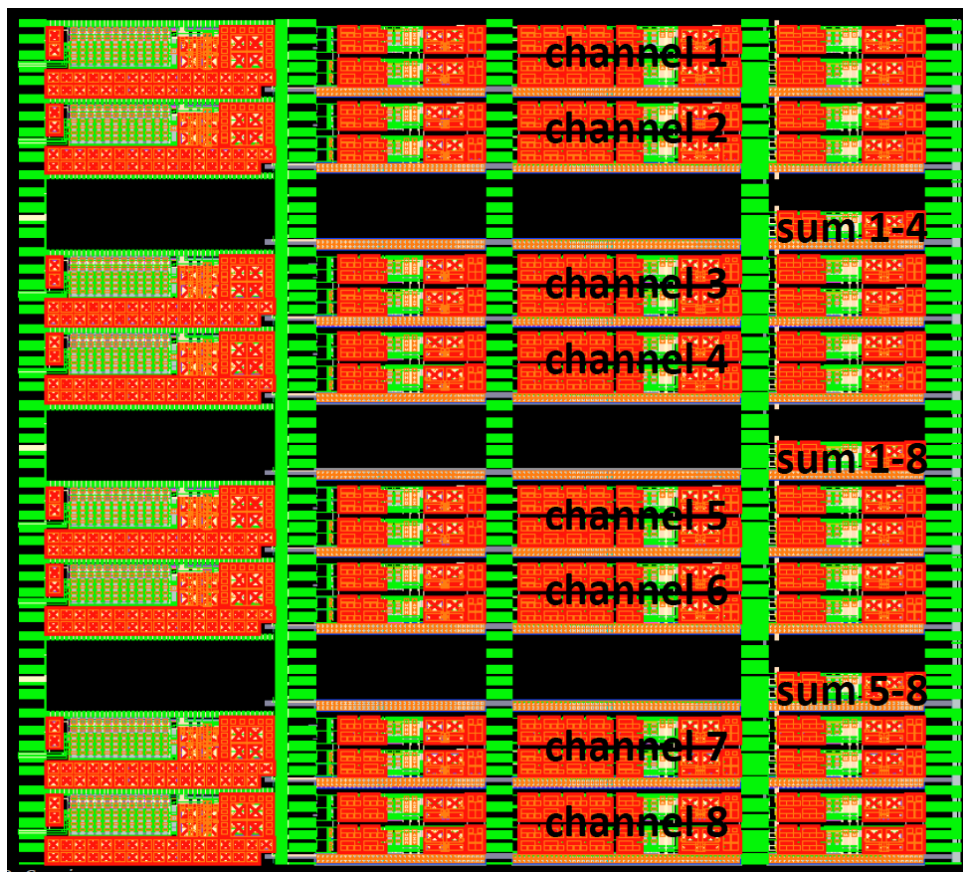
❖ Choose architecture & technology by end 2017





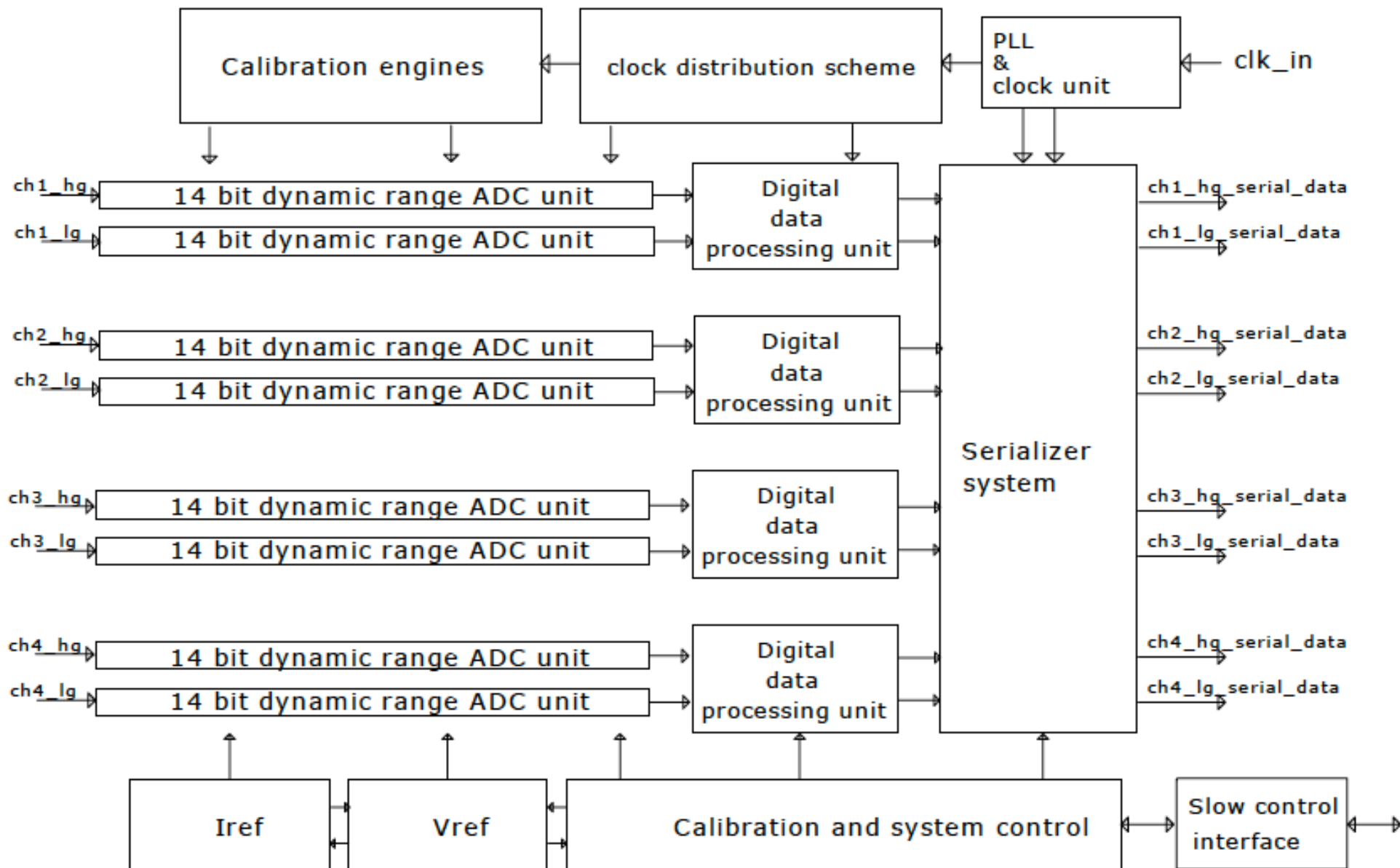
Preamp-Shaper Simulation

❖ 65 nm prototype chip





ADC: 4x2 Channels





14-bit ADC Unit

- ❖ Core ADC block contains 12-bit SAR and Dynamic Range Enhancer
 - DRE block similar to 4x amplifier, but baseline is at $-V_{fs}/2$...
 - Test chip submission (TSMC 65 nm CMOS) in May 2017, will contain DRE+SAR, rad-hard I/O, bandgap, ...
 - Then ~yearly submissions to final prototype in ~2020



Low gain channel

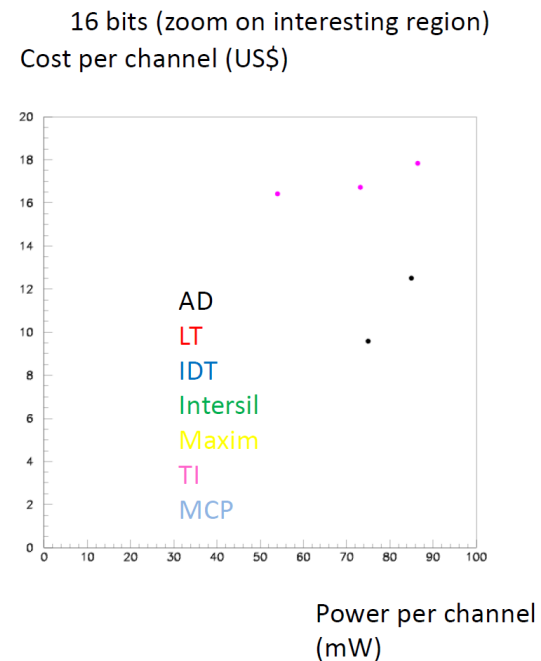
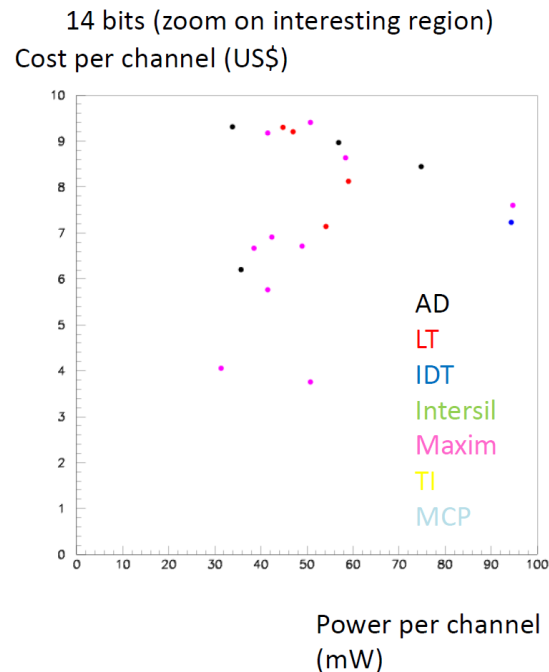


High gain channel



Commercial ADCs

- ❖ New market survey performed, select candidates based on power and cost
 - 20 candidate 14-bit ADCs, 7 16-bit candidates
 - Different vendors, sampling rates (may multiplex if use e.g. 200 MSPS device)
 - Irradiation tests planned for 2017

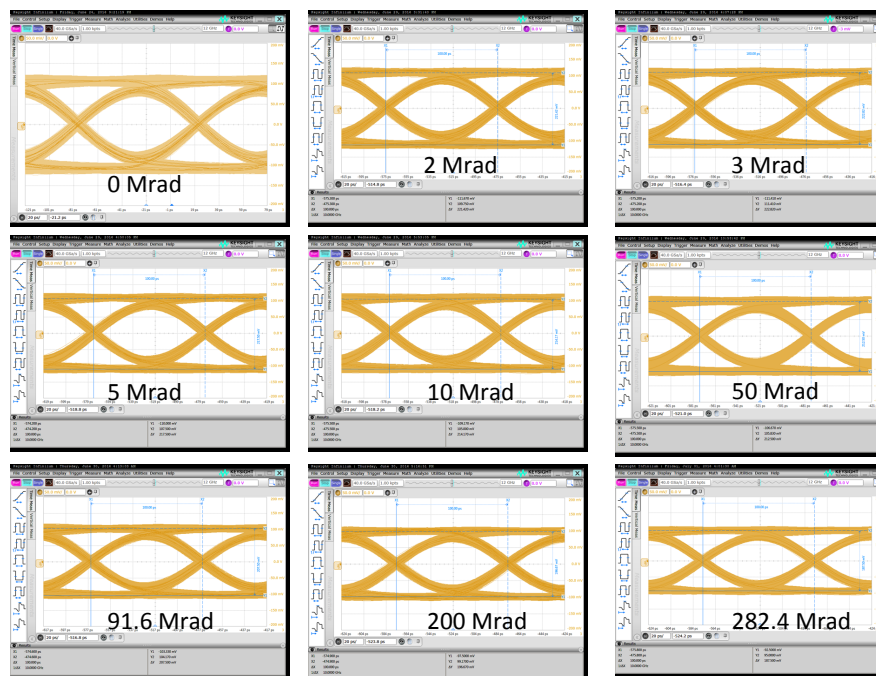




Serializer

- ❖ Use CERN-based IpGBT (8.96 Gbps data bandwidth out of 10.24 Gbps total) and Versatile Link+
 - Contribute to developments
 - Prototype VCSEL array driver ASICs successful, but iteration needed
 - Expect to map 4 IpGBT → 4-channel VL+ module
 - 20 IpGBTs for data transmission per FEB2 (128 calorimeter channels)

Optical driver
prototype
radiation tests





Power

- ❖ Currently HV to DC-DC converter located in Tile calorimeter “fingers” (not accessible), output 11V and lower to front-end crate (~2.5 kW/crate)
- ❖ Would like to move main DC-DC converters to more accessible location
 - HV to 48V or 24V or 12 V
 - Further down-conversion on FEBs themselves (operating voltages will be in 1-2.5 V range)
- ❖ R&D in Si power MOSFETs, and GaN transistors (now exist for high voltage/high current)
 - Successful GaN irradiation test with “power off” (baby steps...)
- ❖ Promising commercial components appearing
 - 1.5 kW 380 V → 12 V in 61x25 mm² package
 - So far passed neutron tests, but failed TID tolerance
 - But if located further out (lower radiation levels) might work...



Front-End Board

- ❖ Architecture largely modeled on current FEB:
 - Clear analog/digital separation
 - Extensive grounding and shielding
- ❖ But minimize single points of failure
 - Multiple mostly independent sections
 - Only power shared
 - Boards individually clocked and controlled
 - No control board in crate
- ❖ Requires many links to/from FEBs
 - 20 lpGBTs to transmit data
 - 1 to 4 lpGBTs for clocks and slow control
 - O(35k) fibers in system
 - Connect to ATCA boards with high fiber density off-detector





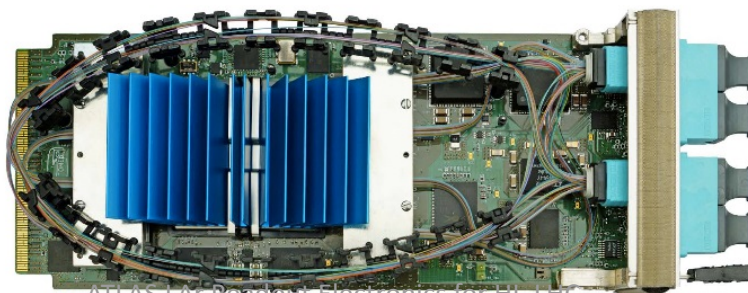
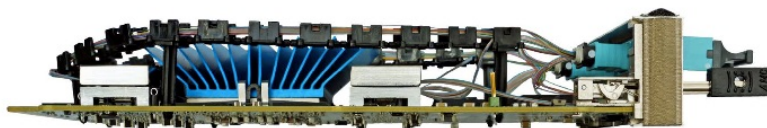
Off-Detector

❖ Processing of digitized waveform

- Filter calculates energy and time, suppressing electronics and pile-up noise
- Take into account accelerator bunch train structure

❖ Relies on modern communications and FPGA technology

- Similar to Phase-1 digital processing system (LDPS) which uses Advanced Mezzanine Cards with ARRIA 10 FPGAs
 - Receive data from LTDB, transmit to Level-1
 - 48 inputs at 5 Gbps
 - 48 outputs at 10 Gbps
 - After Level-1 accept, data to DAQ via ATCA carrier and RTM to FELIX



ATLAS LAR Readout Electronics for HL-LHC



Off-Detector

❖ Detailed design for HL-LHC premature

- Assume technology-scaled version of LDPS
 - Higher input link density: 3+ Tbps input per ATCA blade
- May need fiber remapping plant/hub to route data from 0.2 x 0.4 towers to same FPGA for pre-clustering
- Option of sending some full precision or precluster-like data to Level-0
 - Physics gains under study

❖ And filtering studies on-going

- Fully simulated waveforms with pile-up up to 200 and configurable LHC bunch pattern
- Realistic electronics noise & digital data processing
- Study shaping and sampling rate options, performance of different digital filtering schemes, etc
 - Minimize the impact of pile-up on the energy measurement
 - Expect better performance than current Optimal Filtering Coefficients



Summary

- ❖ All LAr electronics will need to be replaced for HL-LHC
 - Current version cannot meet trigger latency and rate requirements, would have very negative impact on HL-LHC physics reach
- ❖ Front-end R&D work on crucial components:
 - **Preamp+shaper**: Investigating multiple architectures, making test chips
 - **ADC**: Investigating both ASIC (test chip planned for May) and COTS ADC options
 - **Serialization**: Rely on CERN IpGBT
- ❖ Off-detector electronics modeled on Phase-1 upgrade digital processing system
 - But scaled for technological progress
 - **Continuously monitor FPGA market**

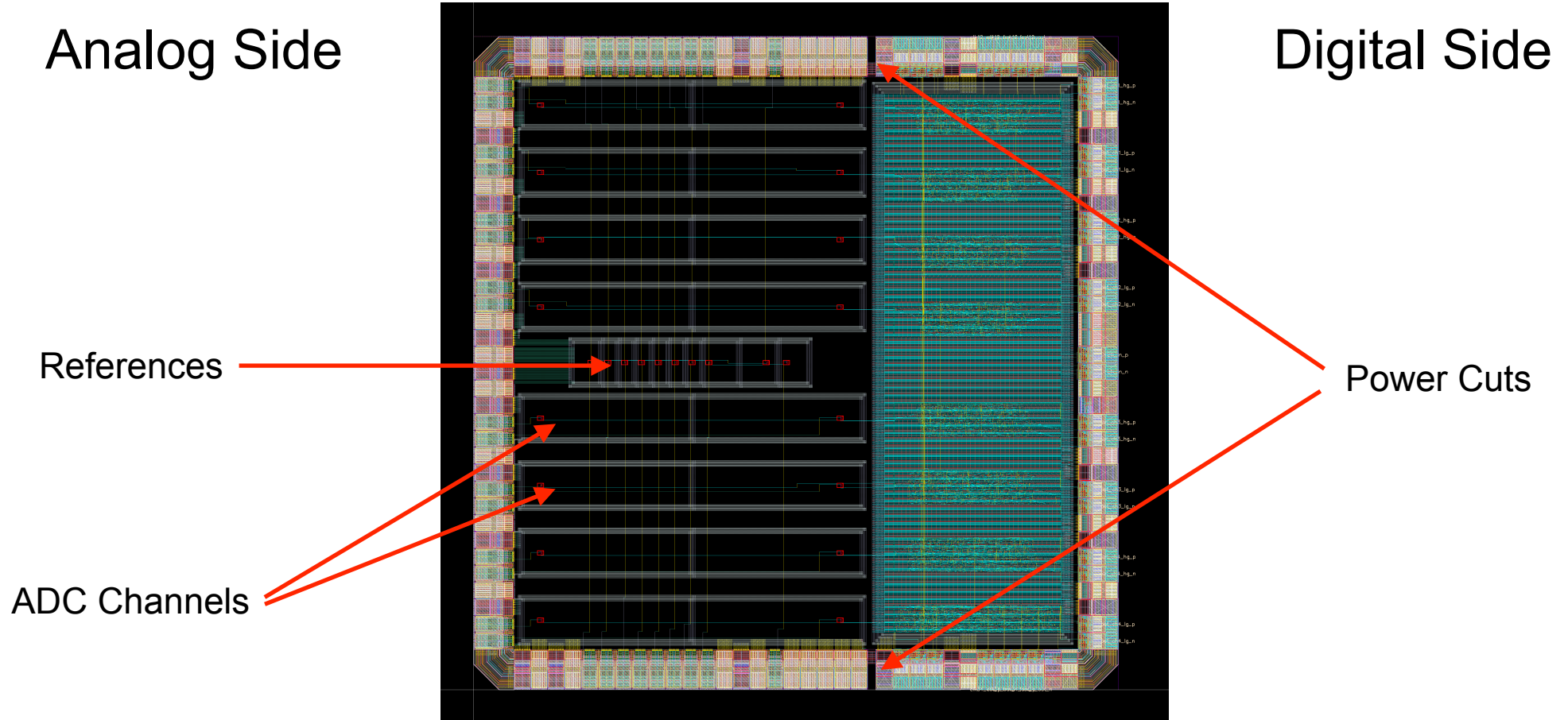


Supplementary Material

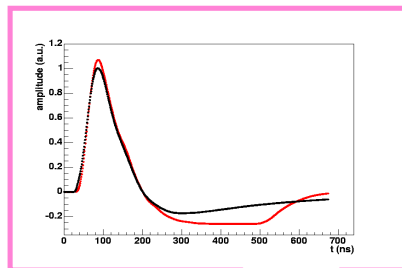


ADC Chip Layout

- ❖ “Assembled” a chip using fake building blocks
 - But I/O pads are real TSMC65 IO pads
 - Have integrated ESD diodes, but will need more on analog inputs



Optimal Filtering



$$E_{\text{cell}} = F_{\mu\text{A} \rightarrow \text{MeV}} \cdot F_{\text{DAC} \rightarrow \mu\text{A}} \cdot \frac{1}{\frac{M_{\text{phys}}}{M_{\text{cali}}}} \sum_{i=1}^{M_{\text{ramps}}} R_i \left[\sum_{j=1}^{N_{\text{samples}}} a_j (s_j - p) \right]^i$$

Cell energy
Sampling fraction
Calibration board
ADC to DAC (Ramps)
Pulse Samples
Optimal Filtering Coefficients
Pedestals

The above formula describes the LAr electronic calibration chain (from the signal ADC samples to the raw energy in the cell). Note that this version of the formula uses the general M_{ramps} -order polynomial fit of the ramps. We use a linear fit as the electronics are very linear, and we only want to apply a linear gain in the DSP in order to be able to undo it offline, and apply a more refined calibration. In this case, the formula is simply:

$$E_{\text{cell}} = F_{\mu\text{A} \rightarrow \text{MeV}} \cdot F_{\text{DAC} \rightarrow \mu\text{A}} \cdot \frac{1}{\frac{M_{\text{phys}}}{M_{\text{cali}}}} \cdot R \left[\sum_{j=1}^{N_{\text{samples}}} a_j (s_j - p) \right]$$

Crates and Power Supplies

