The Belle II Pixel Detector Data Acquisition and Background Suppression System

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- for the Belle II Pixel Detector Group

Instrumentation on Colliding Beam Physics,
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Overview

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1. The Belle II Detector
2. Requirements for the Pixel Detector DAQ

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3. The PXD DAQ System
   - the ASIC part, Front End Electronics
   - backend data handling
   - selection of interesting events
   - calculating ROIs

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4. Slow control system

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5. Results from Beam Test at DESY

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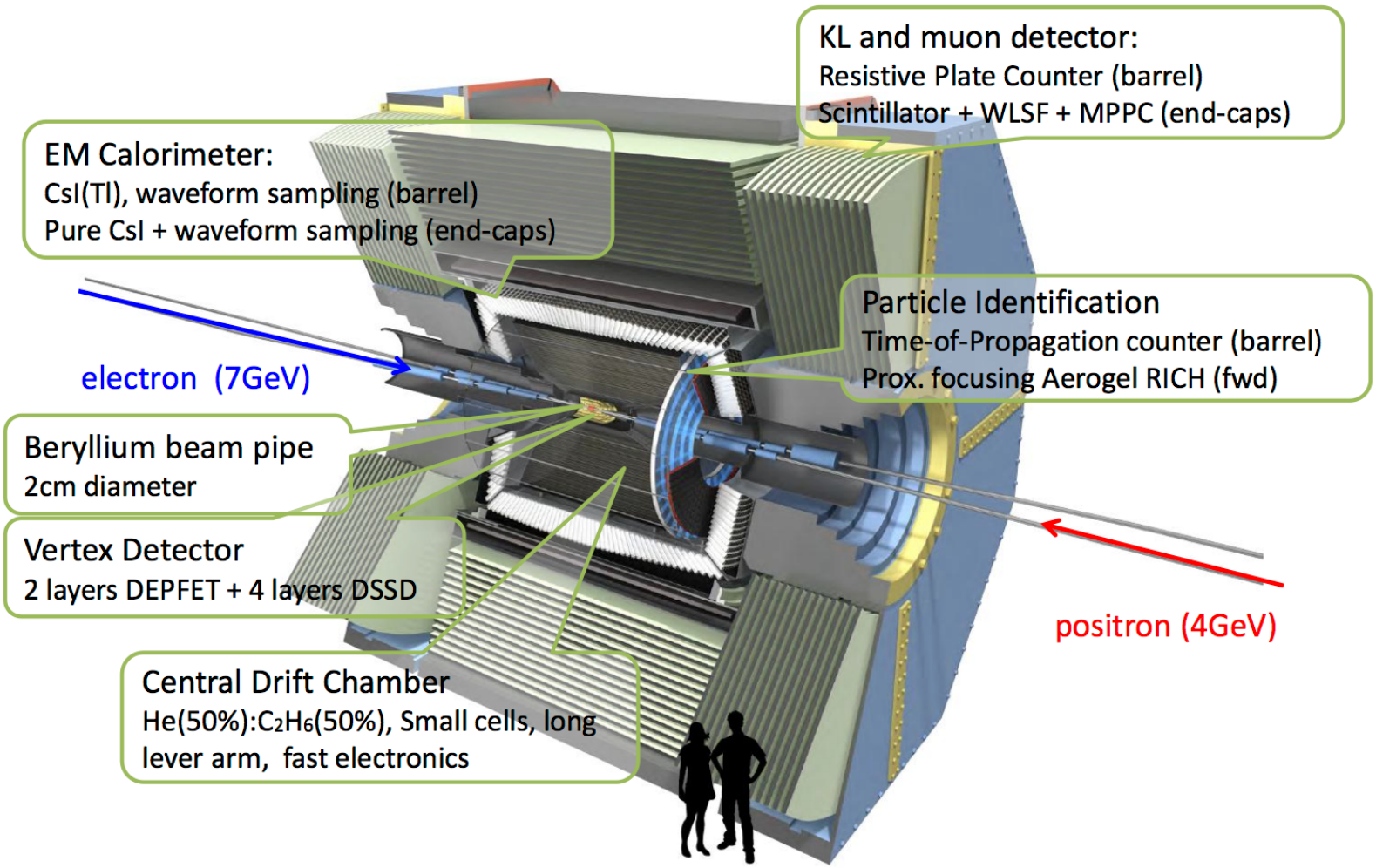
The Belle II Experiment

- *Belle II detector and upgrade of the Belle detector*



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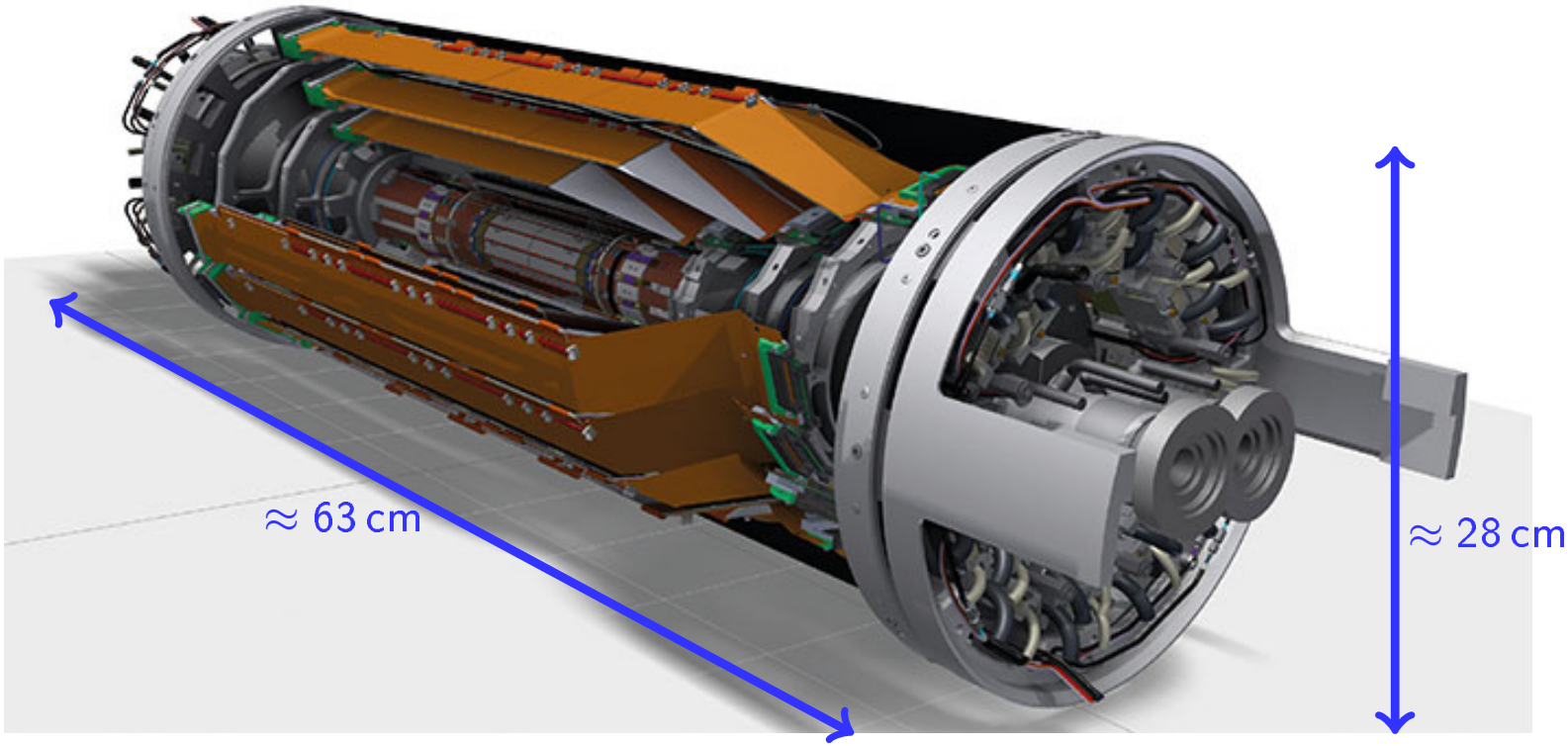
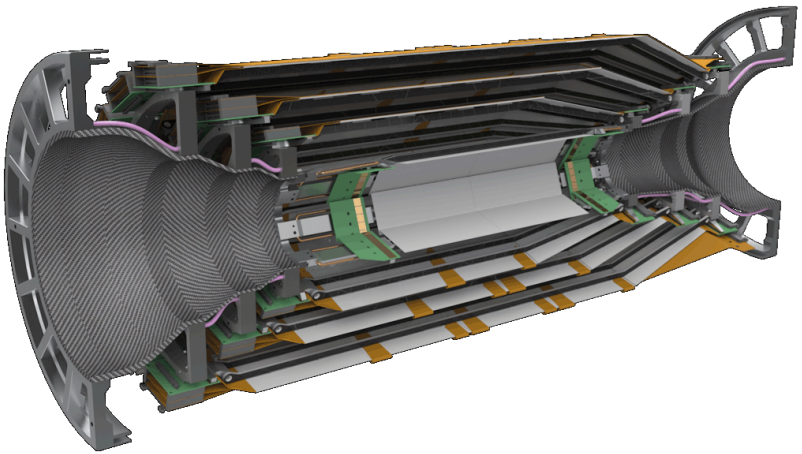
The Belle II Experiment
- *Vertex Detector*



The Belle II Experiment
- *Silicon Vertex Detector*



SVD

- Second innermost detector, 4 layers
- Orthogonally arranged p-doped and n-doped silicon strips
- Occupancy very high ($\sim 10\%$) due to short distance to IP and strip topology
  - first layer at $r = 38\,\text{mm}$
  - fourth layer at $r = 140\,\text{mm}$
- Angular acceptance, 17° to 150°
- Reconstruction of low-p_T (50 MeV) tracks possible
  $\rightarrow$ `DATCON`

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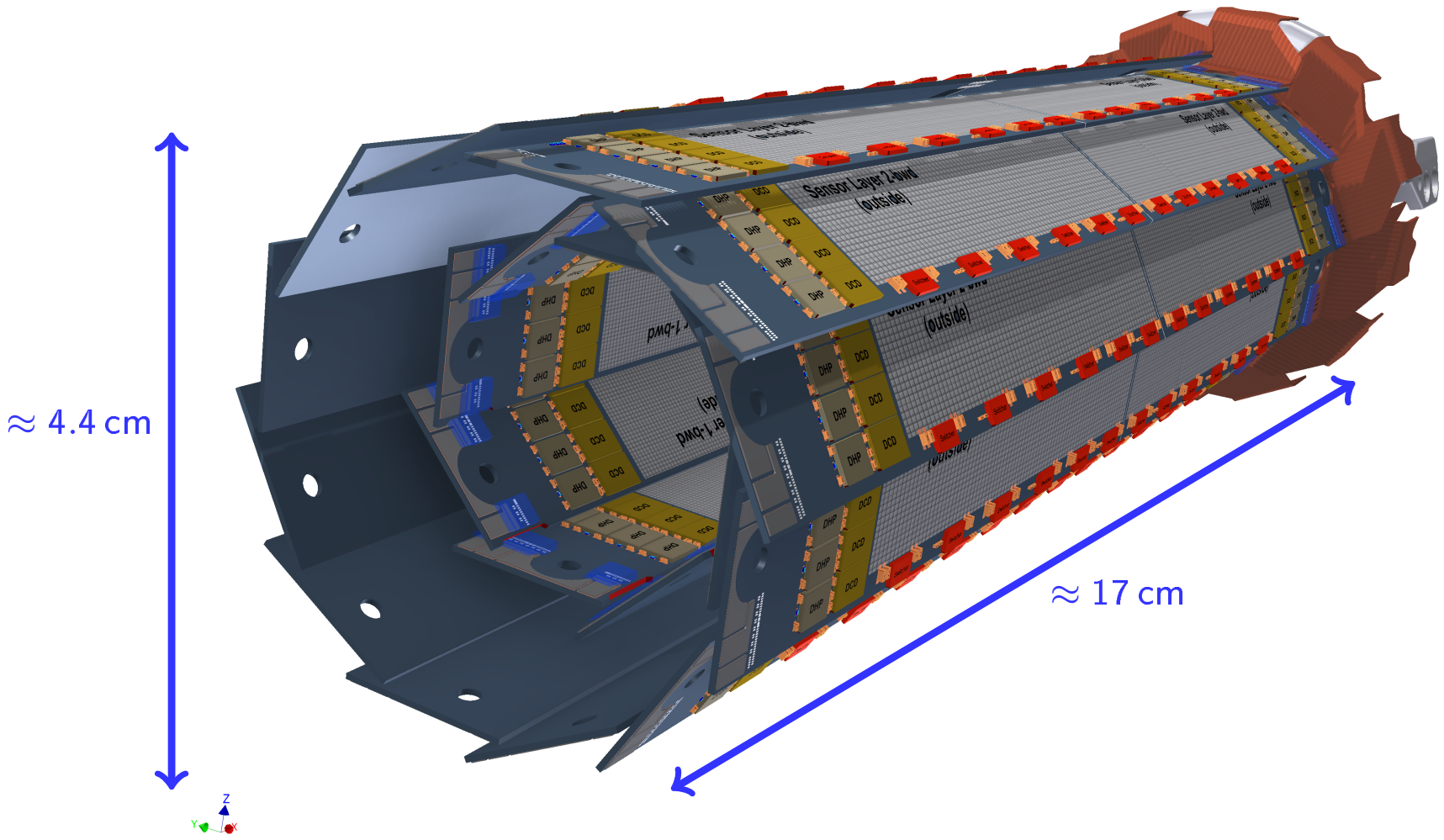
The Belle II Experiment

- *Pixel Detector*



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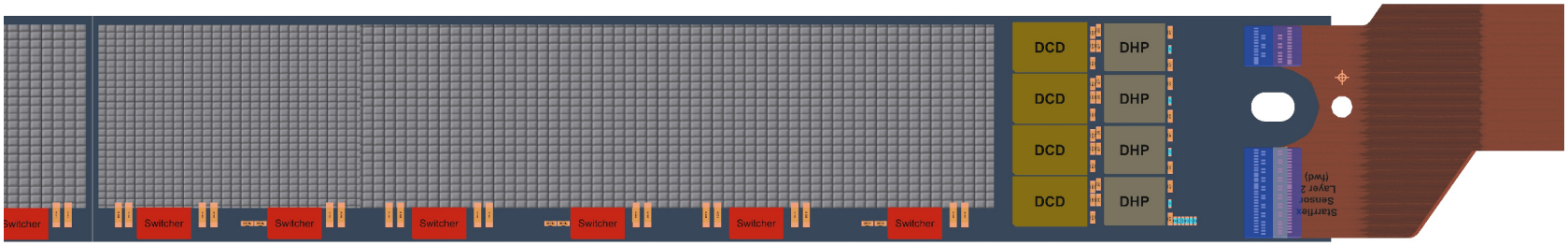
The Belle II Experiment
- *Pixel Detector*

One PXD half ladder



PXD

- Innermost Belle II detector, two layers at 14 mm and 22 mm around beam pipe
- Inner layer made up of 8, outer of 12 so called "ladders"
  - each ladder glued from two "half ladders", which are read out independently
  - sensitive area thinned down to 75 μm
  - each has 768 $\times$ 250 Pixel $\rightarrow$ in total $\sim$ 8 million Pixels
  - sounds not that much, every iPhone has as many pixels

  $\rightarrow$ **BUT**: readout time is 20μs leading to 50000 frames per second (iPhone 60fps)
- Each pixel based on DEPFET (DEPleted Field Effect Transistor) technology
- Improves vertex resolution by factor of 2 $\rightarrow$ 25 μm in beam direction

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Requirements for the Pixel Detector DAQ

Trigger and data rate estimation

- Belle II trigger rate 30kHz
- For the PXD we expect a maximum occupancy of 3%, most of it background
  - Synchrotron radiation
  - Beam gas scattering
  - Touscheck scattering
  - Radiative Bhabha scattering
  - Two γ processes (main background source)
- Given these background processes we expect a data rate of 20 GB/s
  - 10 times more than all other Belle II subdetectors

Requirements for the PXD-DAQ

- Online data reduction of factor 30 by rejecting background events
- High bandwidth data transfer
- Parallel processing of events
  $\Rightarrow$ FPGA based DAQ platform implemented in the ATCA (Advanced Telecommunications Computing Architecture) standard

The PXD DAQ

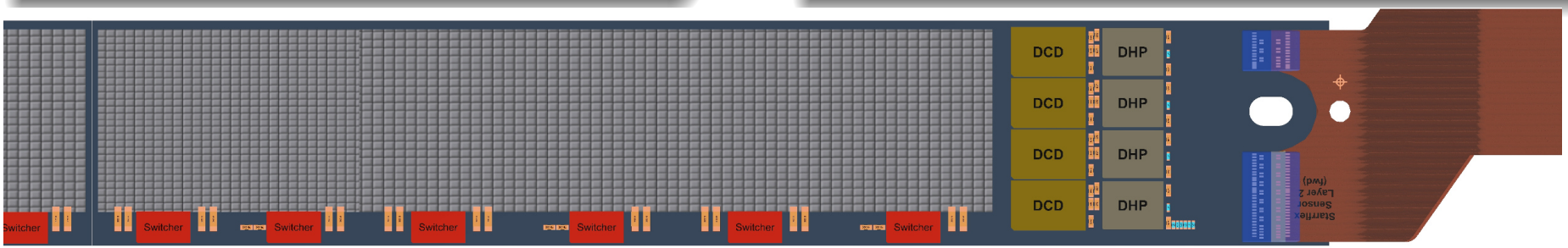
- the ASIC part, Front End Electronics

Selecting pixels - Switcher

- Gate and clear signal
- 32x2 channels
- Fast HV ramp to clear DEPFET

From current to digits - DCD

- Drain Current Digitizer
- 256 input channels with 8-bit ADC
- 50 ns sampling time



First framing - Data Handling Processor (DHP)

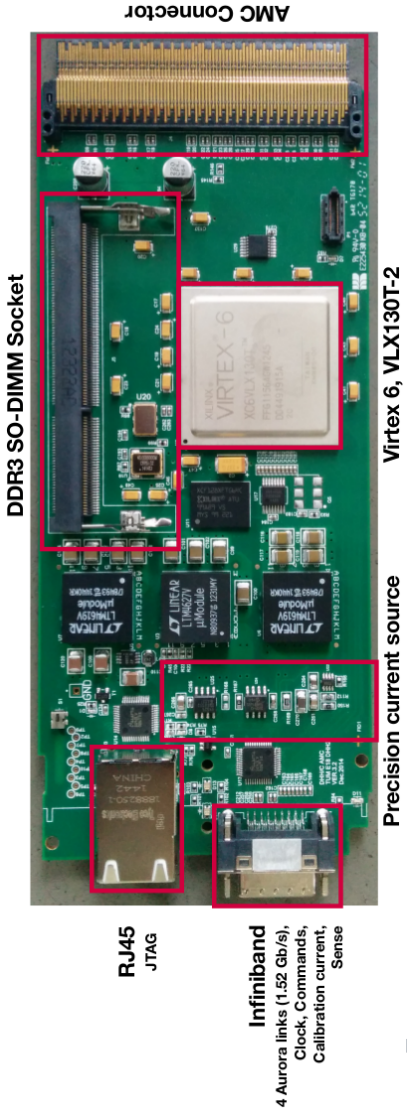
- Stores raw data and pedestals
- Performs zero suppression and pedestal correction
- First data formating

The PXD DAQ

- backend data handling - DHH

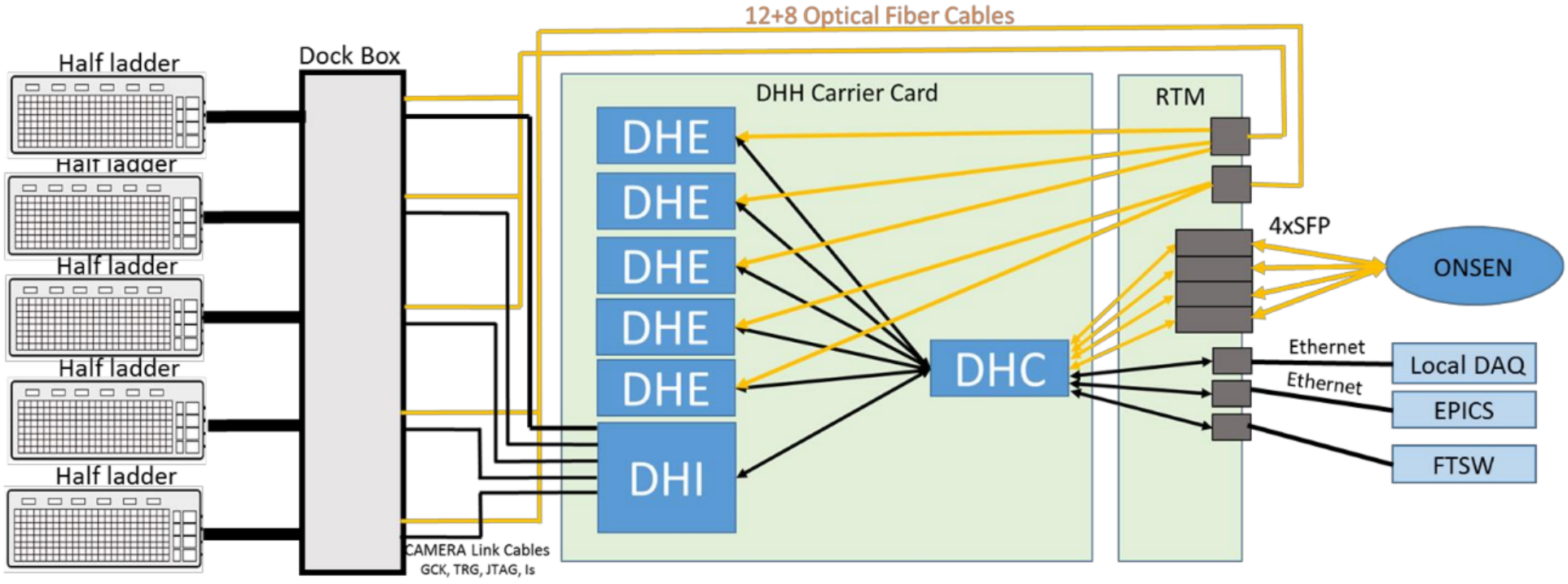
DHH - Data Handling Hub

- ATCA standard shelf
- Consists of
  - 8 carrier cards
  - 8 modules with Camera link (DHI) transmitting control signals like JTAG, command line, ...
  - 8 data combiner modules (DHC) trigger distribution, sub event building
  - 40 data receiver modules (DHE) receiving pixel data, 5 per DHC, ASIC control
- Xilinx Virtex 6 FPGA on all boards



The PXD DAQ

- *backend data handling - DHH*, dataflow



Schematic dataflow of 5 PXD half ladders combined in one DHC module.

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The PXD DAQ

- *selection of interesting events - ONSEN*

ONSEN Hardware - overview

- Developement in cooperation between IHEP Beijing and JLU Giessen
- ATCA shelf including:
  - 14 ATCA slots for carrier boards
  - Full Mesh backplane, communication of MGTs via AURORA
  - Power supply and cooling
- 9x Carrier Boards, each with a Power Supply Board and RTM (Rear Transition Module)
- 33x AMC daughter boards
- Board control via IPMI and dedicated daughter boards

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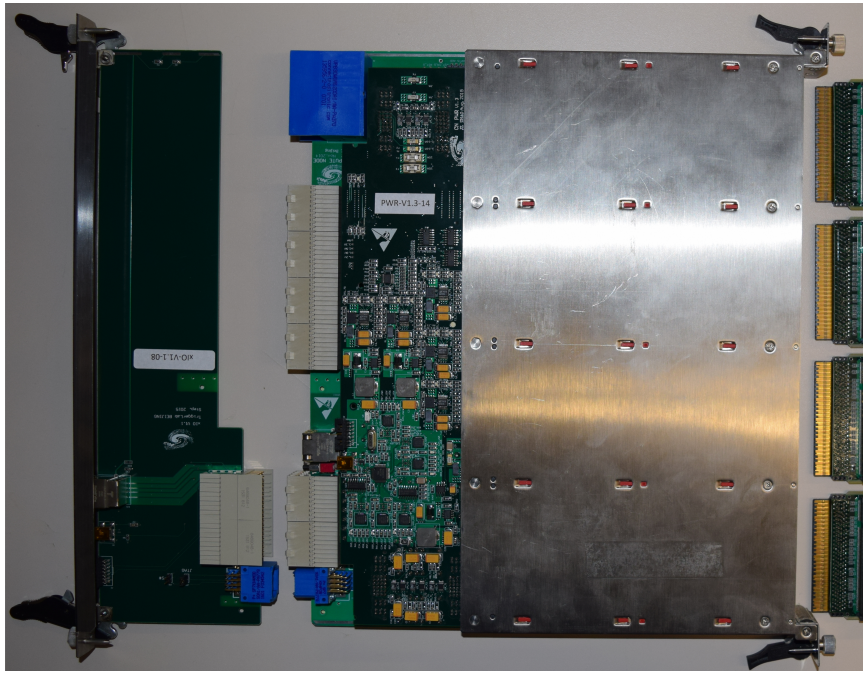
Chinese Academy of Sciences
JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

The PXD DAQ

- selection of interesting events - ONSEN

Carrier Board

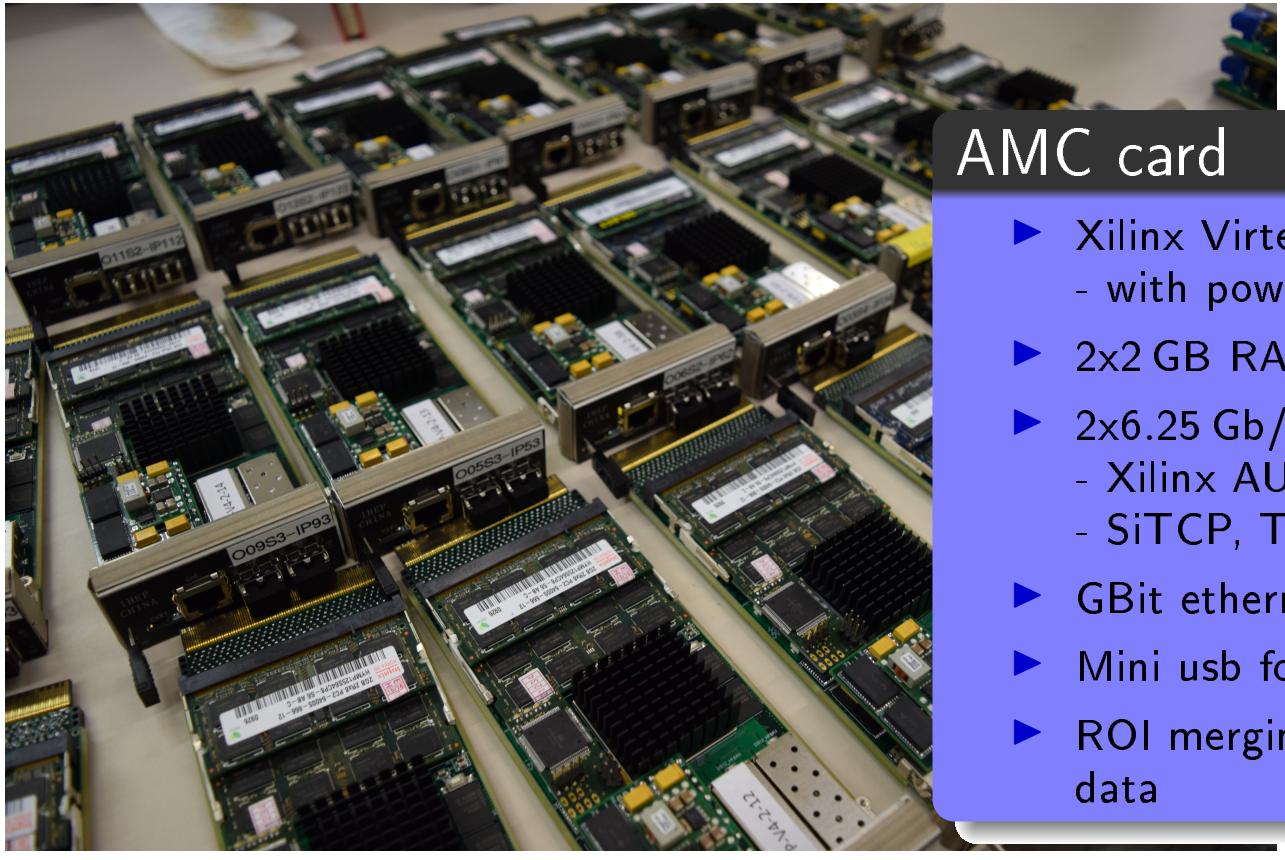
- Xilinx Virtex 4 FPGA
  - with power pc 405
- 4 AMC daughter card slots
- GBit ethernet for slow control
- Mini usb for serial access
- Data transfer between carrier boards via backplane MGT
- Data transfer to AMC cards via LVDS links



D. Getzkow

The PXD DAQ

- *selection of interesting events - ONSEN*



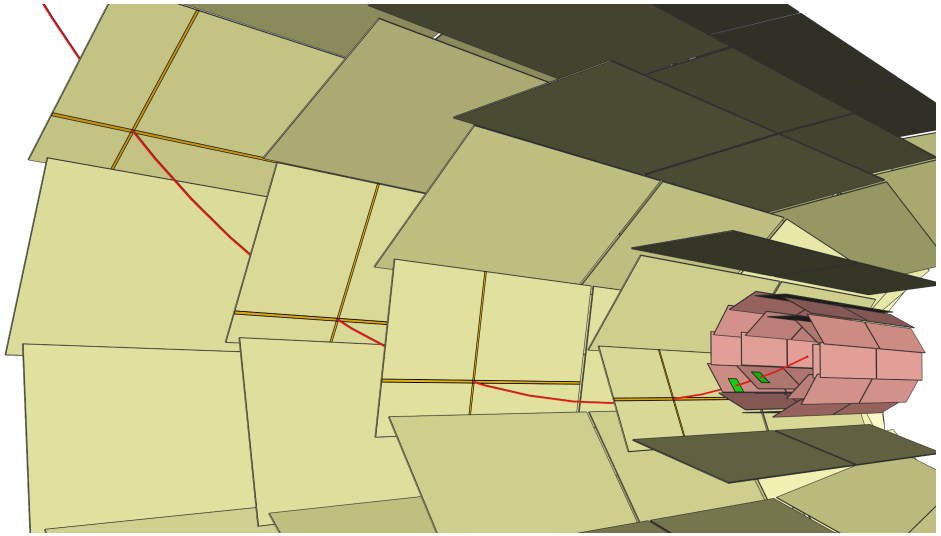
AMC card

- Xilinx Virtex 5 FPGA
  - with power pc 440
- 2x2 GB RAM, for Event storage
- 2x6.25 Gb/s SFP+ transceivers
  - Xilinx AURORA protocol (optical)
  - SiTCP, TCP implementation
- GBit ethernet for slow control
- Mini usb for serial access
- ROI merging and selection of DHC data

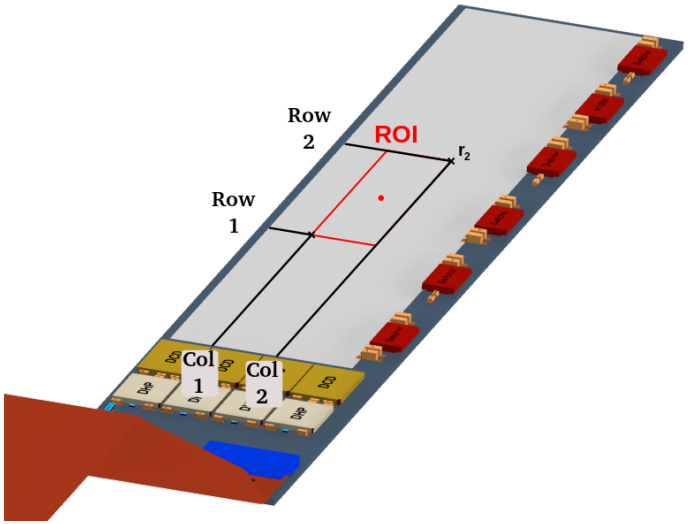
D. Getzkow

The PXD DAQ

- calculating ROIs - DATCON & HLT



Particle trajectory, originating from a physically interesting event near the interaction point (red). The green areas on the detector surface of the PXD illustrate a **R**egion **O**f **I**nterest ROI.

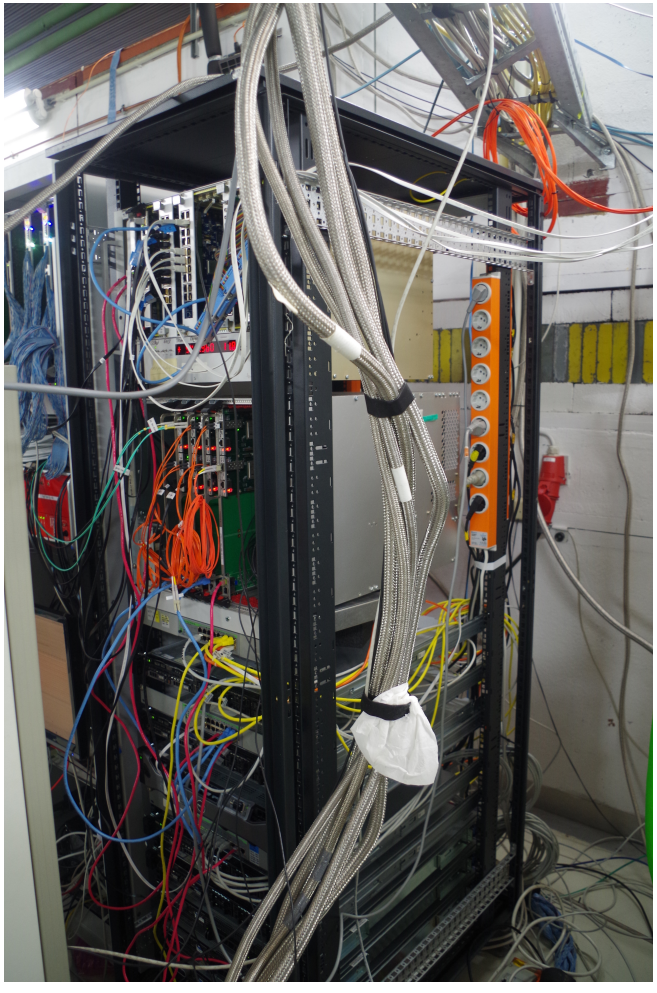


ROI on the PXD sensor surface.

The PXD DAQ
- calculating ROIs - HLT

HLT - Software Tracking

- High Level Trigger
- CPU farm processing data of all Belle II sub-detectors except PXD
- Performs event selection, no HLT trigger $\Rightarrow$ event rejected
  $\Rightarrow$ data reduction by factor of 3
- Picture shows the HLT setup at testbeam - not the full system



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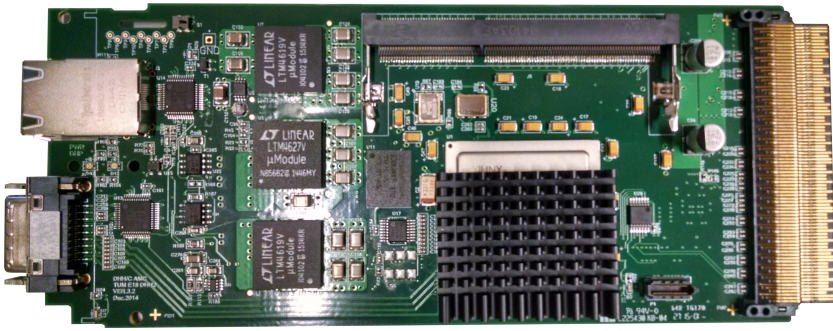
The PXD DAQ
- calculating ROIs - DATCON

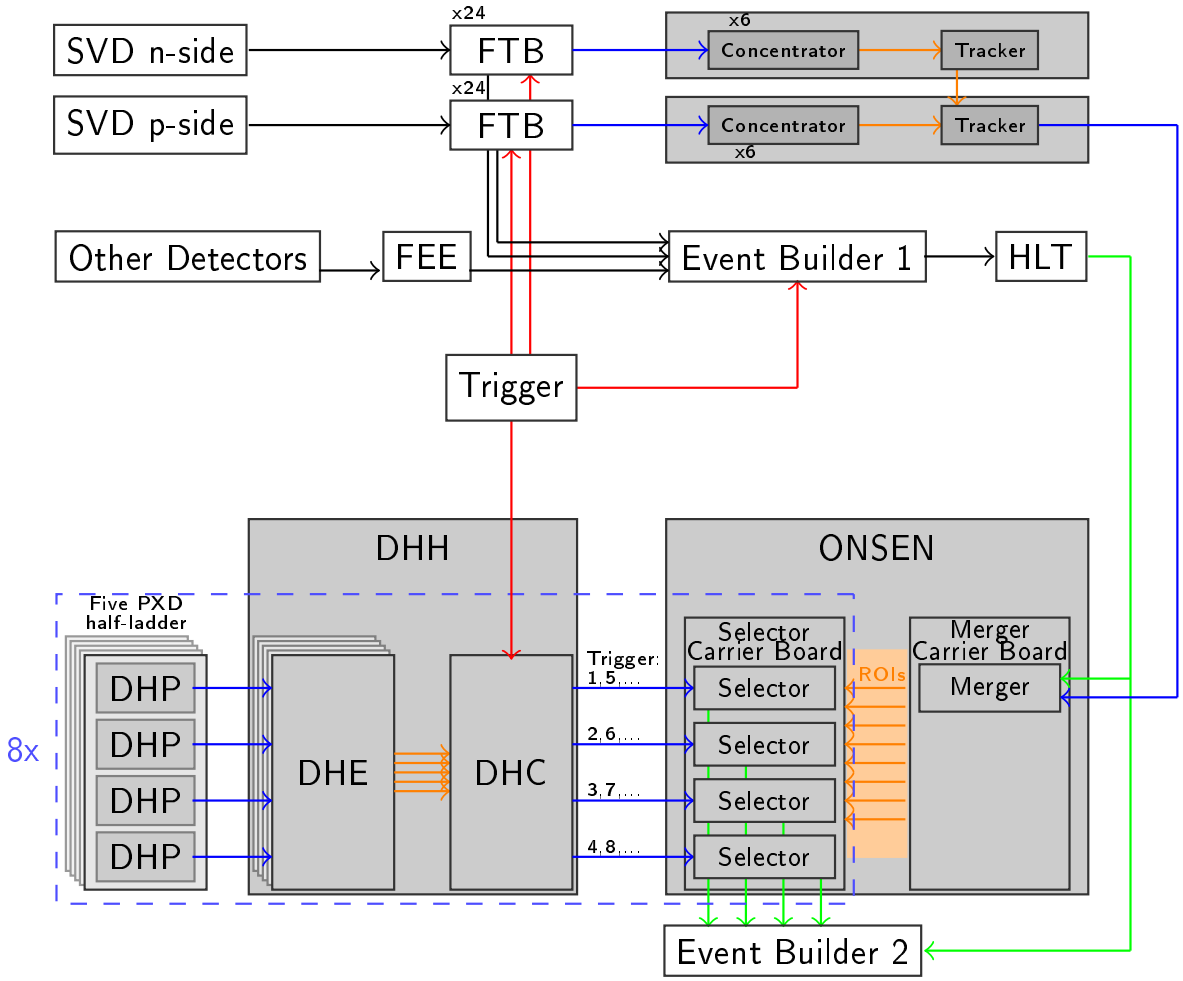
DATCON - Hardware Tracking

- Data Acquisition Tracking Concentrator Online Node
- 2 x 9-slot μTCA shelfs
- 12 concentrator boards
  - AMC boards with Xilinx Virtex 5 FPGA
  - 4 sfp cages, GTP transceivers
  - receive data from SVD
- 2 tracker boards
  - Equipped with Xilinx Virtex 6 FPGA
  - Infiniband connector, GTX transceivers
  - Perform online tracking
  - Hough and conformal transformation
- Picture shows the DATCON setup at testbeam - not the full system



The PXD DAQ

- putting stuff together...



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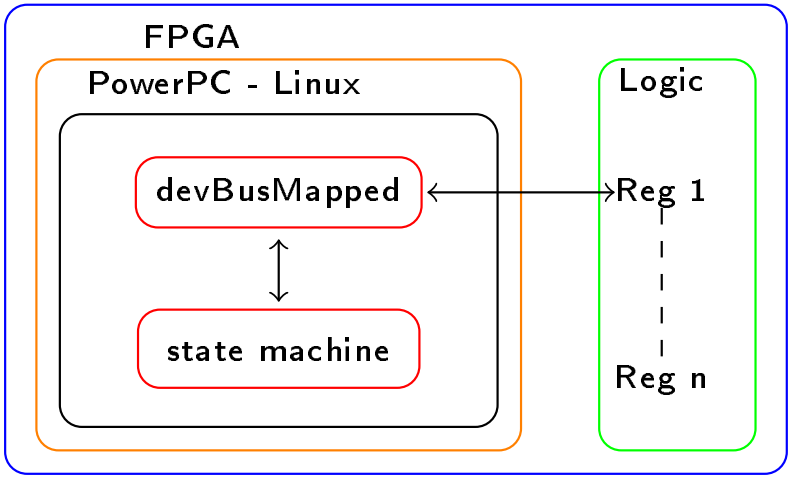
The Slow Control System
- EPICS & CSS

EPICS

- Slow control software
- Control via IOCs (Input Output Controller)
- PVs (Process Variables) are connected with registers on the hardware
- PVs are defined in database file loaded and accessible by IOC



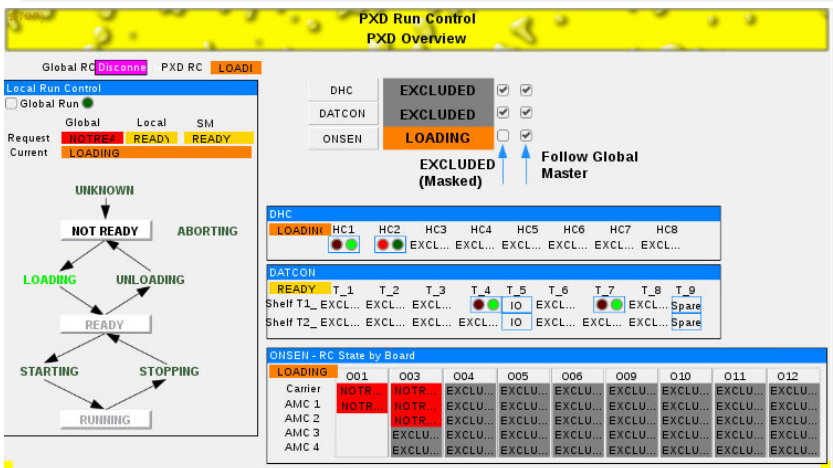
Example of an EPICS IOC with register control.

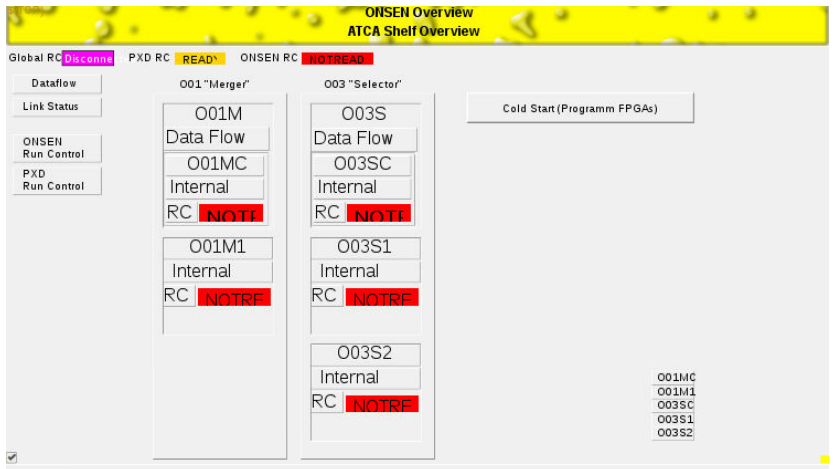
The Slow Control System

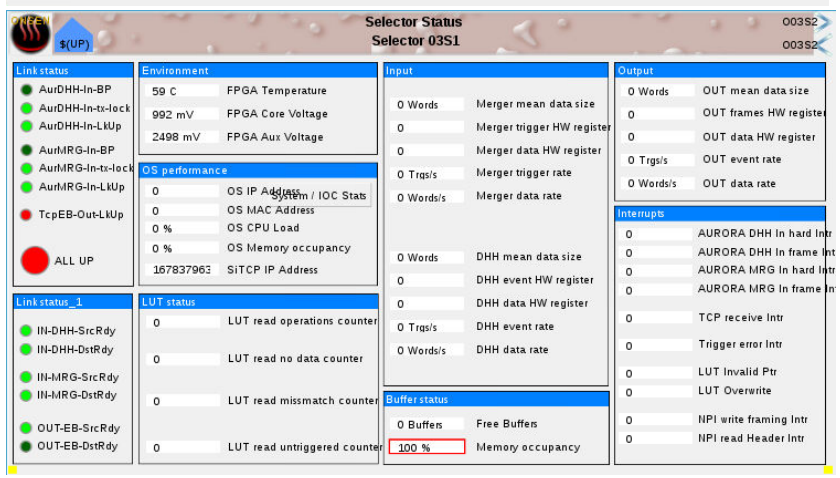
- *EPICS & CSS, schematic flow of run control*

CSS

- GUI reflecting the Status of the system
- Can be used for monitoring and interacting
- Provides alarm system for shifters







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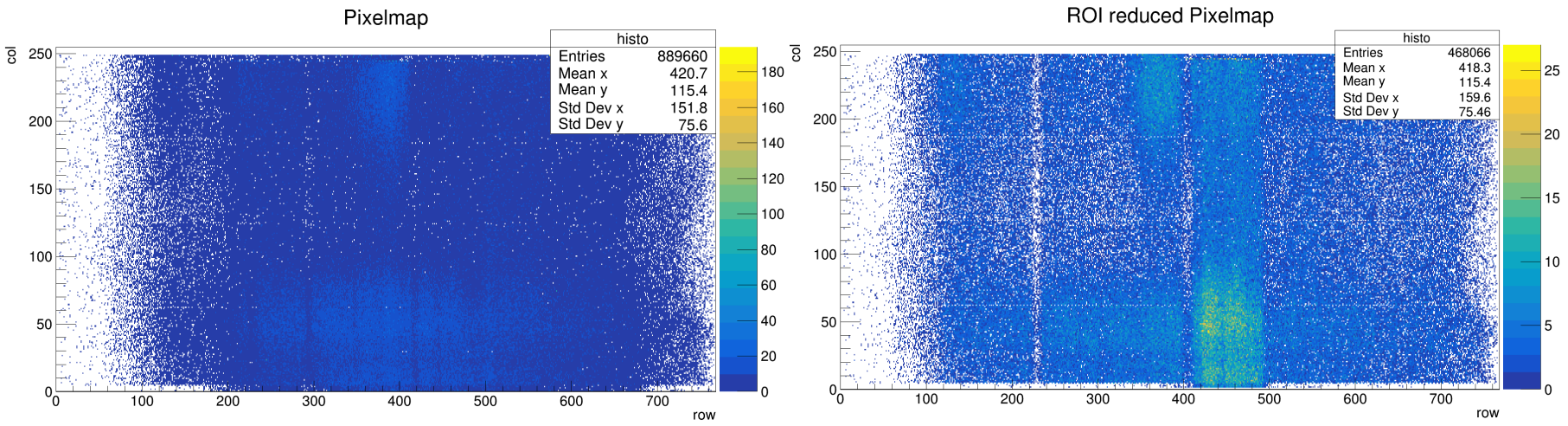
Results from Beam Test at DESY

- achievements during 2016/2017 test beam campaign

Beam test performed with ...

- Full DAQ chain with 2 PXD half ladders and 4 SVD modules
- Final hardware of ONSEN system
- Tracking with three HLT cores
- Multiple ROIs per PXD layer
- Two DHC Streams $\rightarrow$ 2 ROI selectors
- All controlled by global run and slow control
- Live Data Quality Monitoring on CSS
- More than 10^9 events recorded
- Overnight runs for stability tests
- Tested with up to 4.1 kHz (limited by beam structure)

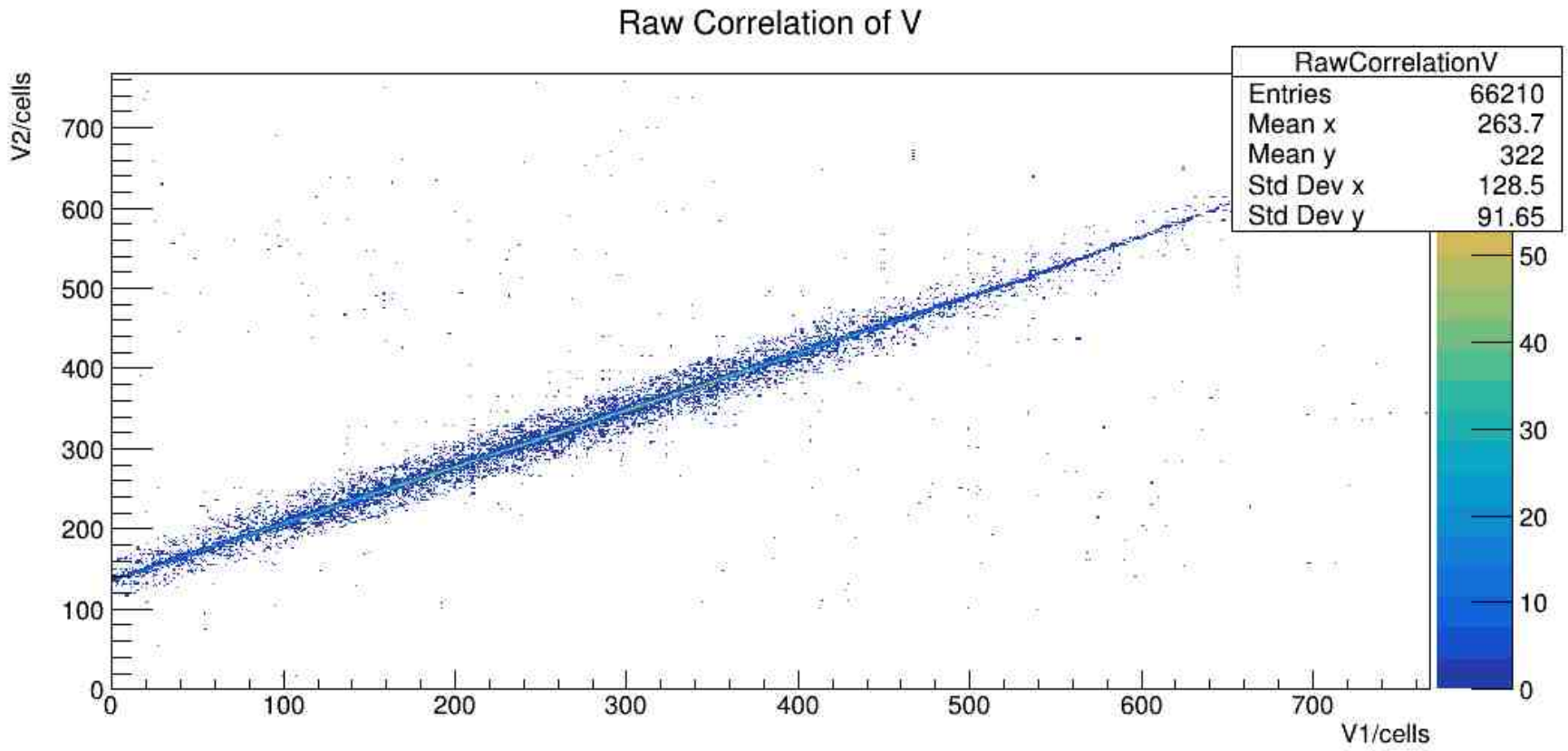
Results from Beam Test at DESY
- *ROI reduction*



If you look at the numbers → ROI reduction ≈ 2 because of ROI expansion due to remapping problem.
Picture from April 2016 testbeam, ongoing campaign has implemented remapping and hopefully a better reduction.

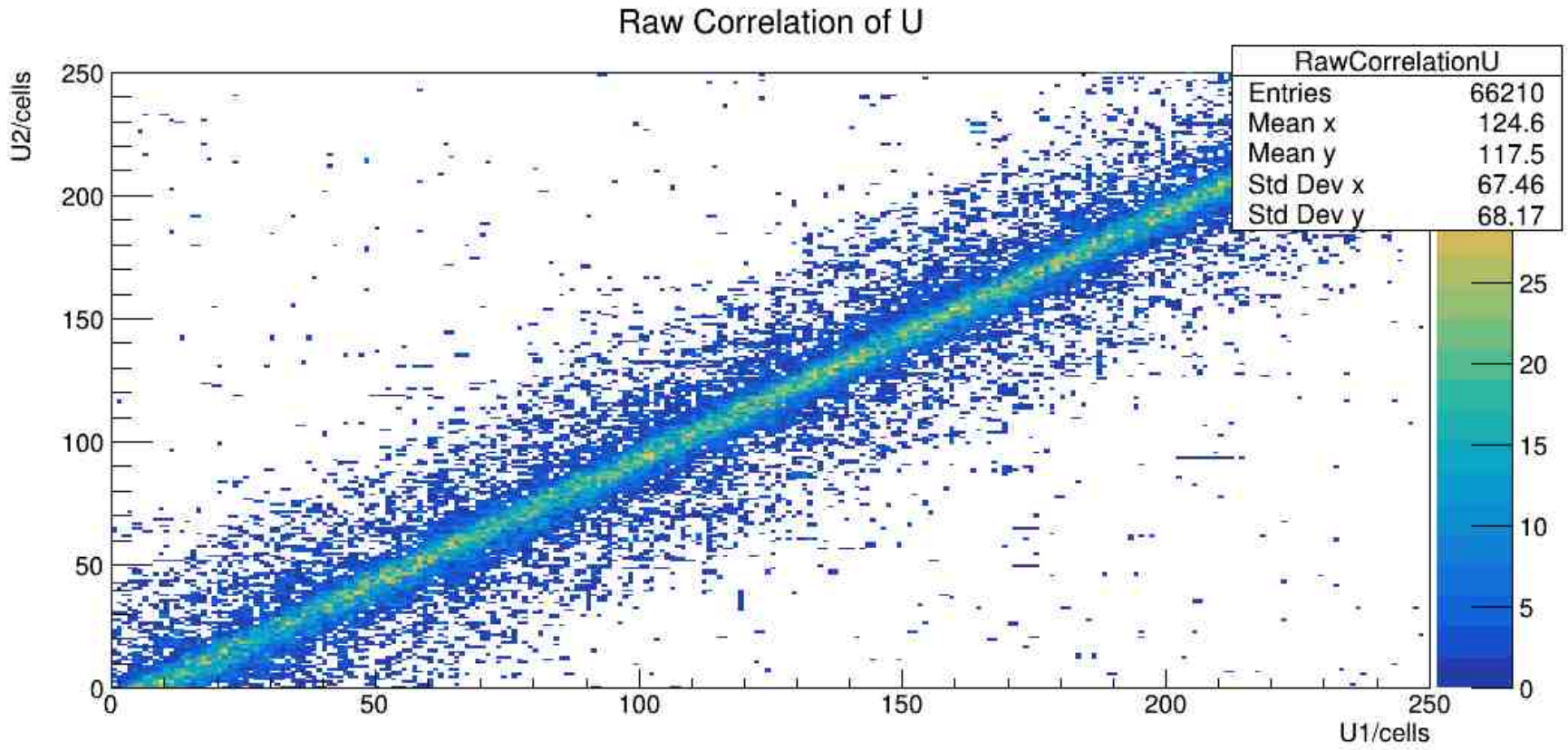
Results from Beam Test at DESY

- correlation of inner and outer layer in row direction



Results from Beam Test at DESY

- correlation of inner and outer layer in column direction



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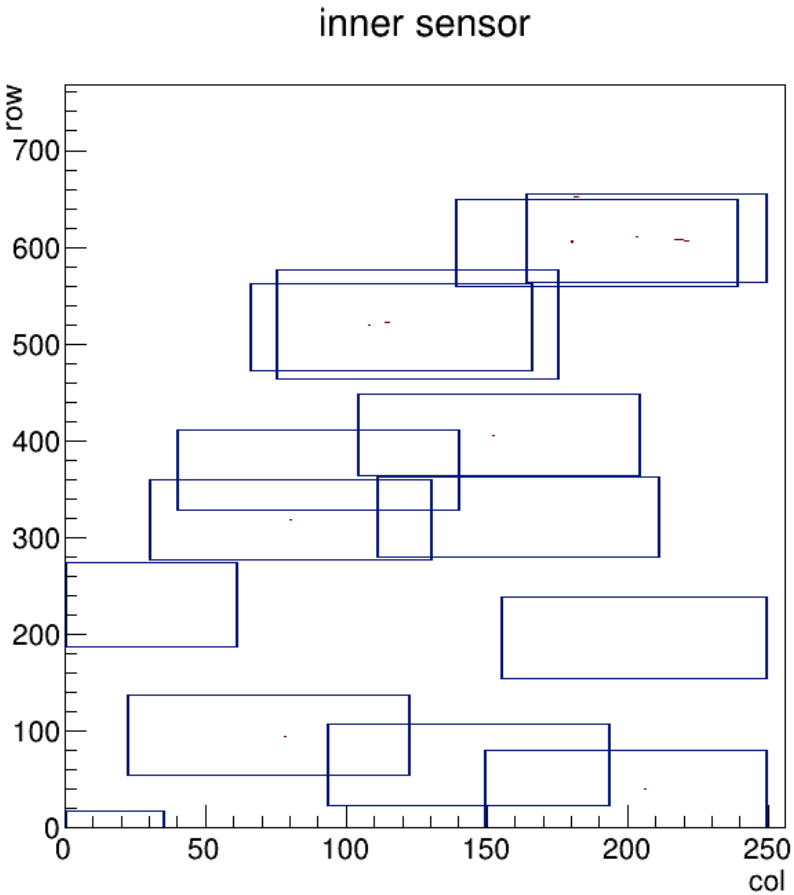
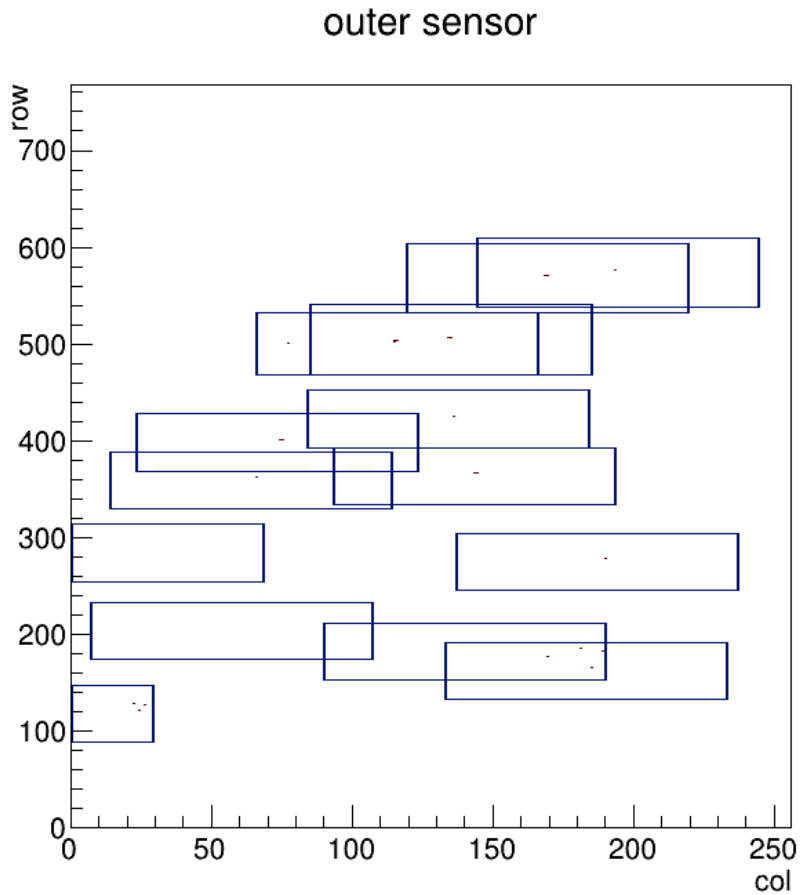
Results from Beam Test at DESY

- *Pixel in ROIs*





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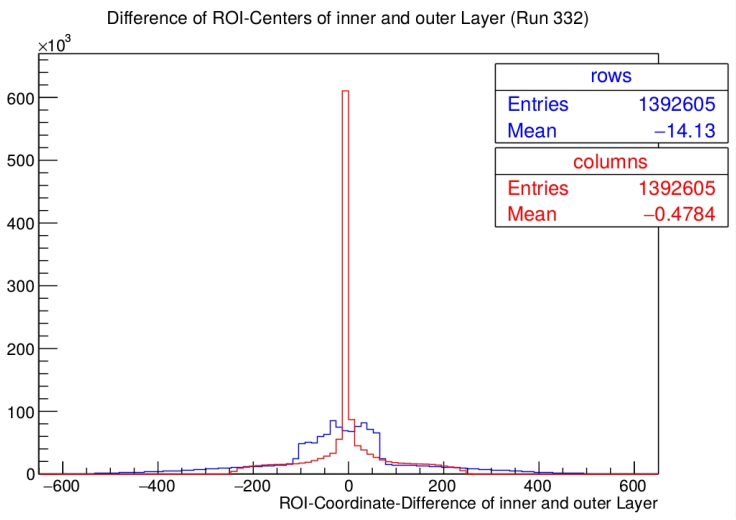
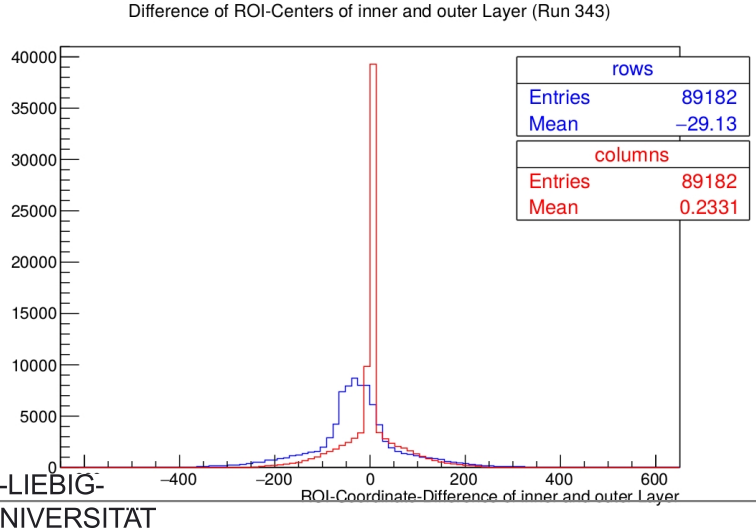
Results from Beam Test at DESY

- *correlation of ROIs*

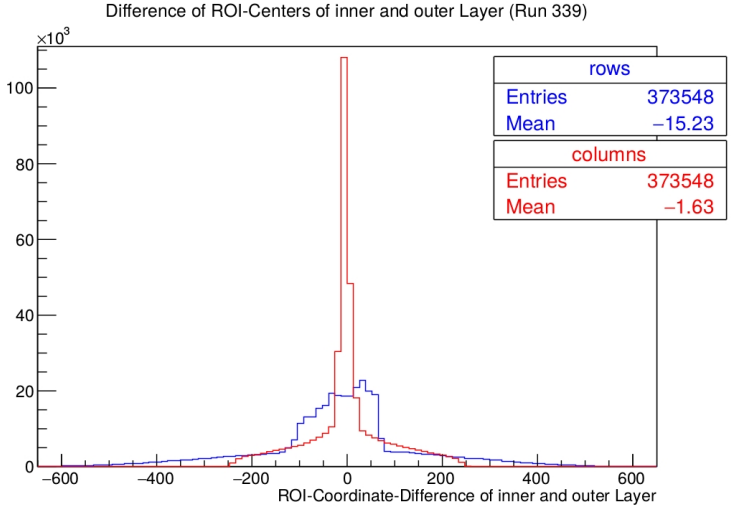
no secondary target - field on



no secondary target - field off



lead target - field on



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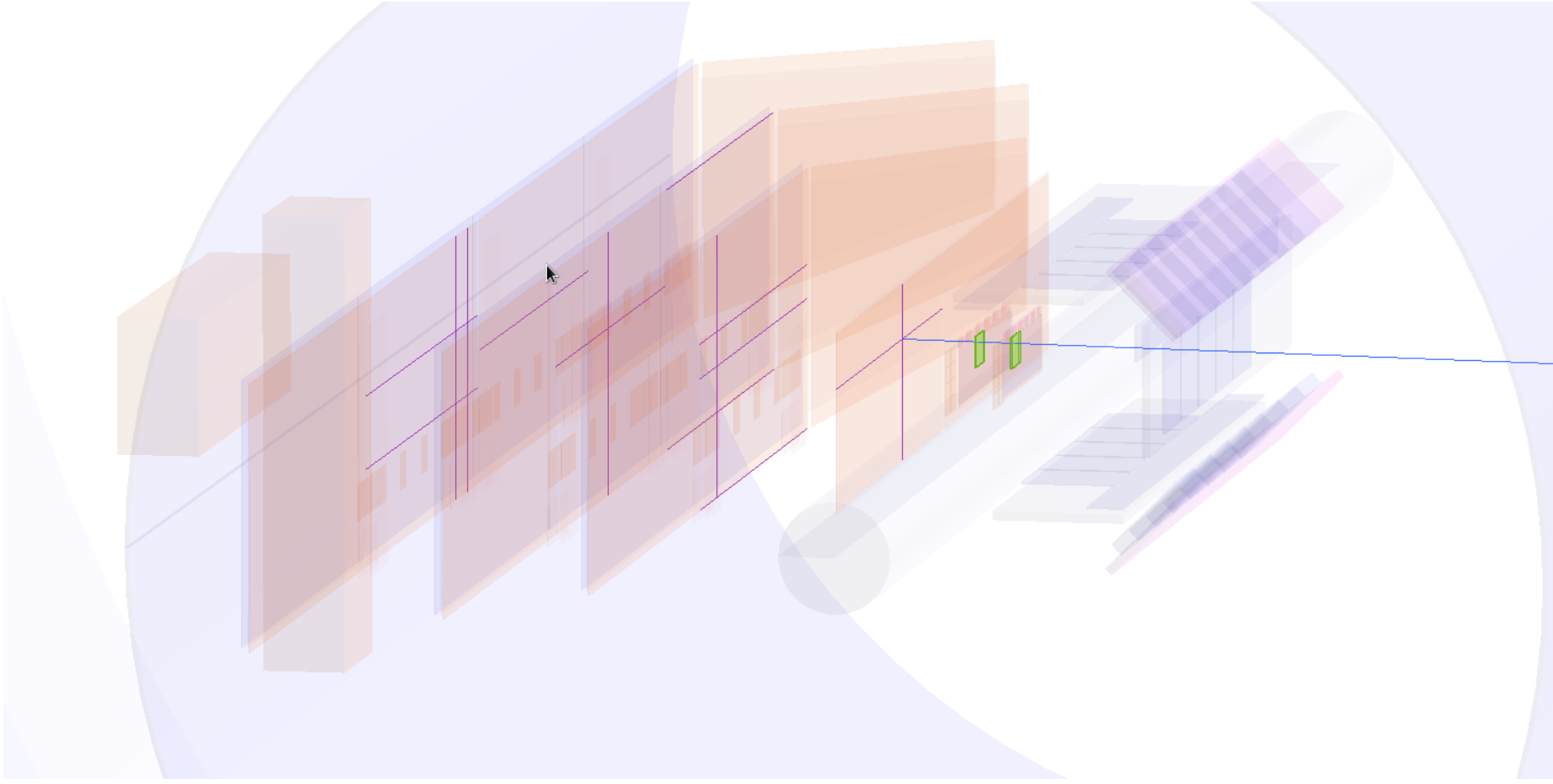
Results from Beam Test at DESY

- track in the event display



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Thank you for your attention

Спасибо за внимание