Phase I Upgrade of the CMS Pixel Detector

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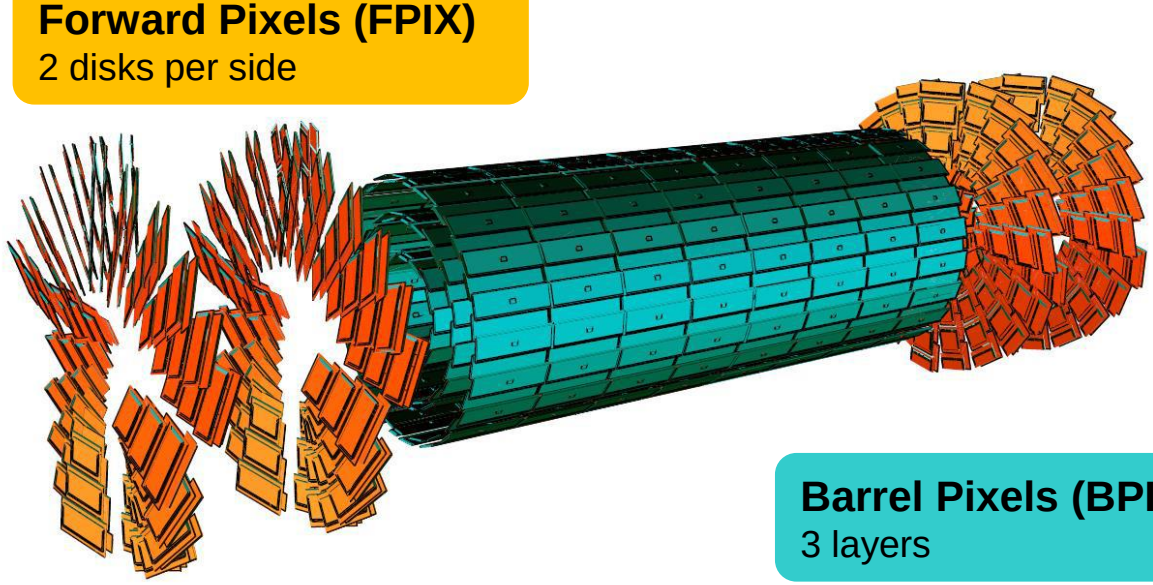
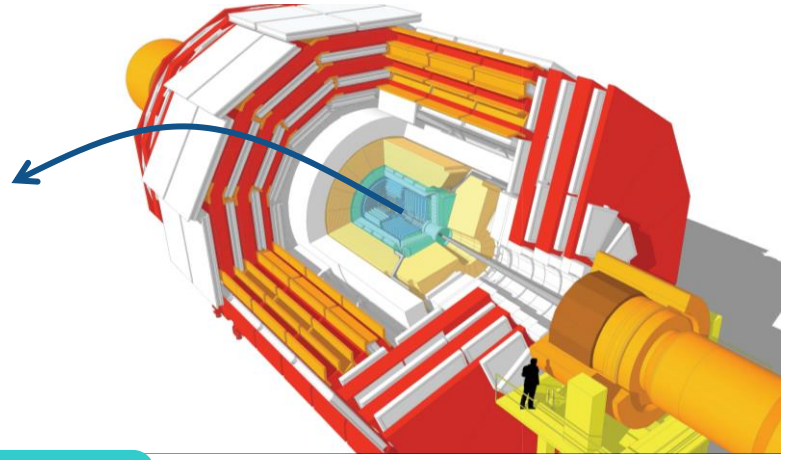
The CMS Phase 0 Pixel Detector

Forward Pixels (FPIX)
2 disks per side





Barrel Pixels (BPIX)
3 layers

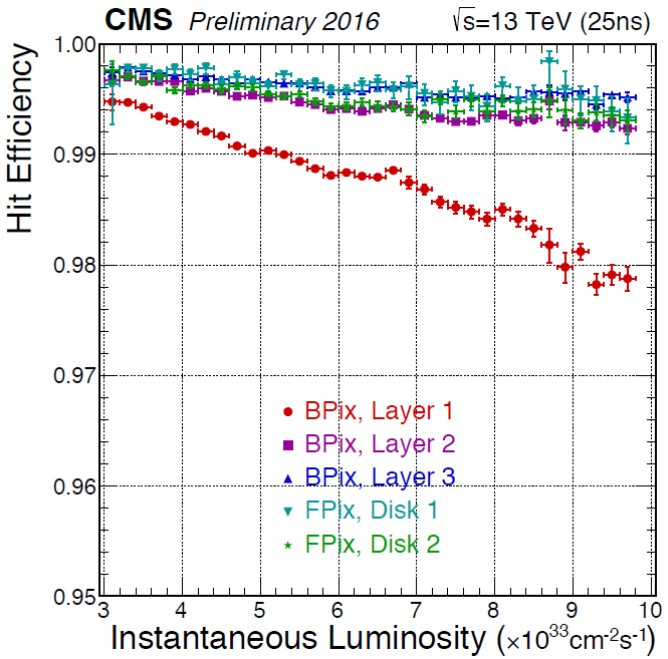
- In total **66 million pixels**
  - n+-in-n sensor, pixel size of 100x150 µm
- Resolution: 10 µm in rφ, 20-40 µm in z
- Designed for $\mathcal{L}_{inst}$= 1 · 10^{34} $cm^{-2}s^{-1}$ and 25ns bunch spacing

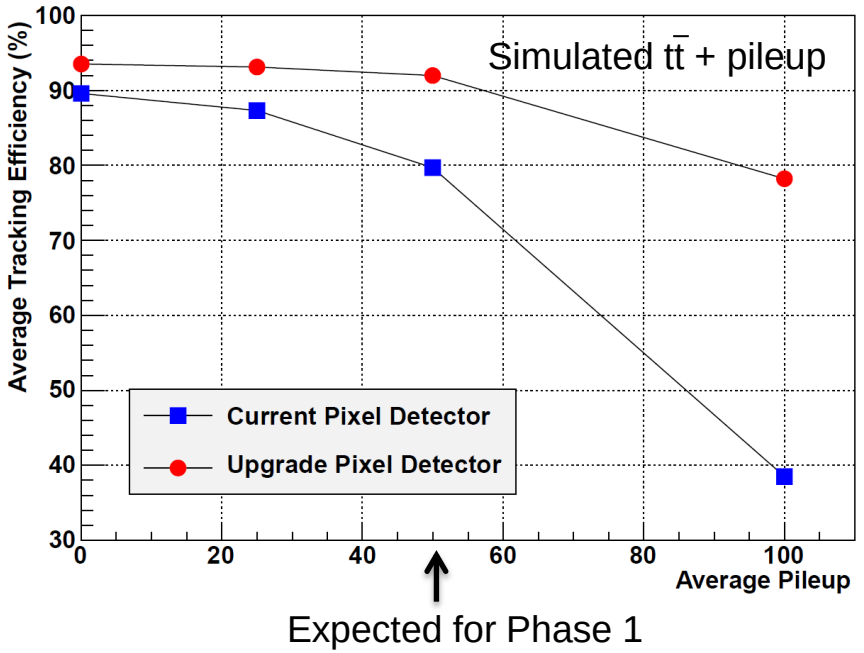
Motivation for the Pixel Upgrade

- Current pixel detector specified for LHC **design luminosity of 1· 10^{34} $cm^{-2}s^{-1}$**
- LHC planning: **~ 2· 10^{34} $cm^{-2}s^{-1}$** between 2015 and 2018
  - Up to **50 events per bunch crossing** (pileup) and hit rates of ≈600 MHz/cm2

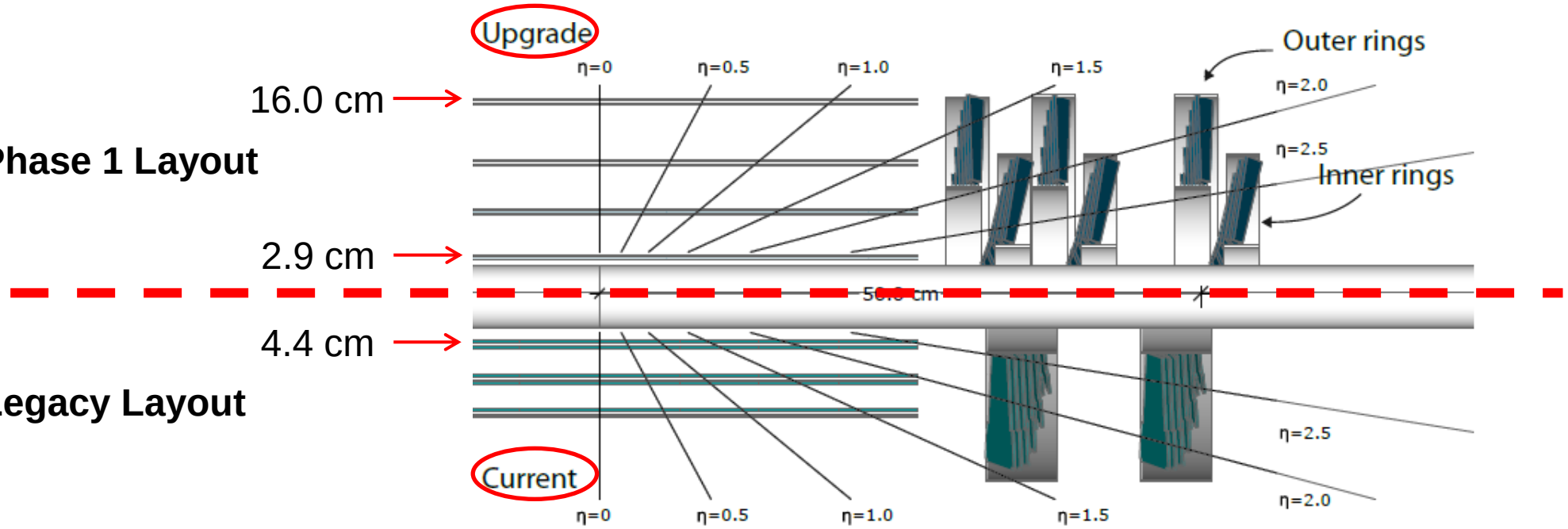
- Dynamic inefficiencies due to limited readout bandwidth
- Low redundancy (3 layers) have impact on tracking efficiency and fake rate

→ replacement of pixel detector during extended year-end technical stop (EYETS) in 2017



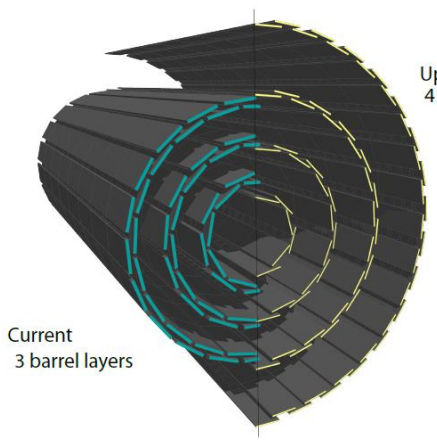


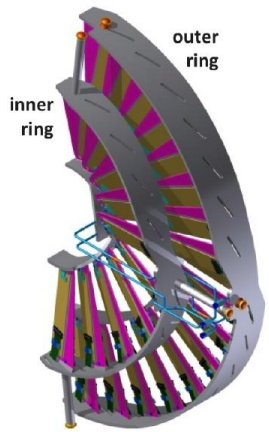
Phase 1 Pixel Detector Design



Phase 1 detector:

- 1 additional layer in barrel & endcap
  - Factor 1.9 more channels (124 Mill.)
- Reduced material budget (≈25 kg → ≈14 kg)
  - 2-phase CO_2 cooling
  - Lightweight support structure
  - Relocation of services



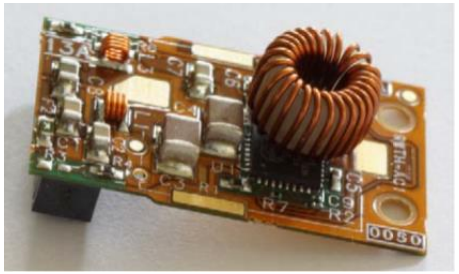


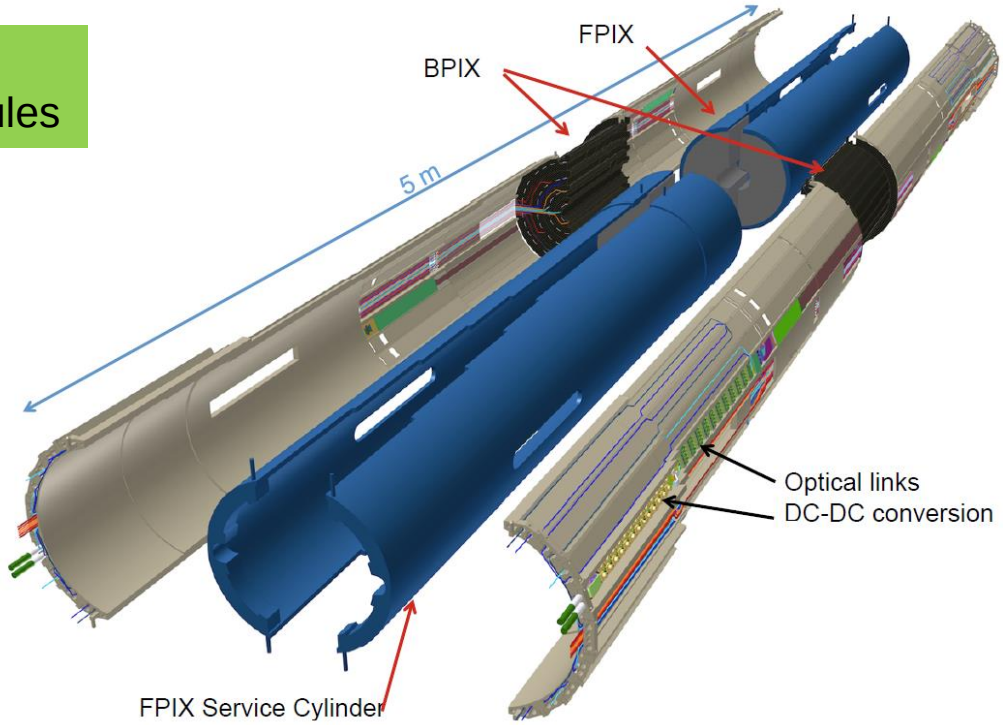
Novel Powering Scheme

Reuse existing cables and power supplies with **factor 1.9 more channels**
→ Factor 4 larger losses on the cables
→ Need a new powering scheme using **DC-DC converters**

Power supply	U=10 V, 50 m	DC-DC converter	U≈3.3 V, 2 m	Pixel modules

- Conversion ratio 3 – 4
- Cable losses reduced by factor 10





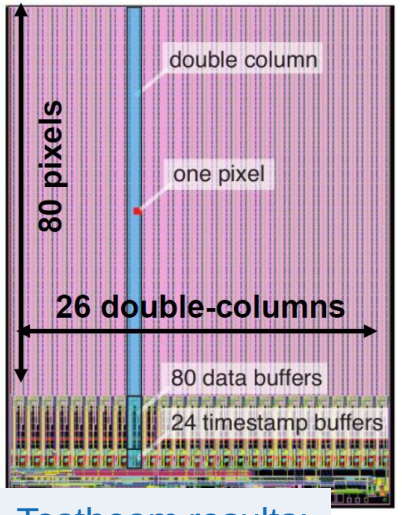
1200 DC-DC converters in total, custom development:
- Radiation hard ASIC (FEAST2 by CERN)
- Air core inductor for operating in magnetic field

Phase 1 Readout Chips

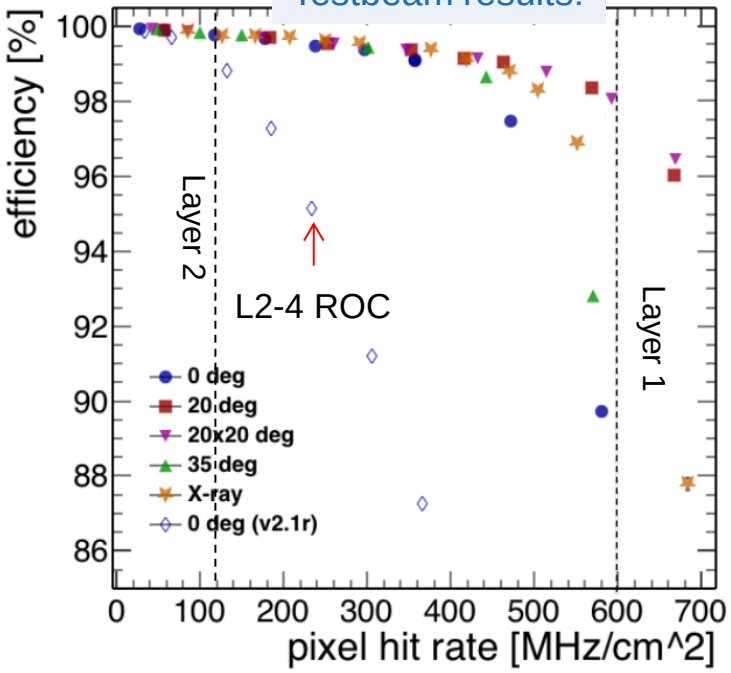
Psi46dig: evolution of psi46, for BPIX layers 2-4 & FPIX
→ „Column Drain“ architecture

- 40 MHz analog readout → 160 Mbit/s digital
- Increase of hit (32 → 80) & time stamp (12 → 24) buffer depth
- Additional readout buffer
- Reduced cross-talk → minimal threshold reduced from ~3200 e to ~ 1500 e

→ Improved rate capability & resolution



Testbeam results:



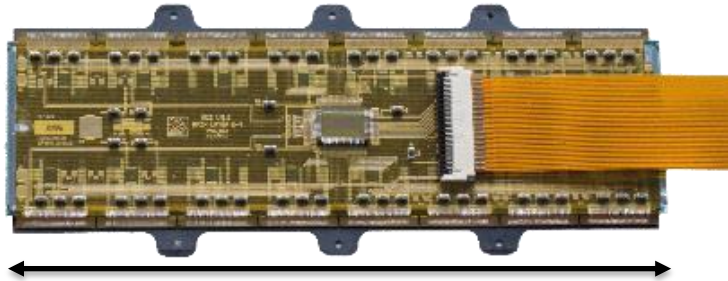
PROC600: new chip designed for BPIX layer 1
→ „Dynamic Cluster Column Drain“ architecture

- Readout of 2x2 clusters instead of single pixels
- Allows up to 7 pending column readouts
- Buffers not reset after readout

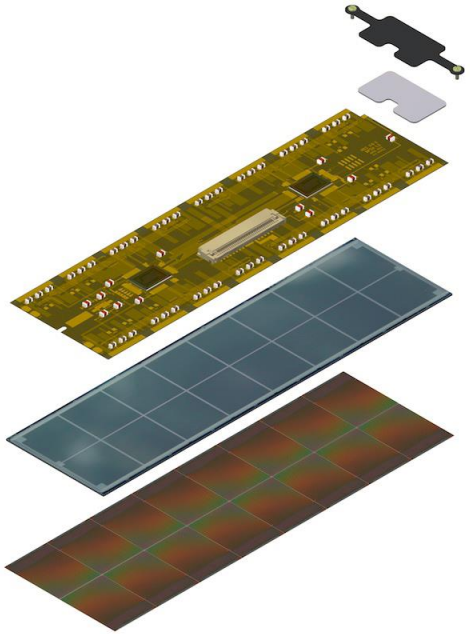
→ 97.5% efficiency at 600 MHz/cm²

Pixel Modules

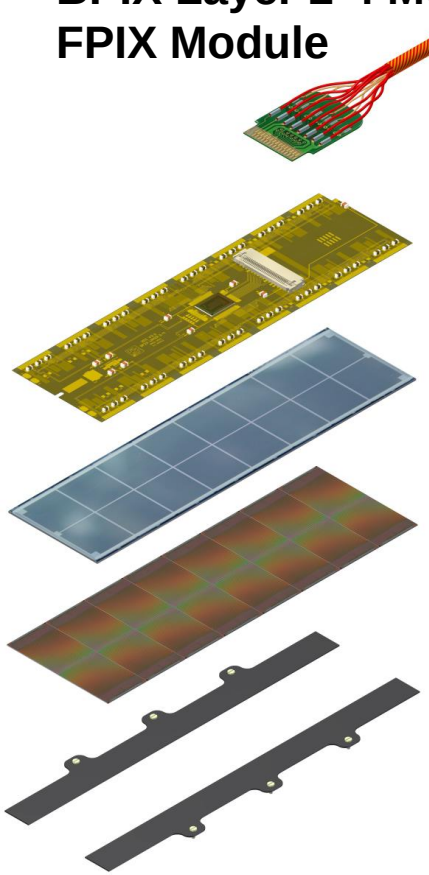
Evolutionary upgrade: Module concept and sensor design unchanged



BPIX Layer 1 Module



BPIX Layer 2-4 Module
FPIX Module



High Density Interconnect (HDI)
1 or 2 Token Bit Manager chips

n+-in-n silicon sensor
66 560 pixels

16 readout chips (ROCs)
psi46dig & PROC600 (BPIX Layer 1)
Bump-bonded to sensor

Si_3N_4 base-strips

Module Production

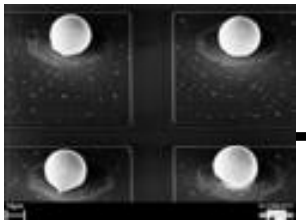
- Modules are produced in a distributed scheme
- A variety of bump-bonding vendors and technologies

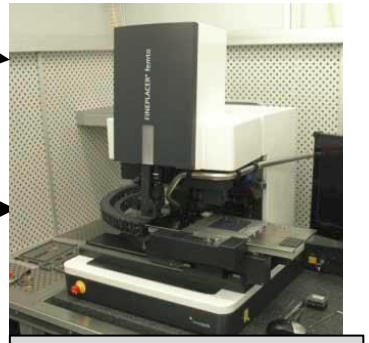
L1 + L2: Switzerland
L3: CERN/Finland/Taiwan/Italy
L4: Germany
FPIX: USA

Example KIT/RWTH:

Sensor production (CiS)

Processing, testing (PacTech)

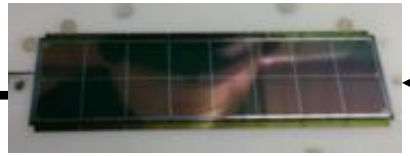


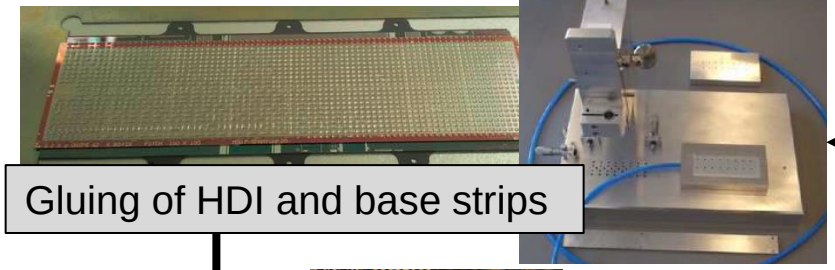


ROC production (IBM)
Wafer testing (PSI)

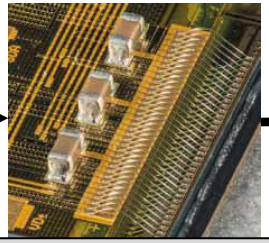
Processing (RTI)

Flip chip process
Bare module test

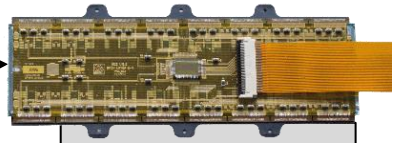




Gluing of HDI and base strips



Wire bonding



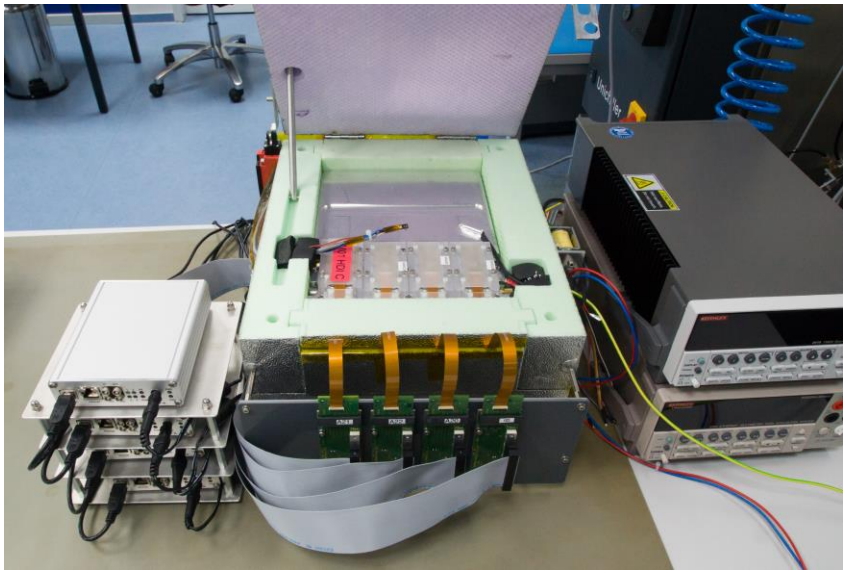
Electrical test
Shipping

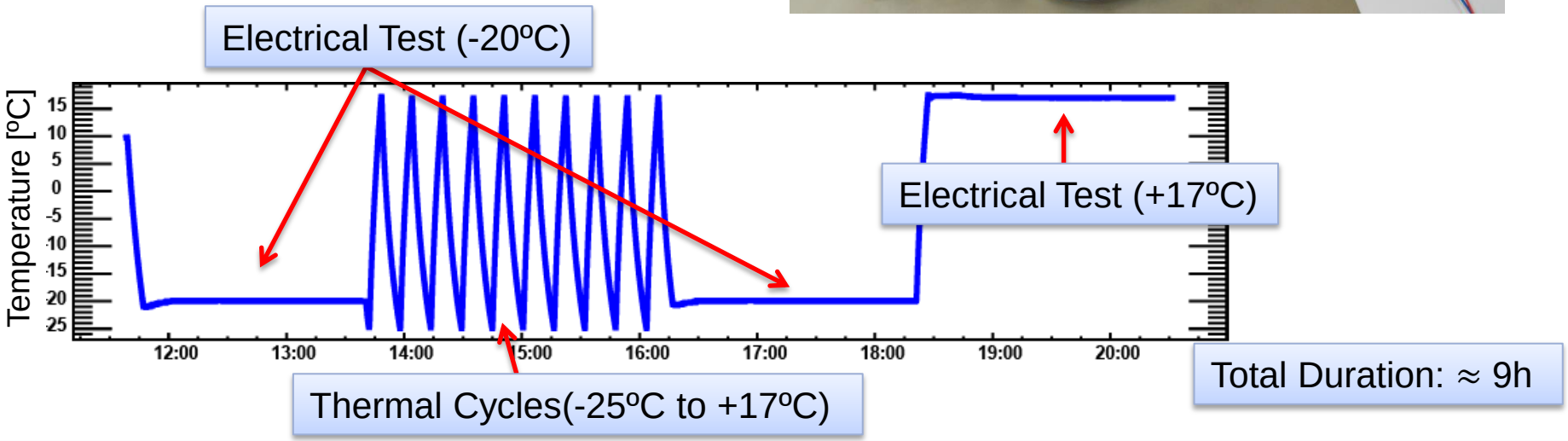
Qualification
Cold test, X-ray test

Common test procedures and software used among all centers:

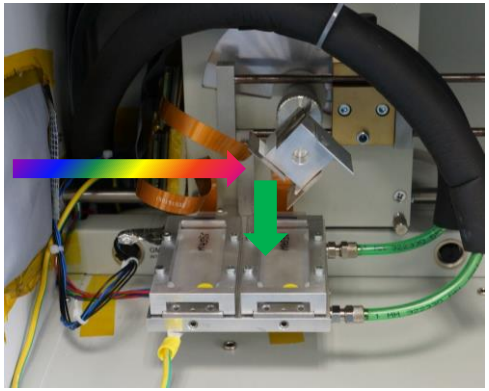
Cold Qualification:

- IV curve measurement and electrical test at +17ºC and at -20ºC
- 10 thermal cycles as stress test



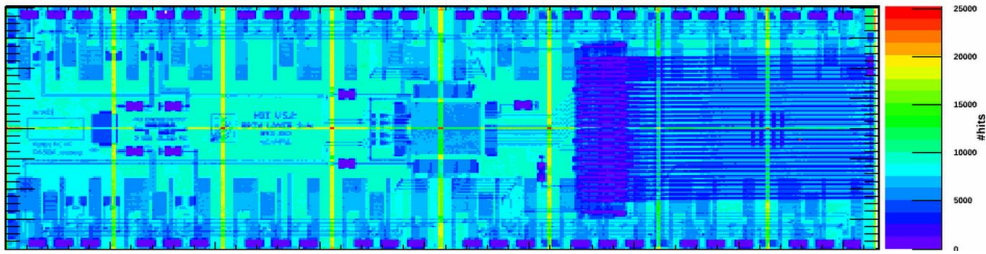


Module Qualification (BPIX)

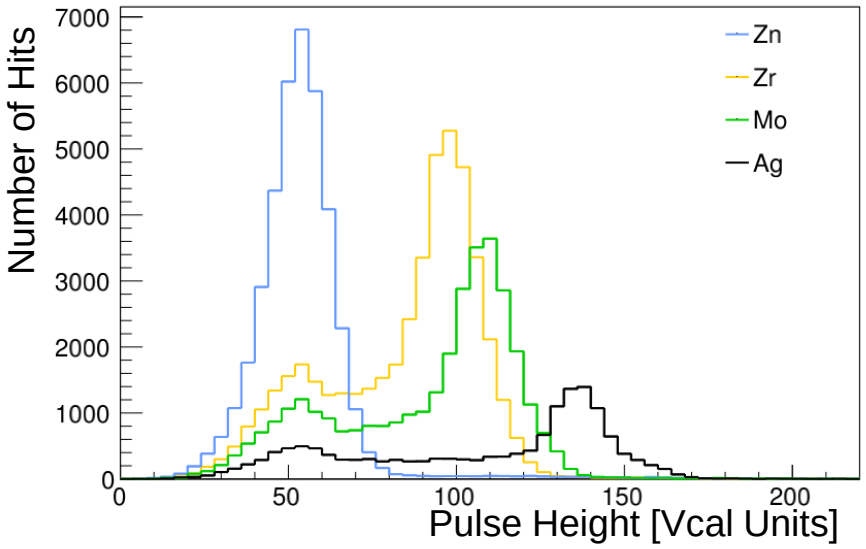


X-ray Qualification:

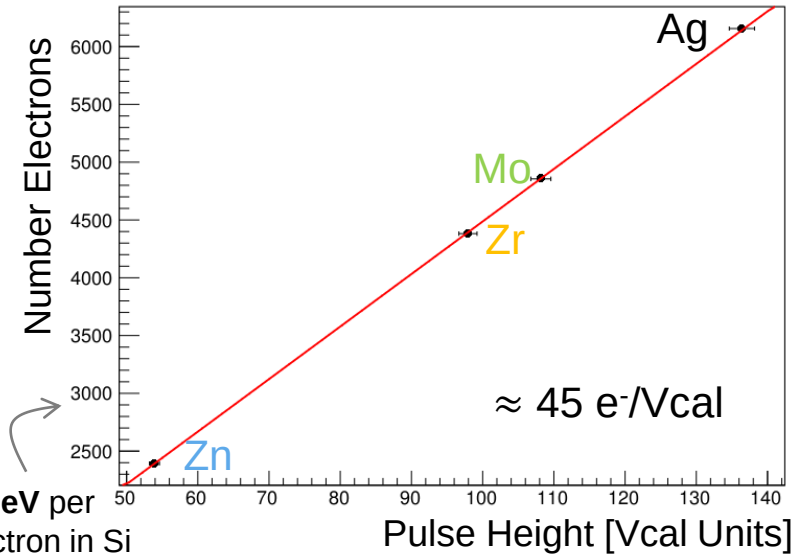
- Energy calibration with fluorescence lines
- High rate tests with X-ray hit rates up to 150 MHz/cm²



Pulse Height Spectra



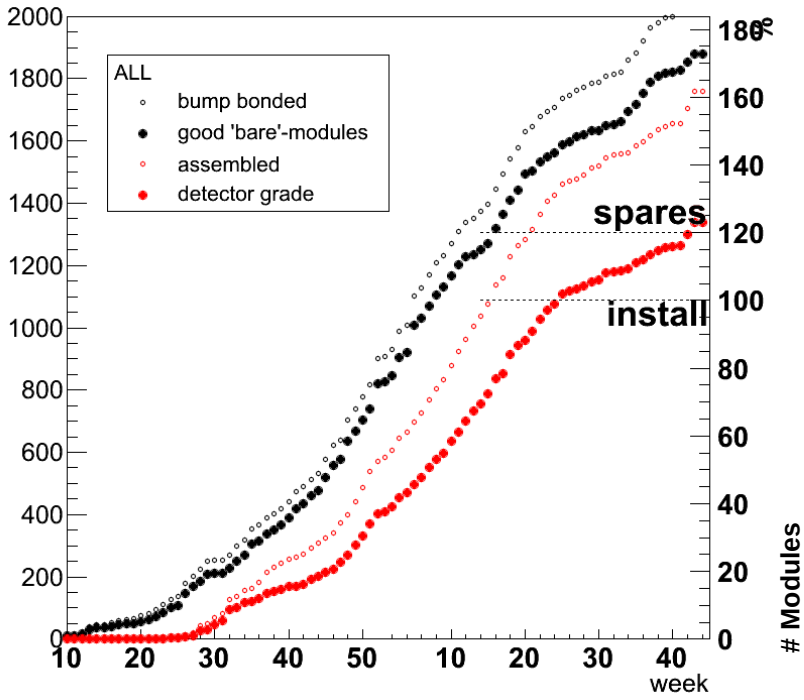
Calibration Fit

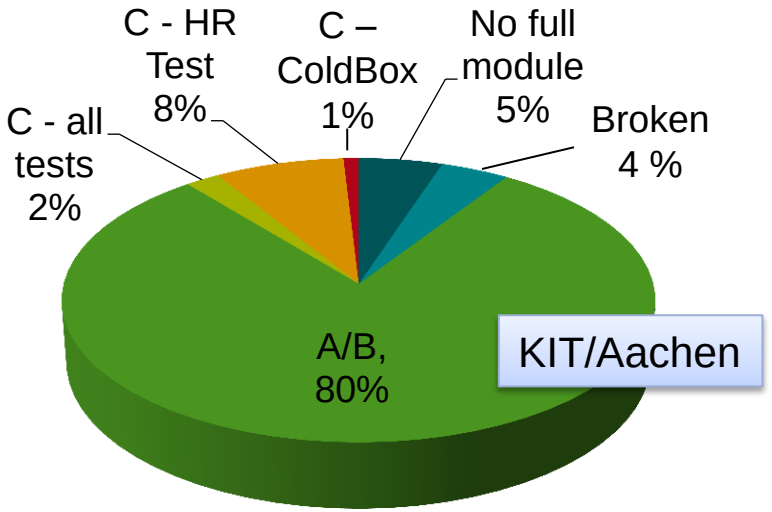


3.6 eV per electron in Si

Results from Production (BPIX)

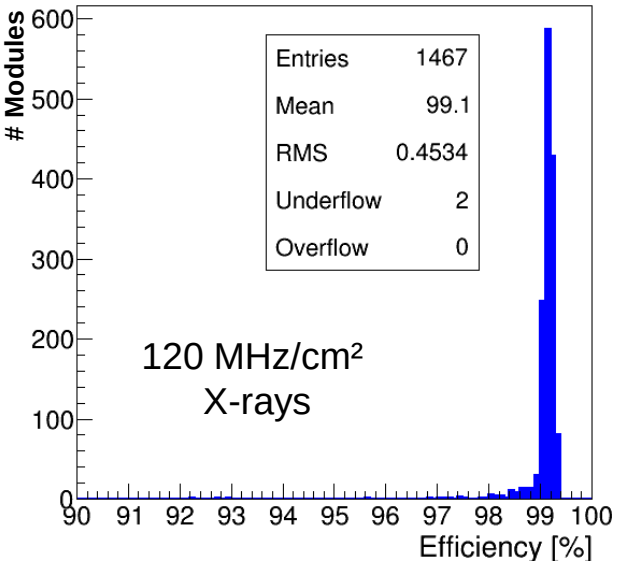
Production finished in Summer 2016:



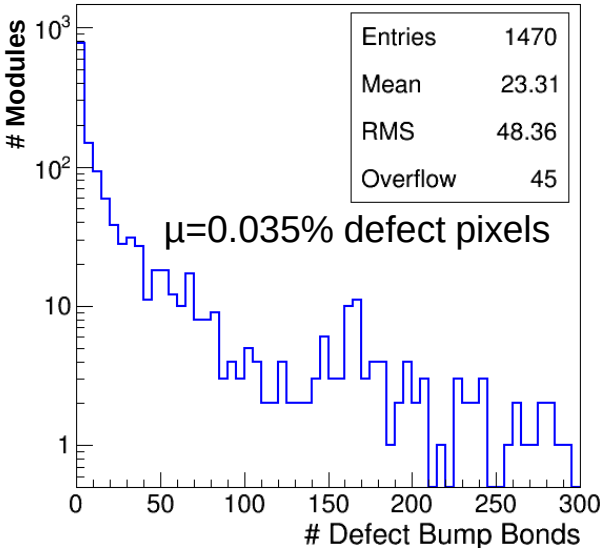


- Slow ramp up due to distributed production scheme
- ≈ 2 years of production

Efficiency (BPIX L2-L4)



Defect Bump Bonds (BPIX L2-L4)



System Tests

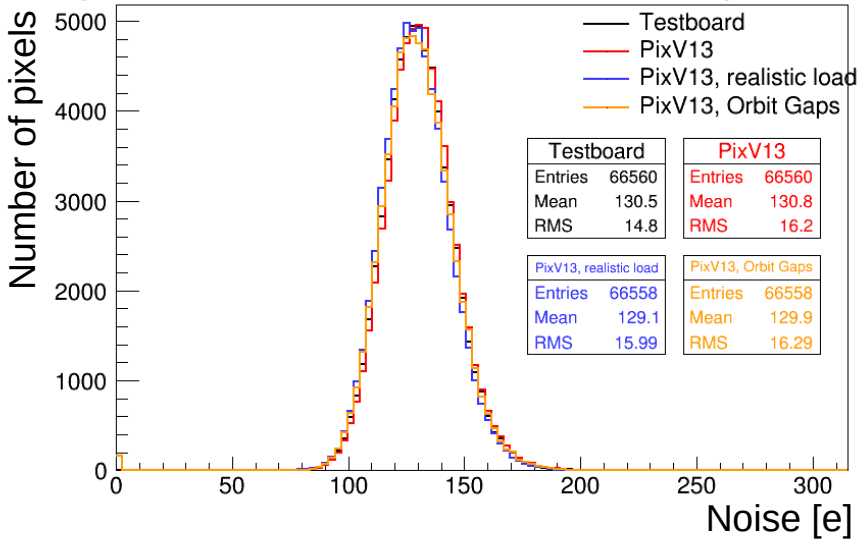
Various **test stands** to test the **full chain** with final DAQ

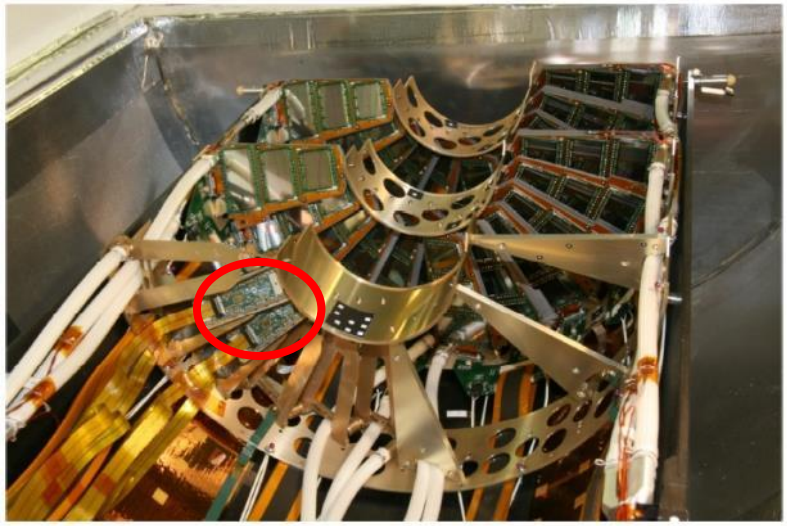
- Test the power system, cooling and readout in practice
- Software and Firmware development for the final detector

Pilot System:

- 8 prototype modules installed in old detector
- Taking data in 2015 and 2016
- Operation under **realistic conditions**

Comparison of conventional and DC-DC powering:

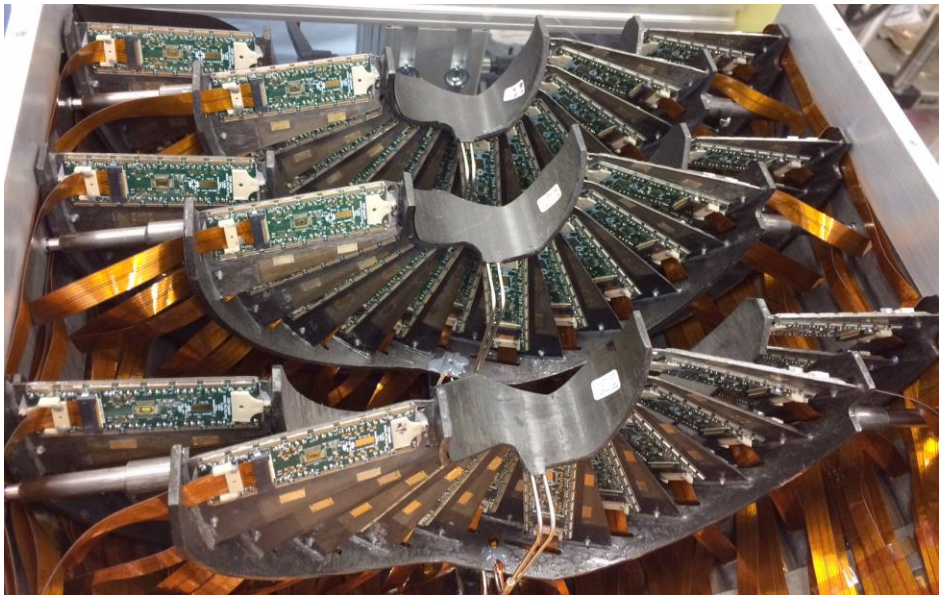


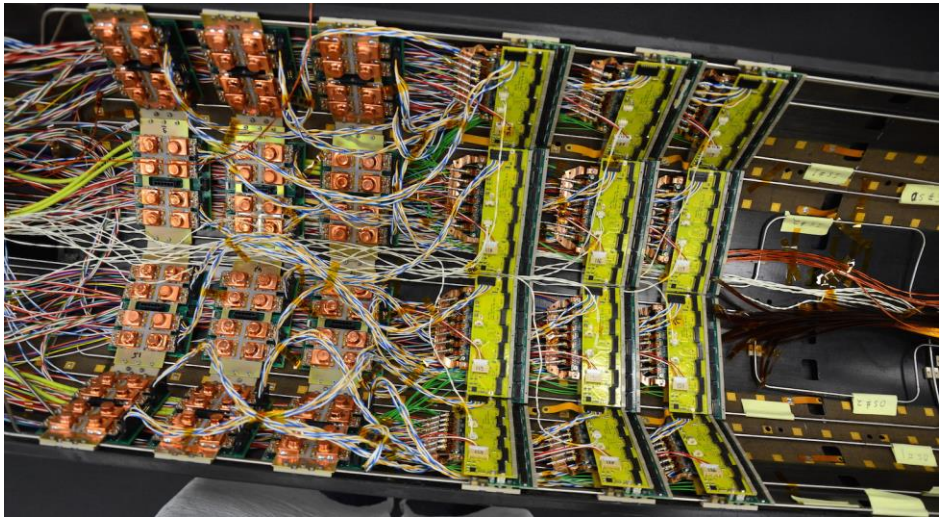


µTCA-based DAQ

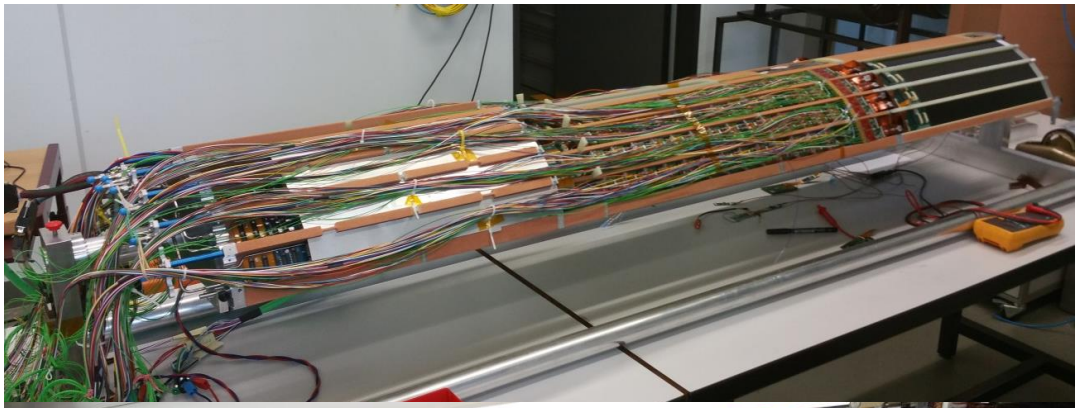
Detector Assembly and Integration

FPIX:



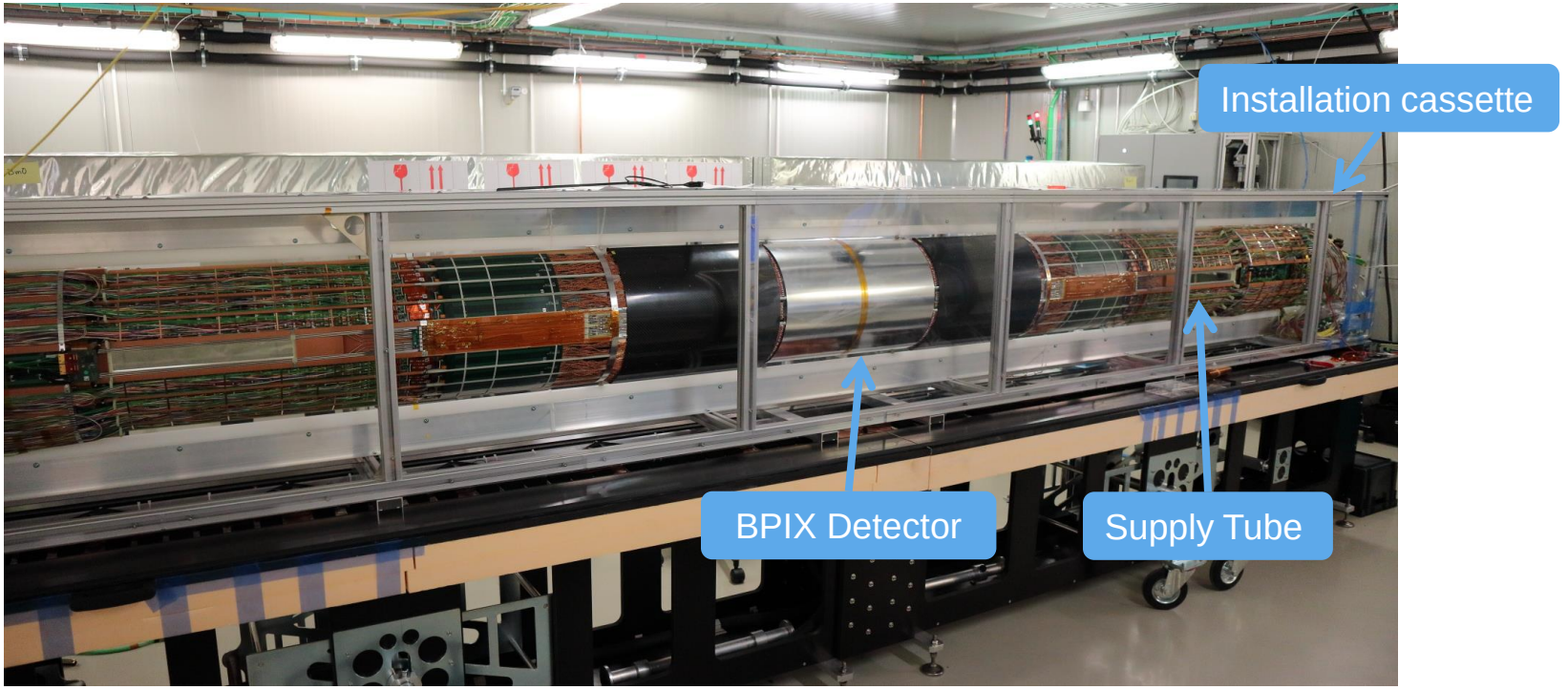


BPIX:



Final Tests

- Assembly and test at the integration centers (USA, Switzerland)
- Detector transported to CERN for **final checkout**:
  - Detector is run cold
  - BPIX: Quick test:
    - Module programmability
    - Noise measurement (Scurves)
    - Low voltage currents
  - FPIX: Full calibration sequence



Summary

New pixel detector to be installed in CMS in extended technical stop 2016/2017

- Additional layer in the barrel and endcaps will almost double the number of channels
- Still reduced material budget due to lightweight structure and evaporative CO_2 cooling
- New readout chips with higher rate capability developed

→ Upgrade detector will maintain high quality physics data taking

- Distributed production of all parts has finished
- Detector is fully integrated
- Final checkout is ongoing at CERN
- Installation at the end of February & beginning of March