Front-End Electronics development status for TPC detector of MPD/NICA project

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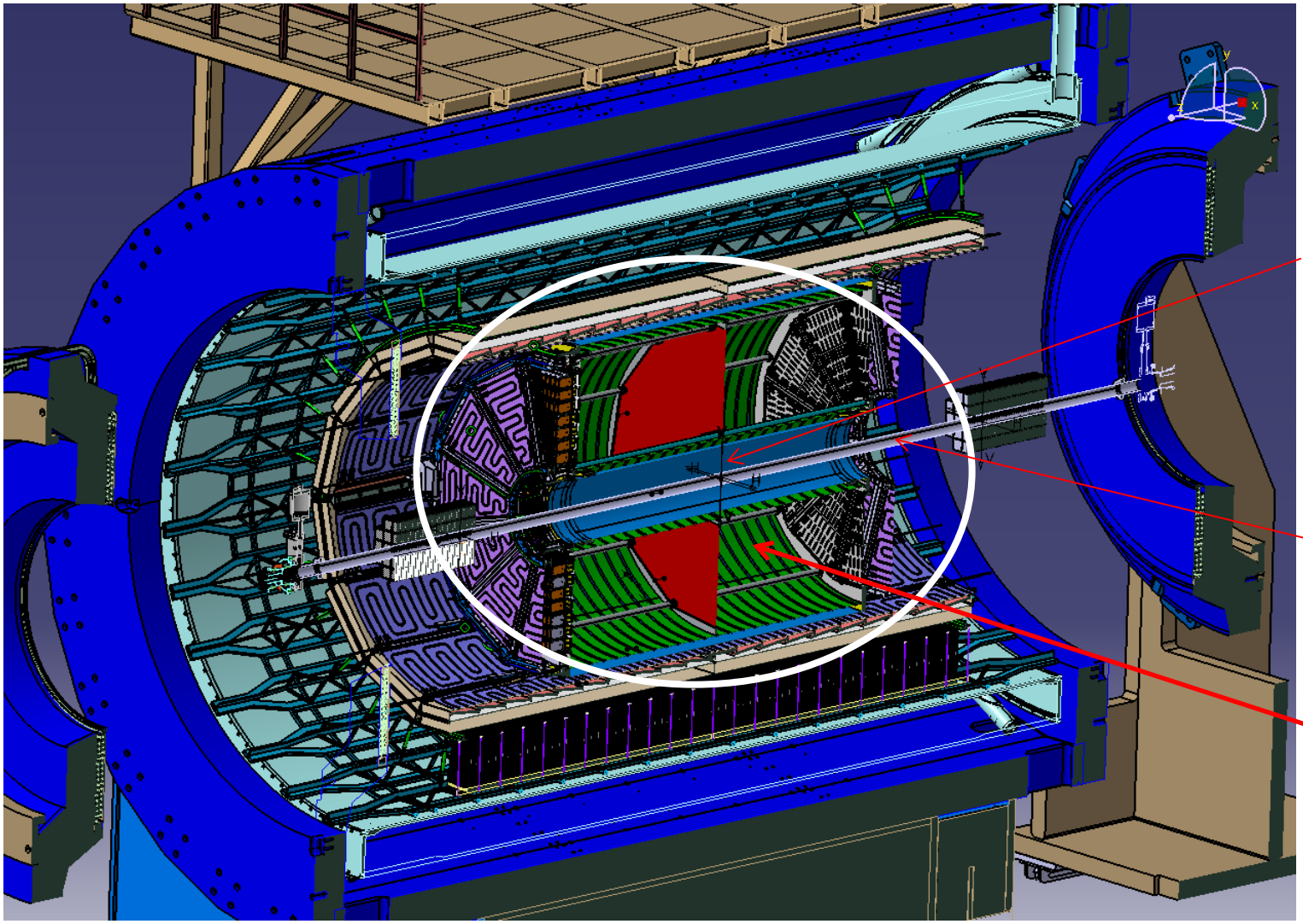
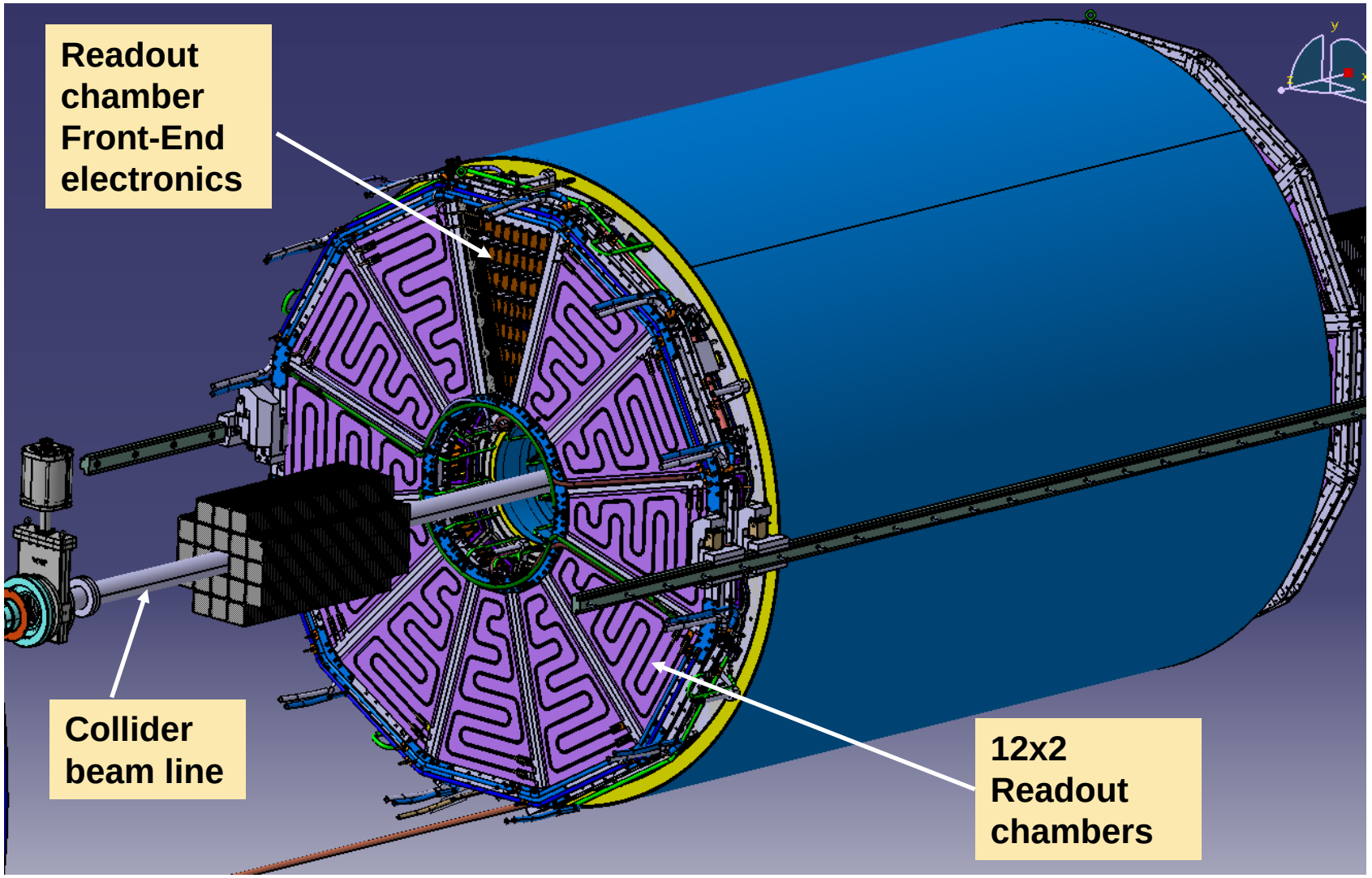
Outline

- TPC/MPD design overview and general characteristics
- Working parameters of the TPC Front-End Electronics (FEE)
- Readout Control Unit (RCU)
- Front-End Card (FEC)
- Testing of FEE
- Future improvements (possible design version)
- Conclusions

General view of the MultiPurpose Detector (MPD) of NICA project



TPC design overview



Main parameters of the TPC

Length of the TPC	340 cm
Outer radius of cylinder	140 cm
Inner radius of cylinder	27 cm
Length of the drift volume	170cm (of each half)
Magnetic field strength	0.5 Tesla
Drift gas	90% Ar+10% CH_4
Temperature stability	0.5°C
Gas amplification factor	~ 10^4
Number of readout chambers	24 (12 per end plate)
Pad size	5x12mm^2 and 5x18mm^2
Pad raw numbers	53
Number of pads	95 232
Maximal trigger rate	~7 kHz (at luminosity up to 10^{27} cm^{-2} s^{-1} for Au^{79+} ions over the energy range $4 < \sqrt{S_{NN}} < 11$ GeV)
dE/dx	better than 8%
Δp/p	~ 3% in $0.1 < p_t < 1$ GeV/c

FEE design goals and concept

- The goal of the design is to satisfy NICA project requirements: trigger rate 7 kHz at luminosity up to 10^{27} cm^{-2} s^{-1} for Au^{79+} ions over the energy range $4 < \sqrt{S_{NN}} < 11$ GeV with expected mean multiplicity ~300 tracks.
- Widely usage of modern technologies such as fast serial lines, optical interfaces, ASICs and FPGAs allow us achieve the goal.
- Our design concept correspond to a upgrade trends for modern data readout systems.

Working FEE parameters

The large data volume which produced by TPC determines severe requirements to the readout system.

- ✓ *Total number of ADC channels - 95 232*
- ✓ *Mean data stream from whole TPC – 10 Gbyte/s*
- ✓ *Power consumption not more then 100 mW/ch*

- Based on ASIC and FPGA
- Fast optical transfer interface to DAQ/MPD

FEE options

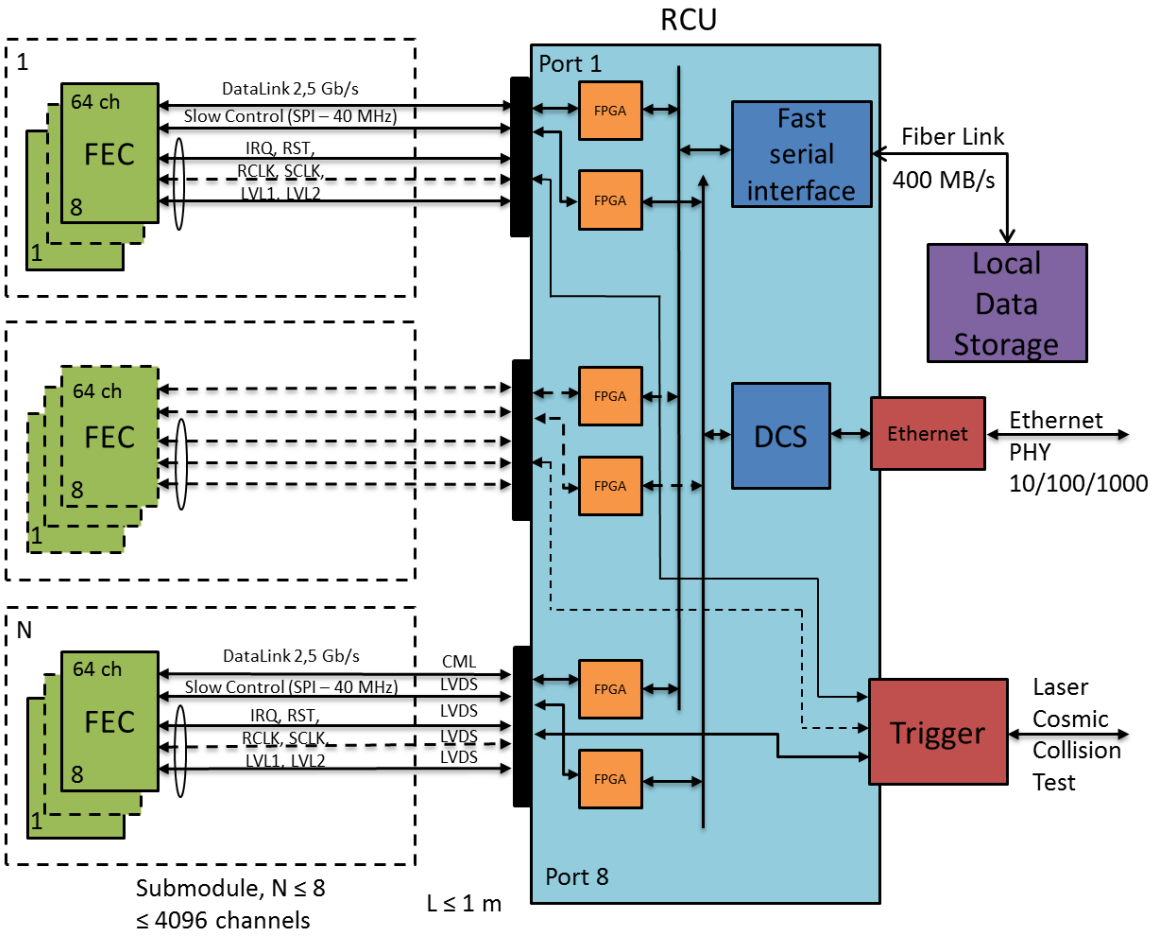
At this point we are seeing two options for FEE ASICs:

- *ALTRO[1] + PASA[2] based electronics*
- *SAMPA[3,4] based electronics*

- ALTRO + PASA base design was completed
- SAMPA design is under considering

[1] ALICE TPC Readout Chip. User Manual. CERN, June 2002, Draft 0.2. ALTRO chip web page, http://ep-ed-alice-tpc.web.cern.ch/ep-ed-alice-tpc.
[2] ALICE TPC Electronics. Charge Sensitive Shaping Amplifier (PASA). Technical Specifications, CERN, 2003.

FEE block diagram for one readout chamber



Total number of ch.- 95 232

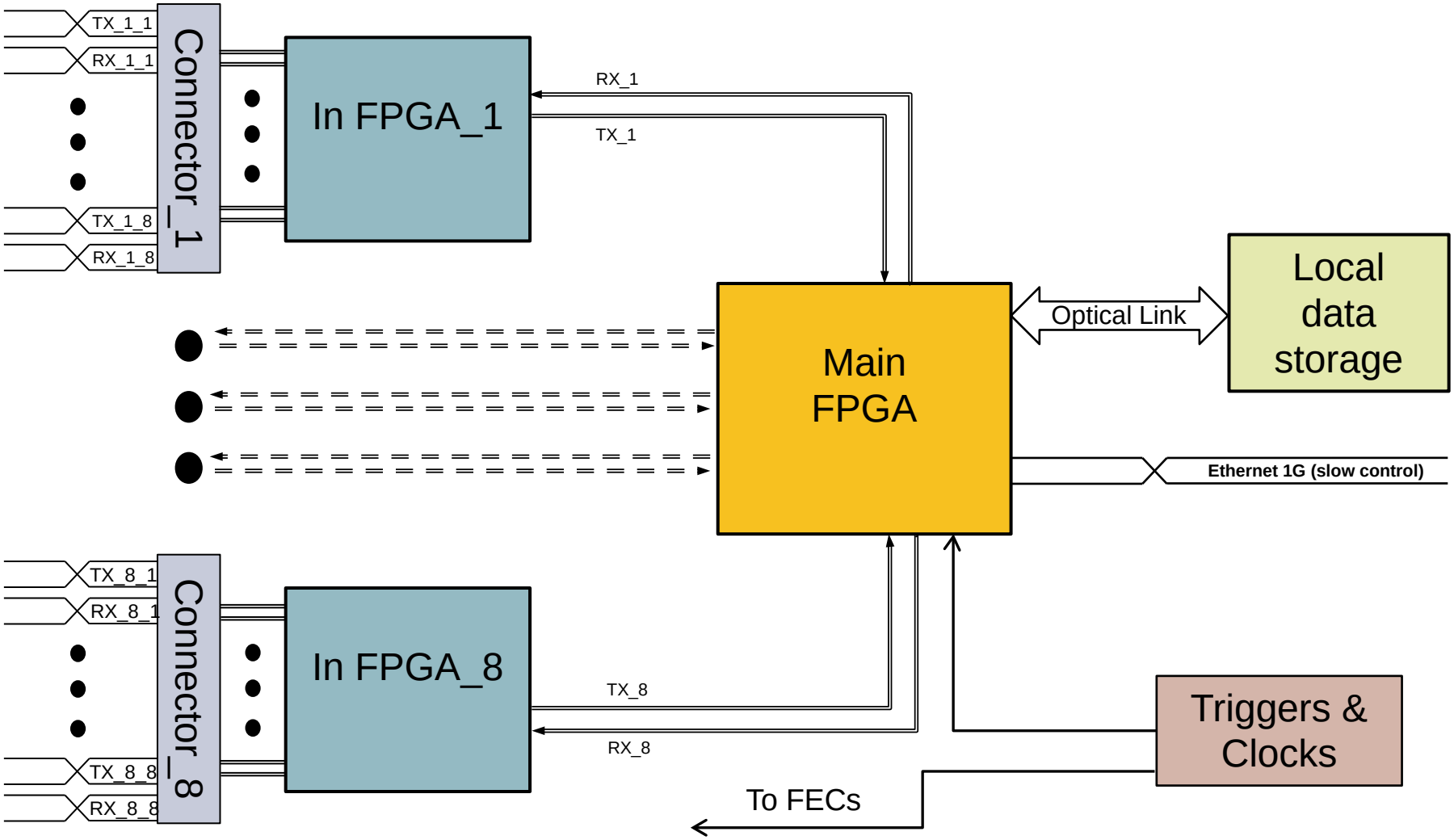
Total number of FECs - 1488

Total number of RCU - 24

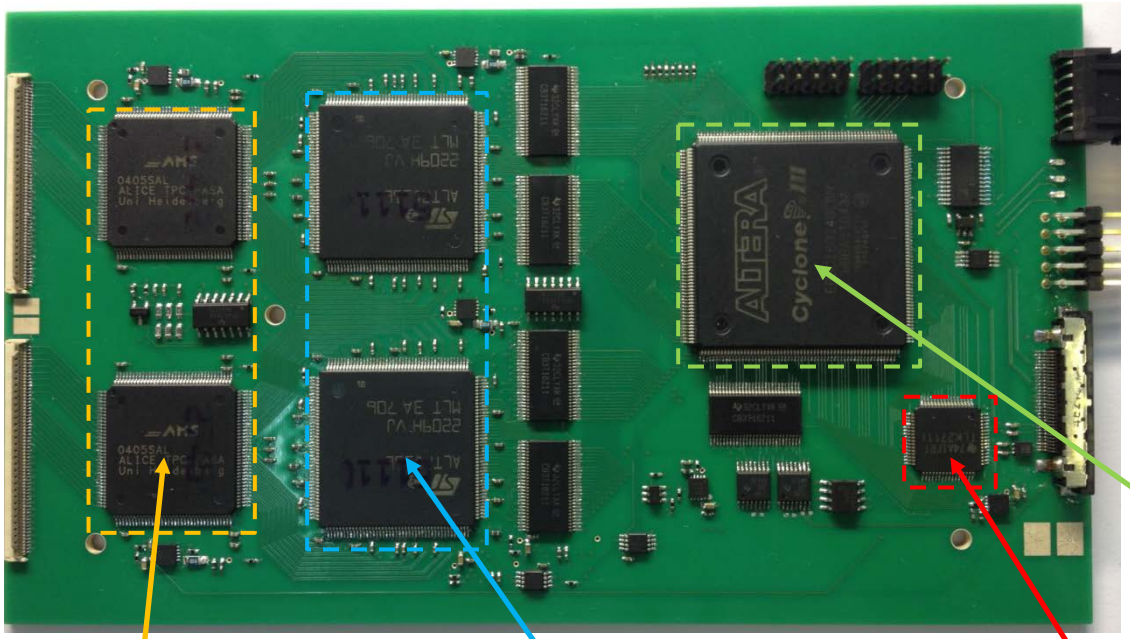
Readout Control Unit (RCU)

- The RCU design with base functionality including FECs initialization and data acquisition is performed.
- FPGAs firmware is designed and simulated.
- The part of FPGA firmware tested with Altera development board as RCU emulator.
- RCU full schematic is completed.
- PCB layout will started soon.

RCU structure (main functionality)



64-ch. Front-End Card (top side)



- Signal to noise ratio, S/N - 30
- $\sigma_{NOISE} < 1000e^-$ (C=10-20 pF)
- Dynamic Range – 1000
- Zero suppression
- Buffer (4 / 8 events)

ALTERA FPGA - board control

PASA chip
16 channels ASIC (low noise amplification of the signal)

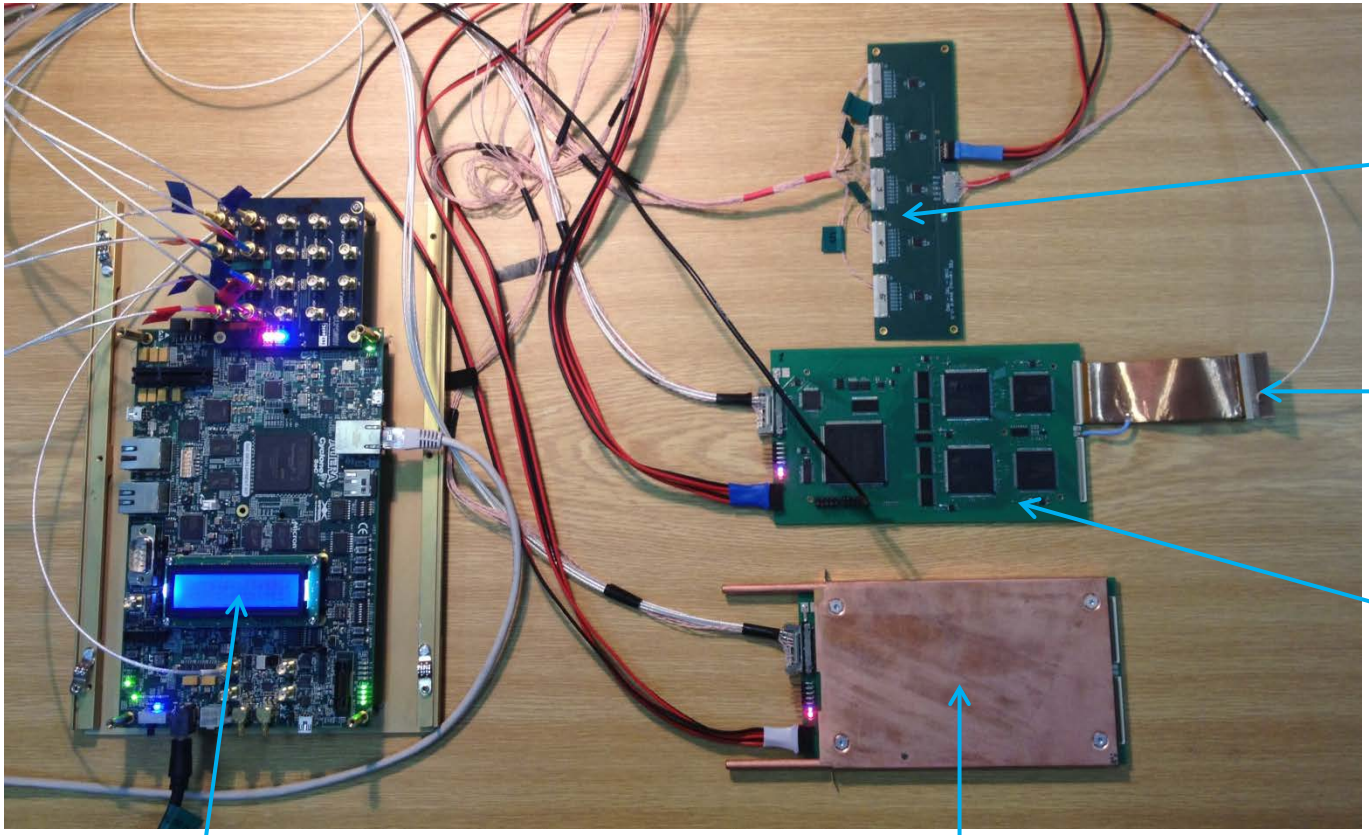
ALTRO chip
16 channels ASIC (digitization and signal processing)

TLK2711
Serial interface
Data throughput up to 2.5 Gb/s

FEC FPGA firmware

- Multiplexing of 64 ADC ch. parallel words ALTRO data packet to serial data stream.
- Providing initialization and data acquisition modes.
- Providing triggering and synchronization ALTRO processing.
- Monitoring of the temperature and 15 values of voltages and currents on board.
- CRC self checking of the FPGA firmware.
- Slow control interface (SPI 40 MHz).

Full-function FEE system testing



Clocks, triggers and reset fan-out board

Signal injecting chain

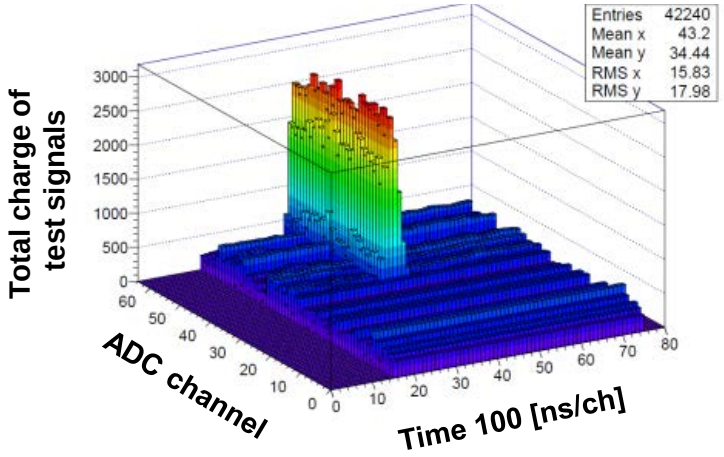
FEC

Altera kit
(RCU emulator)

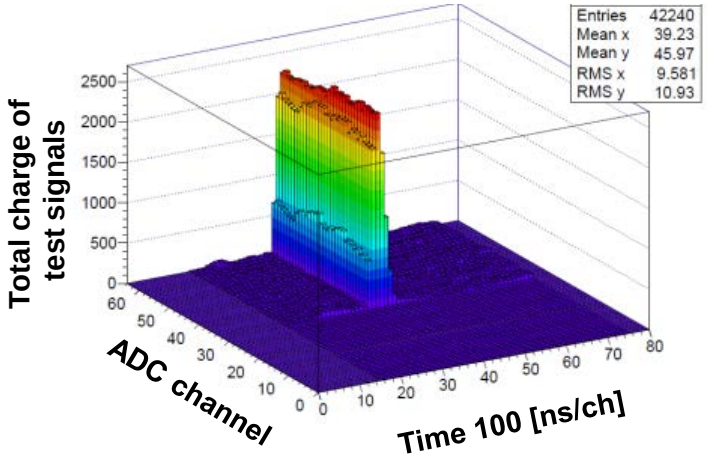
FEC with cooling box

ALTRO signal processing

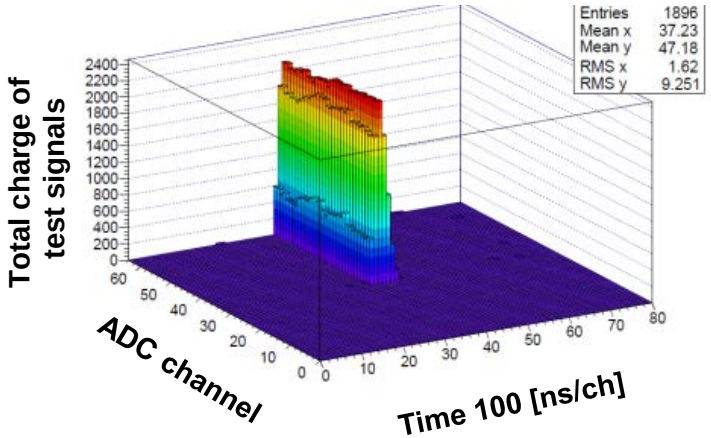
Test signal without processing



ADC self calibration mode



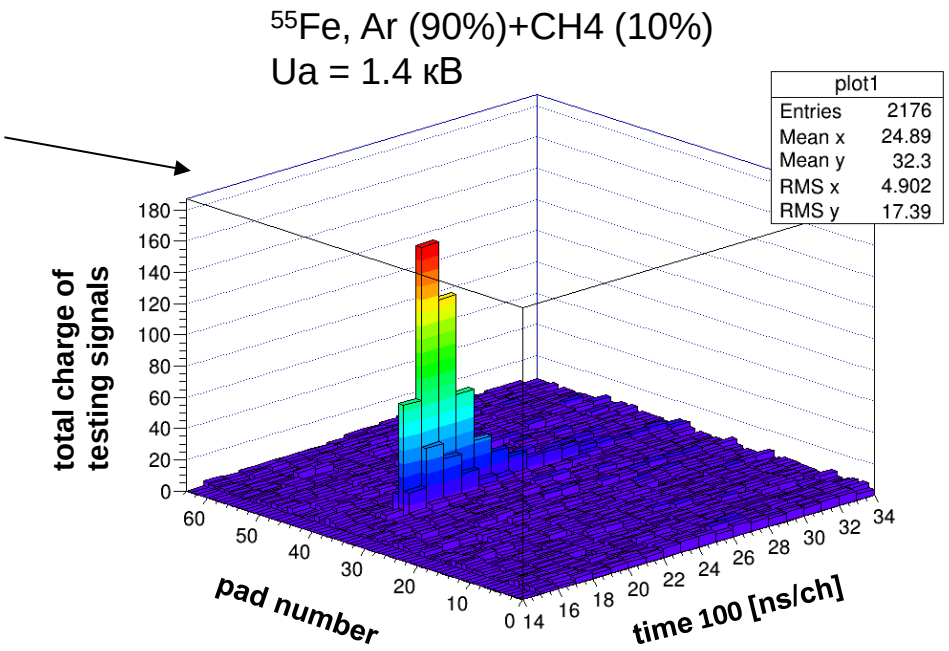
ADC self calibration mode + zero filtration



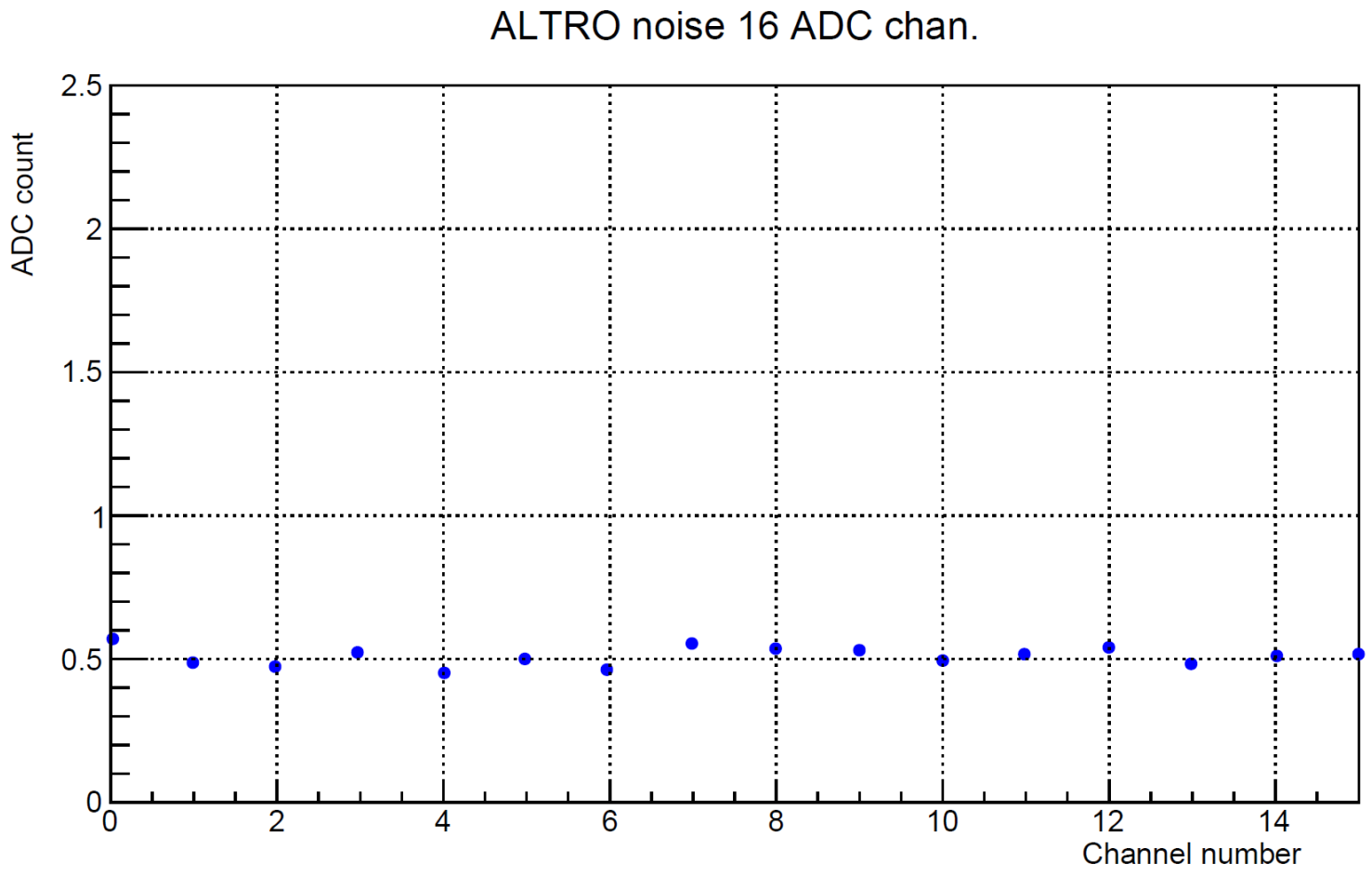
FEC testing on the readout chamber with ^{55}Fe

- Trigger from anode wires
- γ quantum ~ 400 Hz
- Total number of channels 64x3
- Event collection with different collimators

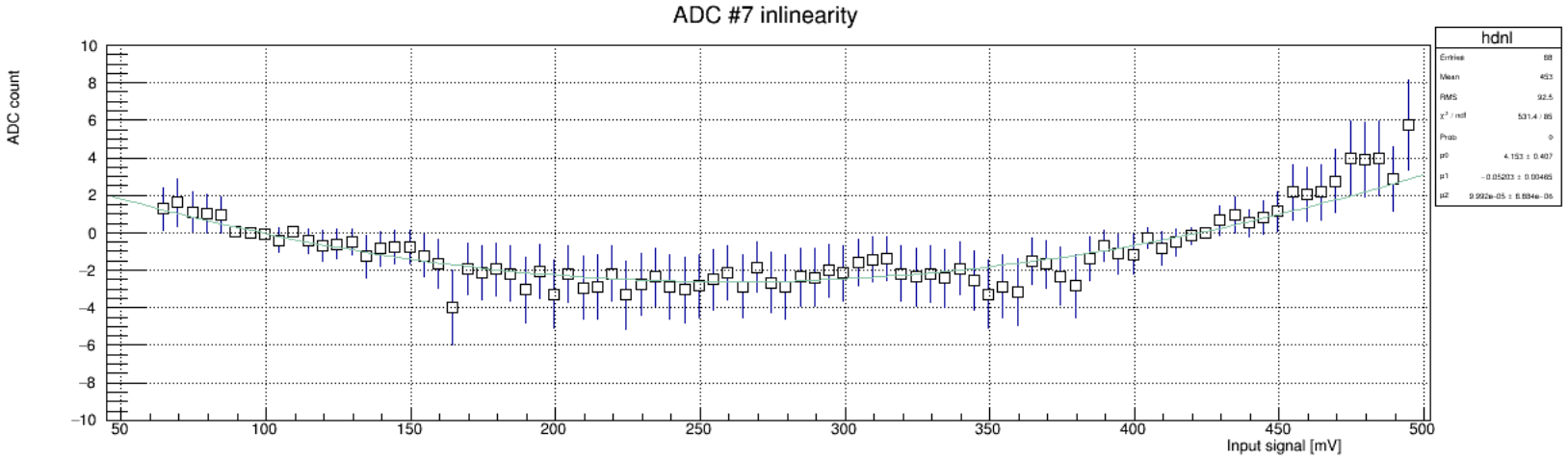
γ quantum value with energy E= 6 kEv which fell on the middle of pad 36

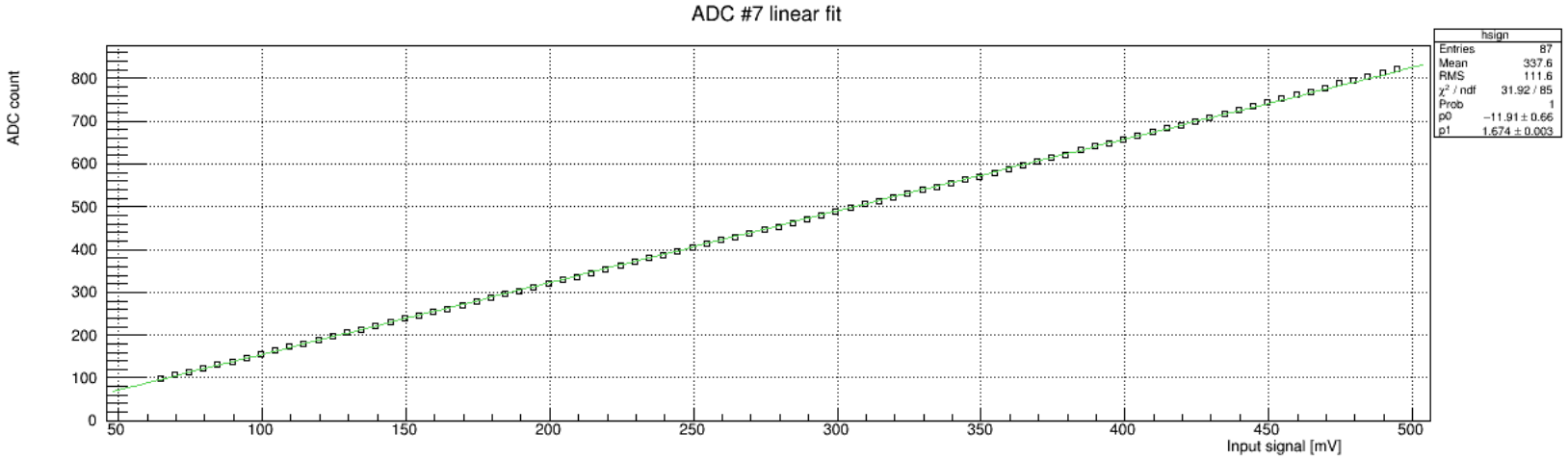


FEC noise measurement



FEC linearity





New ASIC for TPC electronics (SAMPA)

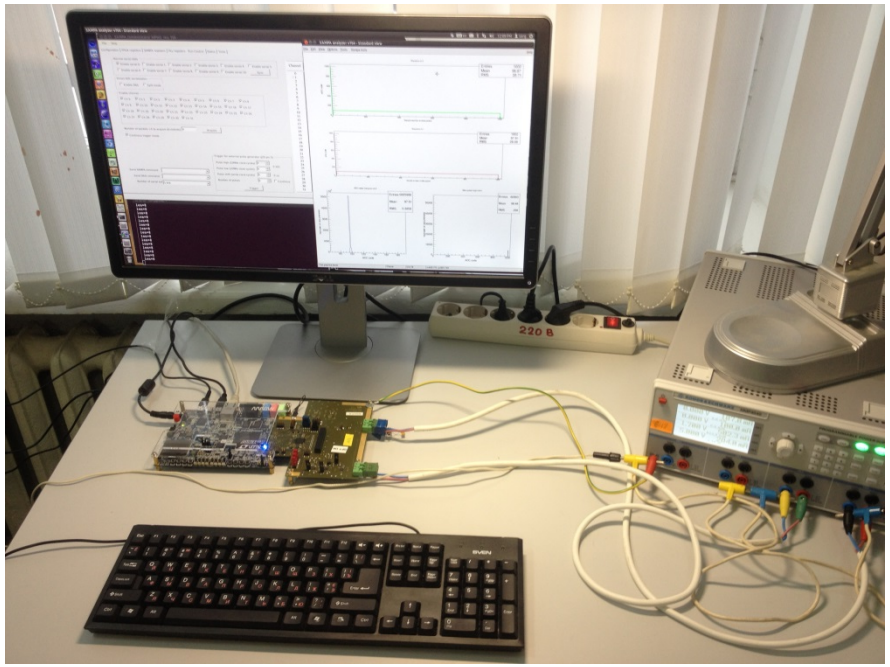
- New ASIC SAMPA [3,4] is under development.
- Few amount of pilot chips version was tested and measurement results show us feasibility of design SAMPA-based FEC for the TPC MPD/NICA.
- Concept of usage SAMPA chip in FECs was defined.

[3] S.H.I. Barboza et all. SAMPA Chip: a New ASIC for the ALICE TPC and MCH Upgrades. // J. Instrum. 2016. V. 11. C02088.

[4] Topical workshop on electronics for particle physics TWEPP2016, http://indico.cern.ch/event/489996/book-of-abstracts.pdf, p. 55.

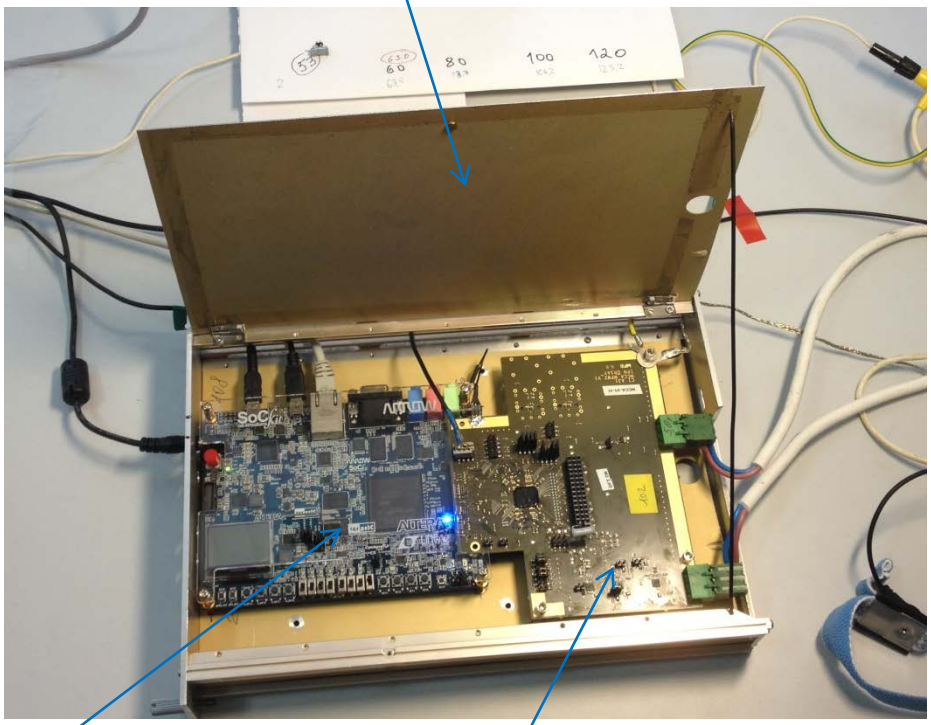
SAMPA testing in Dubna

https://indico.cern.ch/event/593915/contributions/2407472/attachments/1389543/2116166/Noise-NCCA-vs-Cap-15dec_.pdf



General view of test bench

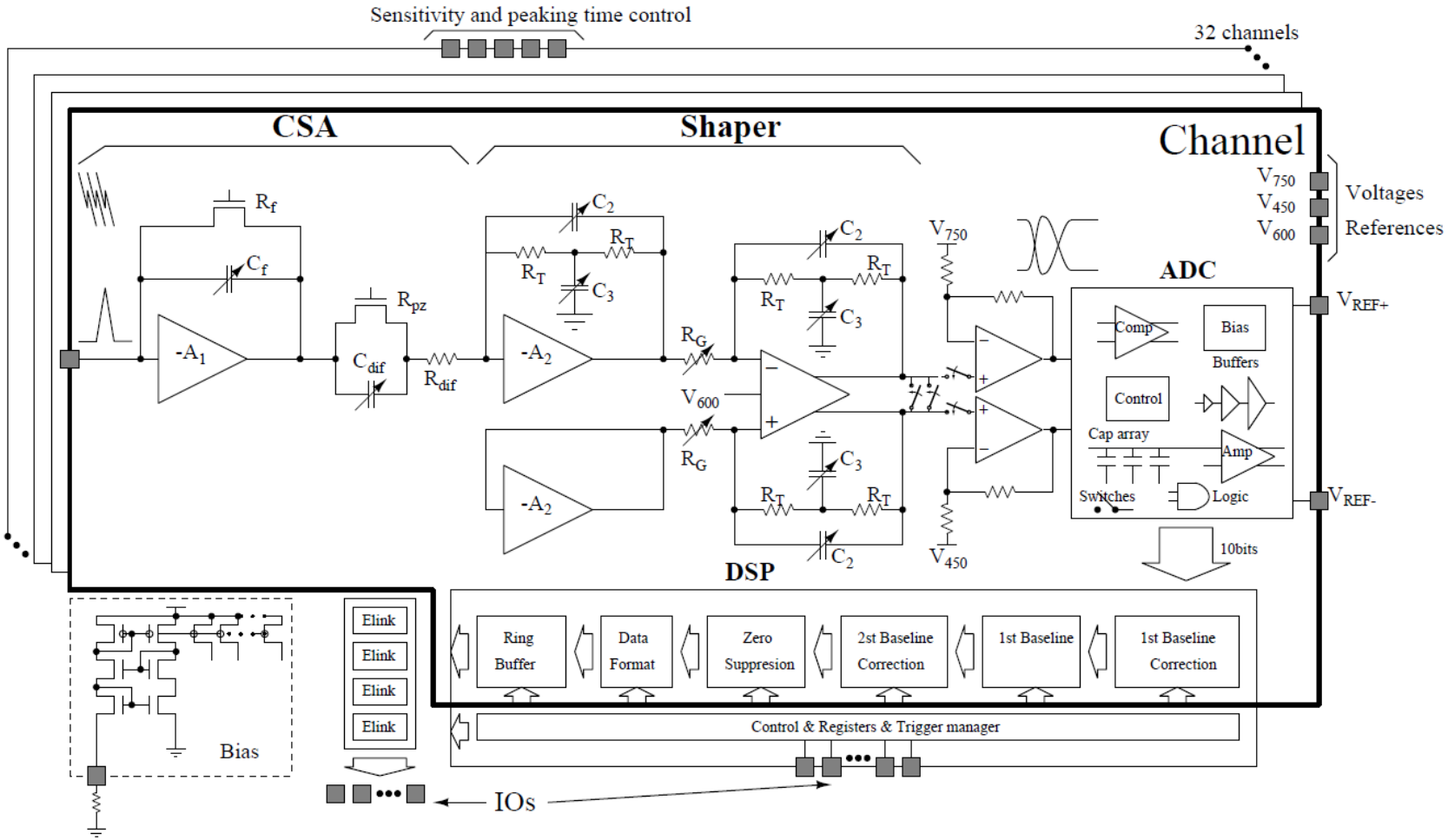
Shielding box



Altera Cyclone V
SOC Kit

SAMPA test board

SAMPA block diagram



Main advantages of SAMPA

- SAMPA is more integrated then PASA + ALTRO.
  - Contain analog and digital parts in one package.
  - Consist of 32 channels.
- Operate as with positive as with negative polarity i.e. compatible as with MWPC as with GEM detectors.
- Provided opportunity of self-triggered mode.
- Contains serial data outputs.
- Consume low power.

Conclusion

- FEE TPC for MPD/NICA project was designed.
- FEC testing including analog and digital parts was performed. RCU firmware was developed and verified.
- ALTRO-based FEC design is complete and trial lot of FECs was fabricated.
- RCU prototype is under verification.
- FEC concept based on SAMPA chip is defined.

On behalf TPC/MPD electronics group
allow me to express gratitude for the help to:

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Alex Kluge (CERN)
Marco Bregant (USP, Brazil)

Thank you for your attention!