Development of high resolution GEM-based detector for the extracted electron beam facility at the VEPP-4M collider.

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Abstract: *The Facility of the extracted beams of electrons and gammas is based at the e^+e^- VEPP-4M collider. This installation is designed to test prototypes of detectors for HEP projects. Measurements taken at this installation require high resolution low-mass tracking detectors to precisely determine particle trajectories.*

The extracted beam facility experiment

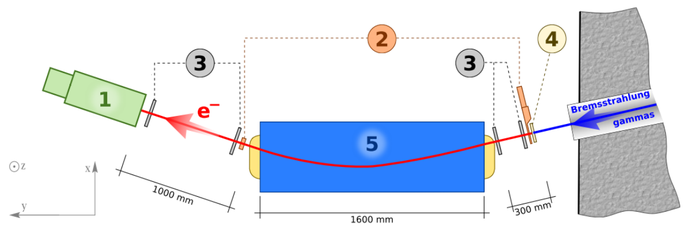

Figure. 1: *The extracted beam facility schematic view. Experimental setup: 1 – BGO calorimeter, 2 – trigger scintillation counters, 3 – GEM detectors, 4 – lead target, 5 – bending magnet.*

Budker Institute of Nuclear Physics has a special installation for generation of extracted beams of electrons and photons in a wide range of energies at the VEPP-4M collider.

This installation is designed to test prototype of detectors for HEP projects. Design parameters of the extracted electron beam are the following: intensity is not less than 50 Hz, energy range is from 0.1 GeV to 3.0 GeV and energy resolution is about 2–3%. The gamma energy range is from 0.05 GeV to 4.0 GeV with an accuracy of 0.5% of energy [4]. The designed intensity of the gamma beam is about 1000 Hz.

Since 2011 the extracted electron beam is used for tests and measurements for various detector prototypes. For the purposes of this experiment four triple-GEM detectors are planned to be installed (fig. 1).

The GEM Detector

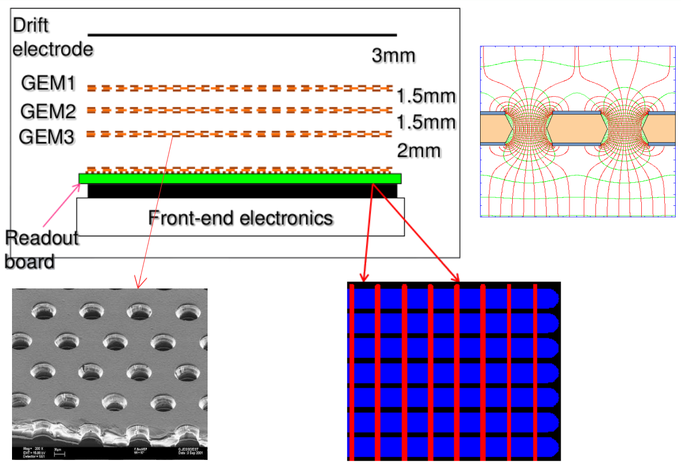

Figure 2: *Schematic view of the detector's cross-section*

The prototype detector design with high spatial resolution and low material content was developed and during 2016 the first detector was manufactured (GEMs, flexible readout structures and electronics PCBs made at CERN Workshop, assembly finalized at the BINP).

In general the detector design is very similar to that of the detectors for the DEUTERON experiment [3]. The detector consists of three cascades of gaseous electron multiplier (GEM), the X-Y readout structure and detector electronics. Electronics is based on the APC128 ASIC (analog pipeline chip, 128 channels), six of these chips are used covering 768 channels in total. These channels are connected to the readout structure (fig. 2), which has two layers: 512 vertical strips and 256 horizontal strips, both directions have 0.25 mm pitch of the readout strips. The detector sensitive area is 128x64 mm^2.

In order to minimize multiple scattering the detector elements will have a reduced thickness of copper down to 1-2 μm at each GEM side. Such an approach was investigated and it was found that the thinning of copper layers does not affect the detector performance.

Triple-GEM detector with thinner copper layers will have a total amount of material seen by particles of ~0.15% of radiation length. With such amount of material the contribution of multiple scattering to the spatial resolution of the detectors in the experiment will fall below 100μm, the exact value is a subject of future study.

Detector electronics

In figure 3 the photograph of a new detector is shown. The new custom made detector electronics is based on the APC128 front-end chip [2], which will be described in the next section.

The detector electronics is divided into motheboard PCB and two DAQ boards. Each DAQ board consists of 4 blocks of APC128 ASIC and a dedicated 14-bit ADC covering 512 channels in total. Input channels of the DAQ board are wired through the special protection circuits against high voltage discharges (see Fig. 4). Both DAQ boards are connected to the motherboard through flat ribbon cables, and custom power cables.

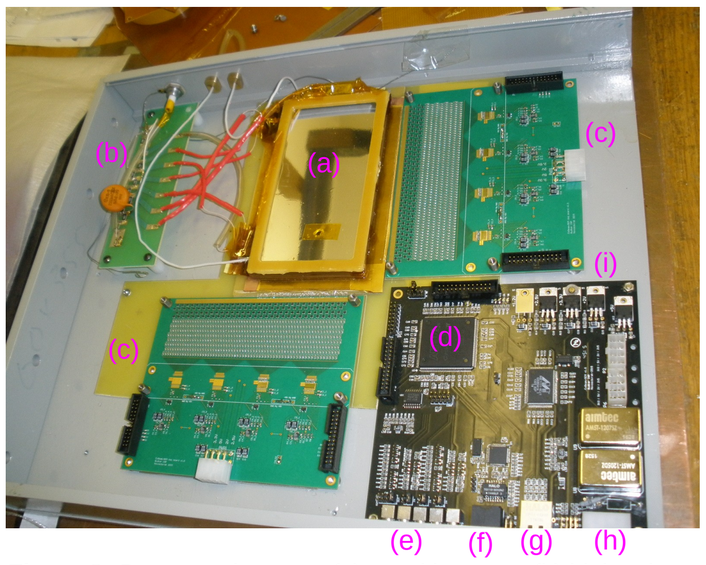

Figure 3: *Detector elements: (a) sensitive area, (b) high voltage, (c) DAQ boards, (d) FPGA, (e) trigger inputs, (f) 100MBit ethernet, (g) 1GBit ethernet, (h) power +12V, (I) analog power for DAQ boards.*

The readout of all ADCs is performed in parallel and synchronously with the front-end chips readout sequence. The Altera Cyclone III FPGA controls the data-taking process and is connected to the PC by the 100MBit ethernet interface. The interaction between electronics and PC is performed over UDP datagrams with commands and digitized data. The electronics also features additional 1GBit ethernet interface for the faster data transfer.

In the prototype detector the high voltage is fed from the outside HV source, but detector has a special mount point for installation of HV board which was developed but is still in the process of manufacturing.

Due to limited amount of APC128 chips and expecting better parameters from alternatives, future designs will be based on DMXG64 ASIC which was developed at the BINP.

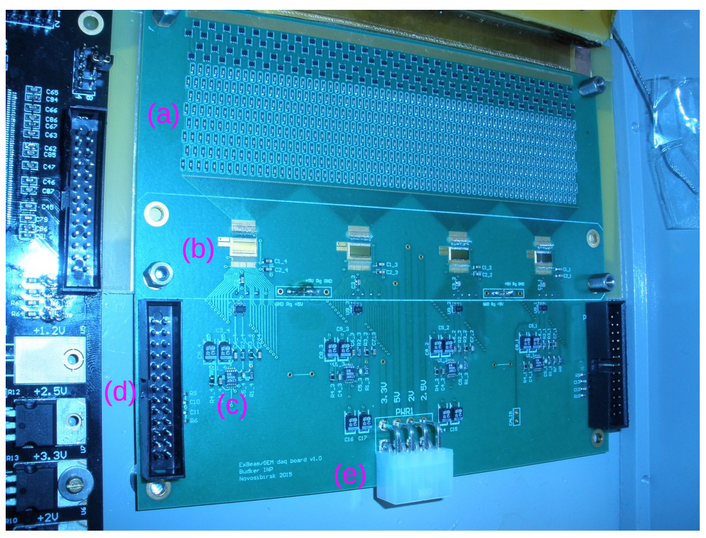

Figure 4: *DAQ board elements: (a) ESD protection circuits, (b) APC128 ASICs, (c) 14bit ADC, (d) motherboard interface connector, (e) power connector (+3.3/+5.0/+2.0/+2.5V/GND)*

APC128 front-end chip

Figure 5 shows schematically one of 128 channels of the Analog Pipeline Chip. Each channel has a charge sensitive, low noise, low power preamplifier followed by a 32-cell storage pipeline. The storage pipeline consists of switched capacitors. When disconnecting the capacitors they store a charge proportional to the output voltage of the preamplifier. The storage capacitors of the pipeline are controlled by the pipeline shift register. This pipeline shift register can be operated with a frequency of 10.4 MHz.

To read out the pipeline the sampling is stopped and the input of the charge sensitive preamplifier is disconnected from the sensor by the IS signal (see Fig. 5). By means of the SR signal the pipeline is connected to the input of the preamplifier. The bit in the pipeline shift register determines now, which storage cell is re-read by the amplifier. This so called re-read architecture, a peculiarity of the APC chip, offers various advantages: As the preamplifier re-reads its own signal a perfect matching of the operating point is automatically given. The ratio between the pipeline capacitor C_p and the feedback capacitor C_1 or C_1+C_2 allows to define a signal gain while re-reading.

The serial readout of the 128 latch-capacitors of the chip is controlled via the readout shift register that connects one channel at a time to a common two stage readout amplifier. Both the re-reading architecture and the serial readout are area-efficient concepts implicating that most of the area on the APC chip is occupied by the bond pads and the pipeline capacitors. This leads to a total chip size of 6.3mm by 3.5mm.

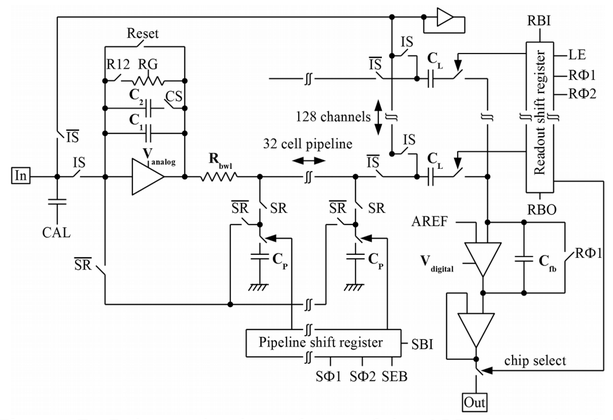

Figure 5: *Schematic view of one of the 128 channels of APC128*

Electronics calibration

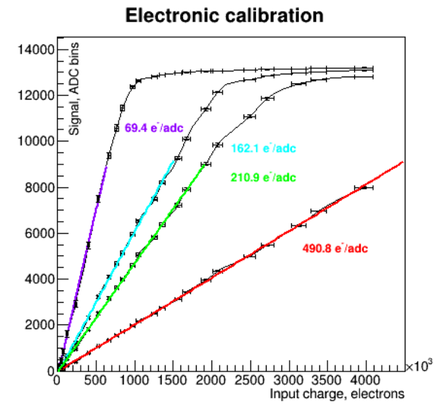

Figure 6: *Electronic calibration results with different internal attenuation: magenta – 0db, blue – 9db, green – 13db, red – 22db.*

The electronic calibration is made by injecting known charge into an input channel of electronics. From the generator signal was fed through the 2pF capacitor into a single channel of APC128. The same signal was used as a trigger for DAQ, thus all the channels including affected one were digitized.

The main purposes were to measure conversion factor from ADC values to the charge in electrons (see Fig. 6) as well as channel noise. Another reason of this procedure is to check if possible crosstalk problem is present.

This process was done for all modes of internal attenuation in order to select the one most suitable for operation in the final conditions at the beam.

Recent results

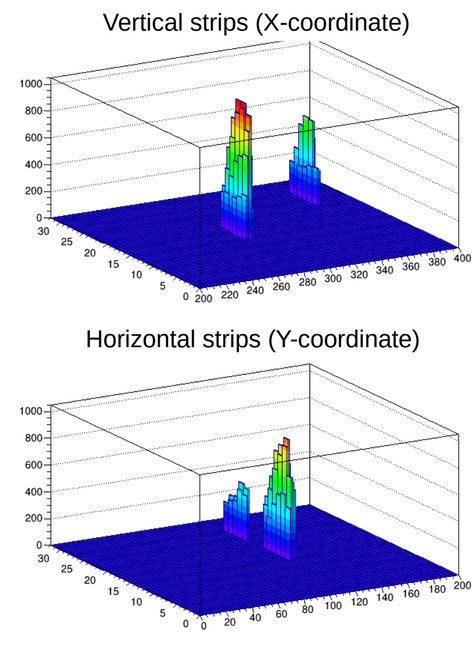

Figure 7: *Sample event acquired in the laboratory with the radioactive isotope.*

The prototype detector was manufactured and proved to be operational. As of now the process of collecting and processing the data at the extracted beam facility and in the laboratory with radioactive source is going on.

In figure 7 the sample event is shown, there top plot shows channels from vertical strips and bottom plot shows channels from horizontal strips. Two tracks were registered and can be separated due to different timing and channels value.

References

[1] Shekhtman L.I. et al. / **High resolution tracking detectors with cascaded Gaseous Electron Multipliers.** // JINST, 2013, 8_C12035
[2] R. Horisberger and D. Pitzl. / **A novel readout chip for silicon strip detectors with analog pipeline and digitally controlled analog signal processing.** // Nucl. Instrum. Meth., A 326 (1993) 92.
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[4] Abramov G.N. et.al./ **Measurement of the energy of electrons extracted from the VEPP-4M accelerator.** // JINST, V.11, I.3, 2016, P03004.