Monitoring Single Event Upsets in SRAM-based FPGAs at the SuperKEKB Interaction Point

Raffaele Giordano[1,2], Vincenzo Izzo[2],Sabrina Perrella[1,2], Gennaro Tortone[1] and Alberto Aloisio[1,2]

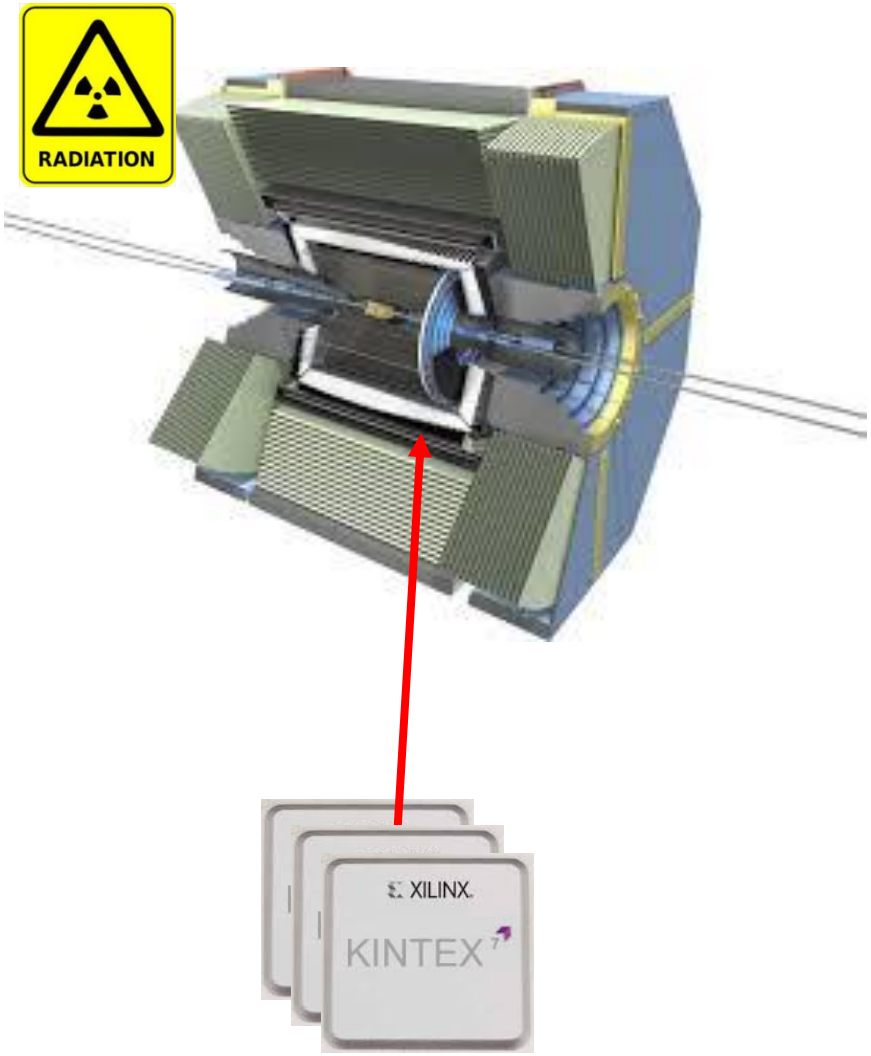
[1] Università degli Studi di Napoli "Federico II", I-80126, Italy
[2] INFN Sezione di Napoli, I-80126, Italy

Contact: rgiordano@na.infn.it

Overview

- Motivation
- The SuperKEKB collider
- FPGA setup at the IP
- Results
- Conclusions

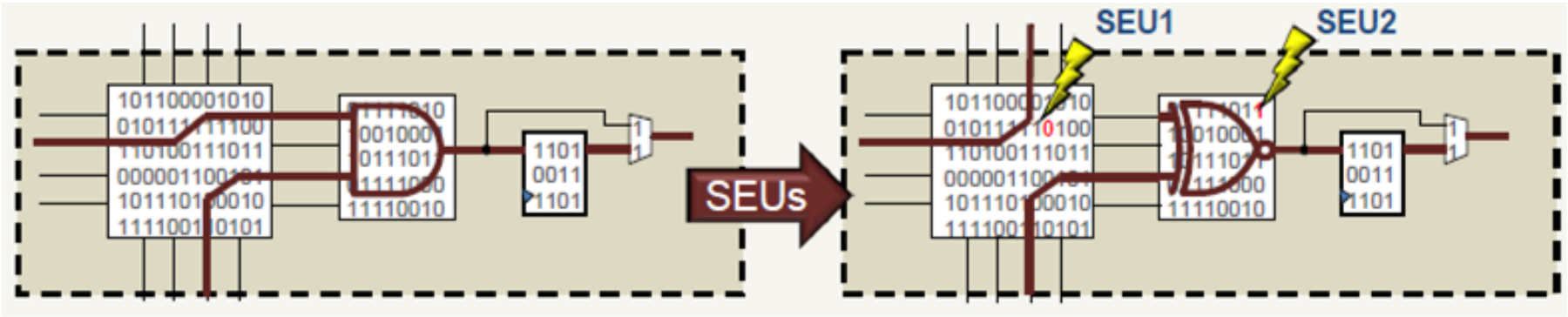
FPGAs in HEP Experiments



- SRAM-based FPGAs are high-speed programmable logic devices
- commercial grade FPGAs widely adopted in trigger and data acquisition systems for HEP
- sensitive to radiation
- soft errors in configuration memory may alter design functionality
- RadHard SRAM-based FPGAs exist but they are very expensive (~50k$ per unit), not sustainable for HEP (thousands of units needed per experiment)
- one possibility is to characterize commercial grade devices and find solutions for mitigating radiation effects

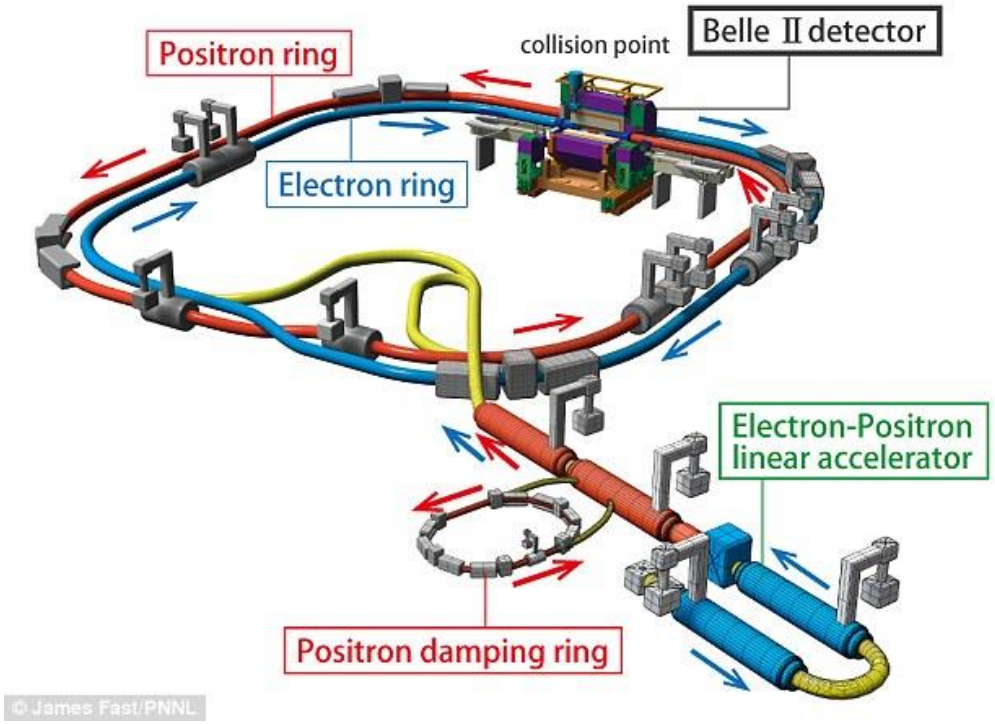
Soft Errors in SRAM-based FPGAs

- Usage of SRAM-based FPGAs is limited in radiation areas
  - Configuration (stored in static RAM) may be altered by radiation



- Radiation environment has to be known in order to have an estimated bit upset rate => design failure rate
- mitigation of radiation effects possible at different levels
  - Logical => Triple Modular Redundancy (lower the failure probability of each module, must be coupled to configuration scrubbing)
  - Layout => Placement and routing hardening (R. Giordano et al., IEEE Trans. On Nucl. Sci., Vol. 62, no. 6, Dec. 2015, pp. 3177-3185, Open Access http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7348785)

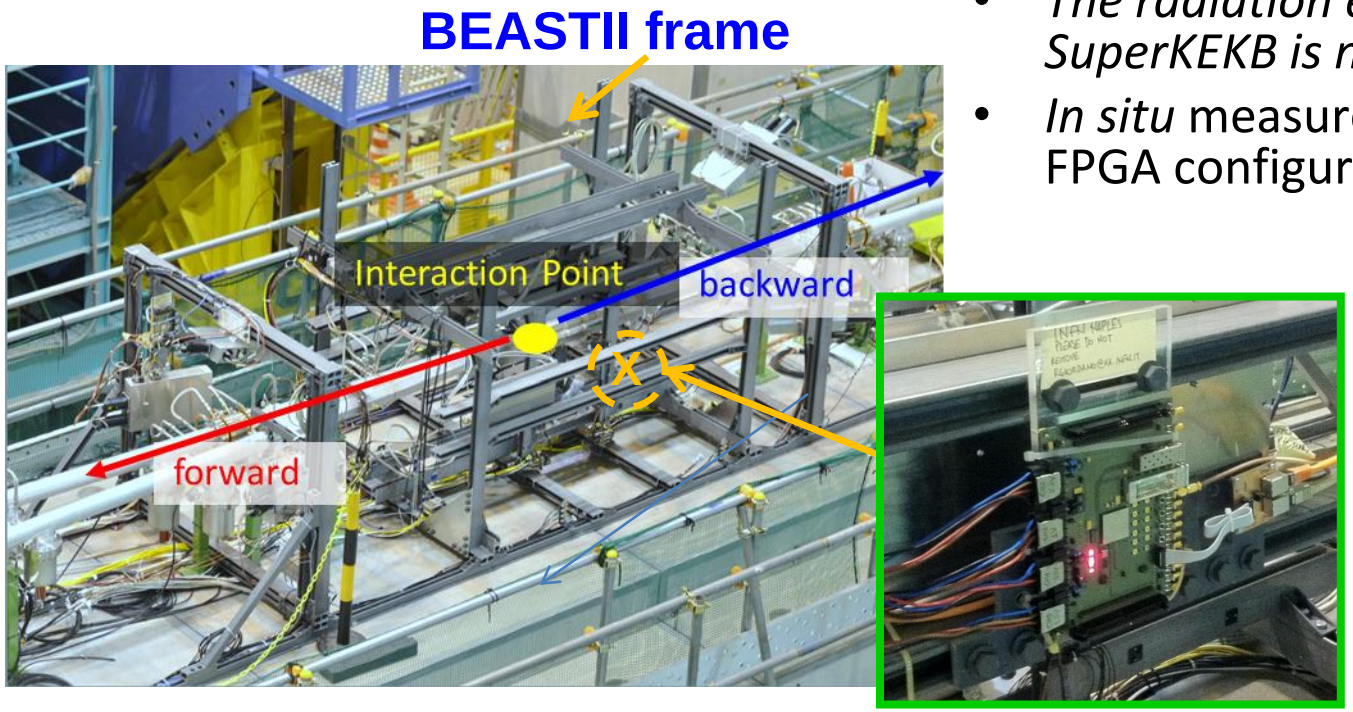
The SuperKEKB Collider



2013/July/29	LER	HER	unit
E	4.000	7.007	GeV
I	3.6	2.6	A
Number of bunches	2,500		
Bunch Current	1.44	1.04	mA
Circumference	3,016.315		m

- SuperKEKB e+e- KEK (Tsukuba, Japan)
- B factory, designed for search of new physics at the intensity frontier
- Main design parameters
  - Target L= 8×10^{35} Hz/cm^2
  - LER (e+) 4 GeV, HER (e-) 7 GeV
- Single collision point: Belle2 detector
- Phase 1 commissioning completed (Feb. to Jun. 2016)

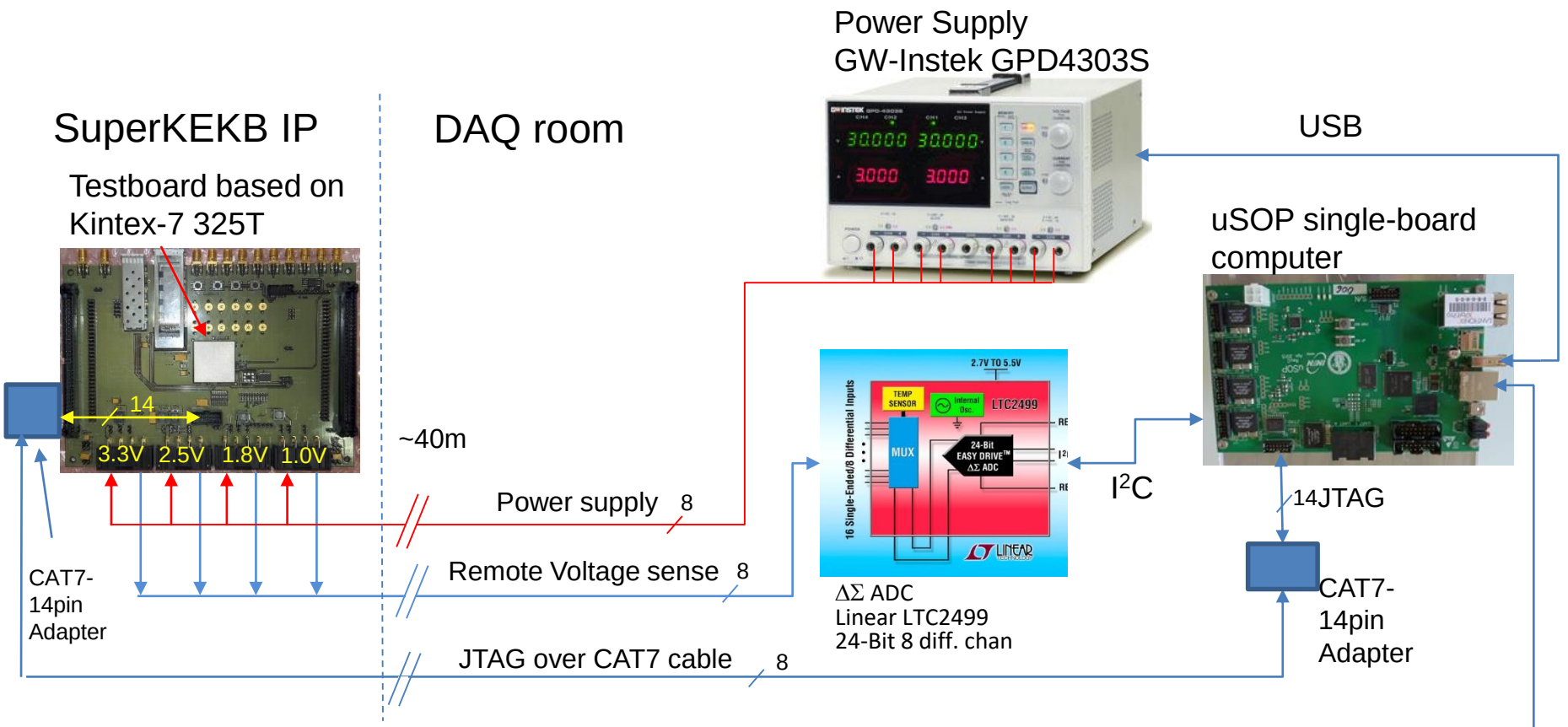
FPGA Setup at SuperKEKB



- *The radiation environment at SuperKEKB is not well known*
- *In situ* measurement of upsets in FPGA configuration memory

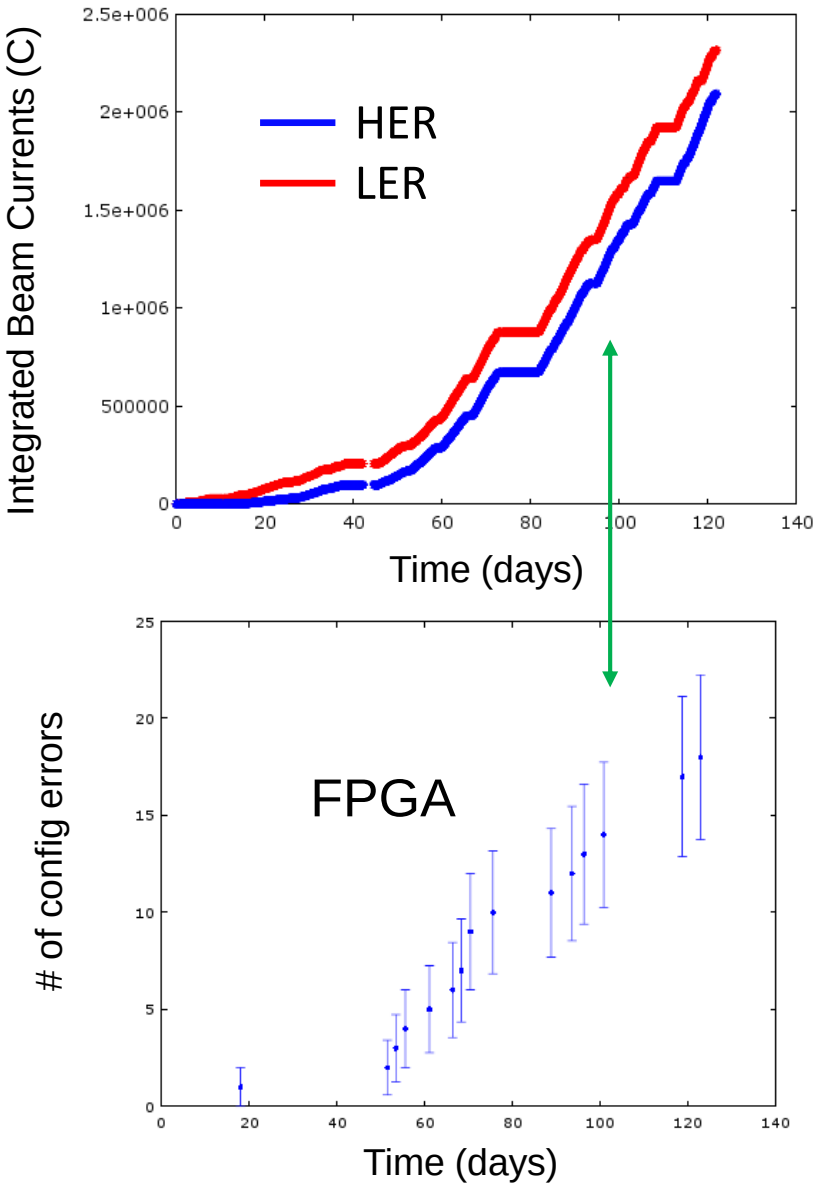
- BEASTII commissioning detector aimed at measuring machine backgrounds (see this afternoon's talk by P. Lewis)
- FPGA installed on the BEASTII support frame (~1 m from the beam pipe)

Test Setup



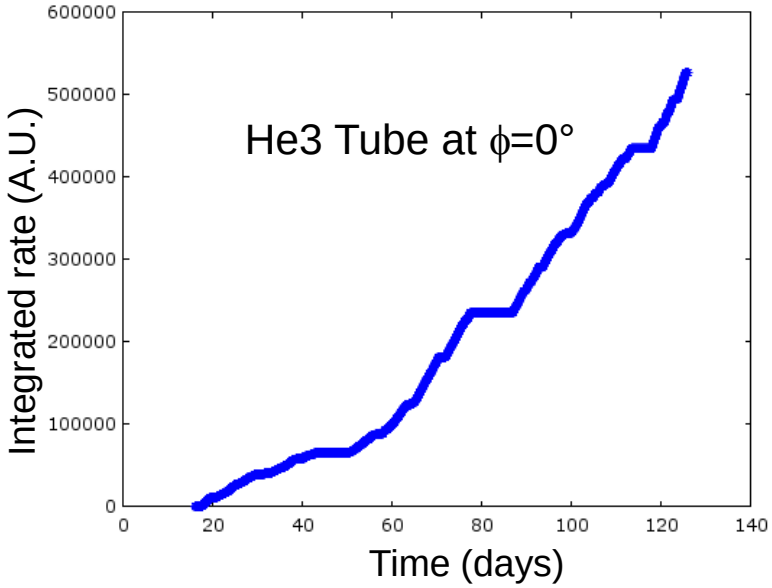
- Custom designed FPGA testboard, no other active components
- USB-controlled power supply, 4 channels for FPGA supply domains
- 24-bit sigma-delta ADC for voltage sense at FPGA
- uSOP single-board computer, controls power supply, ADC and FPGA configuration/readback via JTAG, remote control via LAN
- More details on uSOP in next talk (F. Di Capua)

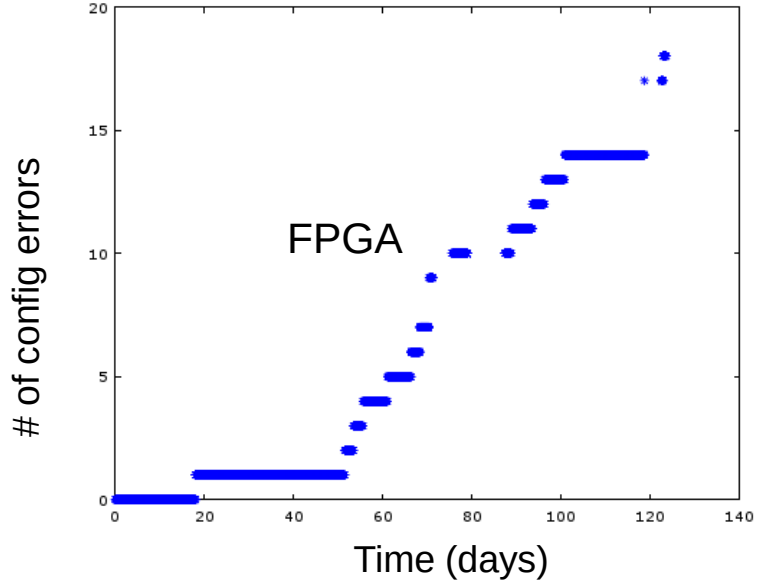
Results



- During SuperKEKB operation from Feb. 14th to June 11th
- FPGA upset count had a similar trend to integrated beam current
- 18 configuration errors detected out of $91.5 \cdot 10^6$ configuration bits
- Average rate 0.15 SEUs/day (or 1 SEU every 6.7 days)
- Results from PIN diodes at BEASTII (M. Nayak, 25th Belle2 General Meeting) => total dose @FPGA < 300 krad
- Negligible variation in currents absorbed by FPGA (< 1mA, i.e. no TID effects)
- FPGA is still fully functional, no permanent damage
- Beam currents will increase in SuperKEKB phase2 and beams will be focused, so it would be interesting to continue data taking when that will happen

Upsets vs He3 Tube Events





- Four He3 tubes were installed around the beam pipe, at distance of nearly 1 m from IP, at ϕ=0°, 90°, 180°and 270°
- FPGA test board behind tube at ϕ=0°
- He3 Tube integrated rate follows integrated beam current very well
- So does FPGA error count

Error Logs

Readback time
(i.e. uncertainty in SEU time stamp)

Extract from error logs

```
date = 04/13/2016:23:15:41 | total_errors = 0 | Verify of 28291 frames took 917 seconds
date = 04/13/2016:23:30:58 | total_errors = 0 | Verify of 28291 frames took 917 seconds
date = 04/13/2016:23:46:15 | total_errors = 0 | Verify of 28291 frames took 917 seconds
…
date = 04/20/2016:17:21:45 | total_errors = 838 | Verify of 28291 frames took 911 seconds
ERROR(s) | date = 04/20/2016:17:24:27 | frame_addr = 00021B16 | flipped bits = 0328:0->1
total_errors = 839
ERROR(s) | date = 04/20/2016:17:26:32 | frame_addr = 00042620 | flipped bits = 2077:0->1
total_errors = 840
ERROR(s) | date = 04/20/2016:17:26:33 | frame_addr = 00042621 | flipped bits = 2077:0->1
total_errors = 841
ERROR(s) | date = 04/20/2016:17:32:18 | frame_addr = 0044070B | flipped bits = 1947:0->1
total_errors = 842
…
```

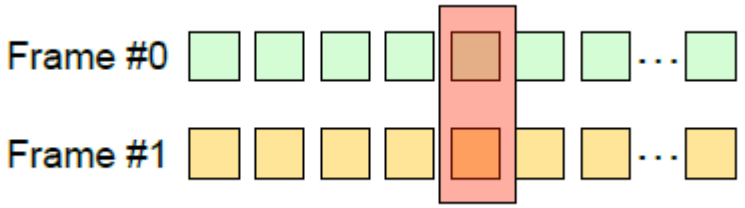
MCU

Adjacent frames

same bit offset

- Custom script for JTAG readback
- For each detected upset we log time stamp, frame address and bit offset
- Detected some MBUs, which appeared as SEUs due to bit interleaving in K7 frames
- All the measured errors can be corrected by 7 series FPGA embedded configuration error correcting code

- Total 18 upsets
  - 16 SEUs
  - 1 MBUs (2 upsets)



[1] M J Wirthlin et al., 2014 JINST 9 C01025

Conclusions and…

- FPGA installed in BEASTII provided us with preliminary information about the expected upset rate
- Measured upset rate is very low (0.15 upsets/day)
  - 7-Series built-in error correcting code can fix single errors in one frame
  - soft error mitigation (SEM) controller could be employed to fix double upsets per frame
- Negligible TID effects in FPGA power consumption
- Beam currents will increase and so will backgrounds => SEU monitoring will continue in BEAST phase2 (Belle2 detector rolled in)

Acknowledgement

- We thank S. Vahsen, P. Lewis, H. Nakayama, A. Beaulieu, S. De Jong, I. Jaegle, M. Hedges and all the other members of the BEASTII community for supporting this activity
- This work is part of the ROAL project (grant no. RBSI14JOUV) funded by MIUR in the framework of the 2014 Scientific Independence of young Researchers program