A custom readout electronics for the BESIII CGEM detector

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on behalf of the CGEM-IT Group

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Instrumentation for Colliding Beam Physics (INSTR-17)
Novosibirsk, Russia
27 February - 03 March, 2017

The BESIIICGEM project has been funded by European Commission within the call H2020-MSCA-RISE-2014.
Outline

1. Overview of the readout electronics for the BESIII-CGEM

2. On-detector Electronics: Design of a dedicated ASIC for CGEM Readout

3. Preliminary results from TIGER Prototype

4. On-detector Front-end Board

5. Off-detector Electronics

6. Outlook for the CGEM electronics
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Overview of the CGEM detector electronics

**ON-DETECTOR ELECTRONICS**

- ~ 10 000 CHANNELS
- Preamplifier Boards
  - 128 channels
- ~ 80 cables
- ~ 10 m
- 160 ASIC -> 80 BOARDS

**OFF-DETECTOR ELECTRONICS**

- Data Readout
  - 512 chs board
  - 20 DATA READOUT BOARDS
- DCS Concentrator Boards
- 2 CONCENTRATOR BOARDS
- DAQ
  - Concentrator Boards
  - 2Gbps Optical links
  - VME bus
  - GbE link

**Institutions**

- INFN-TORINO
- INFN-LNF
- INFN-FERRARA
- Uppsala U
- IHEP-China Torino U
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An analogue readout of the CGEM enables the use of a charge centroid algorithm, improves spatial resolution to better than 130 µm, while loosening the pitch strip to 650 µm. The total number of channels is approximately 10,000.

- 10,000 Channels in 80 Front-end Boards
- 2 ASICs per FEB
- Readout with 160 dedicated integrated 64-channel front-end ASICs
  - Should provide time and charge measurement and feature a fully-digital output
  - Expected signal from CGEM: 30-50 ns Duration, 30-40 ns rising time, 10 ns falling time
    - Depends on gas mixture, gain, and electric field
  - Input charge: 1 - 50 fC
  - Up to 100 pF sensor capacitance
  - 60 kHz Rate per Channel (safety factor of 4 included)
  - 4-5 ns Time resolution
  - Power below 10 mW/channel
  - SEU-tolerant

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1 Lia Lavezzi, "The new Cylindrical GEM Inner Tracker of the BESIII experiment: test beam results of two prototypes".
Front End Design - Preamplifier

- low-noise two-stage cascode charge sensitive amplifier
- signal range $Q_{in} = 1 - 50 \, \text{fC}$ on a $C_d = 100 \, \text{pF}$ detector
- target ENC 800 electrons
- up to 80 mS (4 mA bias current) on input PMOS
- $\text{Gain} = 10 \, \text{mV} / \text{fC}$
- operation in $\mu$ - TPC mode: requirement for a 5 ns time resolution
- signal split for time and charge measurement branches in two dedicated shapers
Front End Design - Dual Shaper

- 4 complex conjugate poles, peaking time defined by feedback loop RC
- semi-Gaussian output signal shape
- maximum signal width 1 $\mu$s on energy shaper, pile-up probability < 1% at 60 kHz
- 250 ns peaking time on energy branch, minimises ENC for charge measurement
- 60 ns peaking time for fast shaper, targets low-jitter timing measurement
- baseline DC (typ 300 mV) imposed by BLH circuit
  - transconductance function is slew-rate limited, rejects variations caused by fast signals
  - dominant time constant $\tau = 1.5$ ms generated with very small bias currents
Overview of the channel

- **Time-based readout**
  - single or double threshold
  - time stamp on rising/falling edge (sub-50 ps binning quad-buffered TDC)
  - charge measurement with Time-over-Threshold

- **Time and amplitude sampling**
  - time stamp on rising edge (sub-50 ps binning quad-buffered TDC)
  - Sample-and-Hold circuit for peak amplitude sampling
  - slow shaper output voltage is sampled and digitised with a 10-bit Wilkinson ADC
Low-power analogue TDC is based on time interpolation, event de-randomization with multiple hit buffering (4x TAC)

interpolation factor 128 : time binning < 50ps with a 160 MHz clock
quad-buffers for voltage sampling, **S/H circuit shares Wilkinson TDC** for digitisation

- sampling starts at **rising edge** of fast (Time) or slow (Energy) shaper output

- **sampling time (target equal to peaking time)** is programmable, defined by simulation and confirmed by parameter scan in silicon

- deviation on measured amplitude **versus** peak amplitude, due to time-walk, is corrected by calibration
TIGER: ASIC Prototype for the CGEM Readout

- **64 channels**: VFE, signal conditioning, TDC/ADC, local controller
- Digital backend inherited from TOFPET2, SEU protected
- on-chip bias and power management
- on-chip calibration circuitry
- fully digital output, LVDS IO
- 4 TX SDR/DDR links, 8B/10B encoding
- SPI configuration link
- power below 10 mW per channel
- nominal 160 MHz system clock
- sustained rate per channel: above 100 kHz
- 25 mm² UMC110 CMOS
- tapeout of first silicon: MPW May 2016

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Status of ASIC Test Activities, in a nutshell

Summary of activities
- Electrical characterisation started November 2016 - tests on 6 chips
- Preliminary tests with diodes ongoing
- Test with planar and cylindrical GEM starting in March
- Trial TID run on testboards done, high-dose TID and SEU tests planned for mid-2017

Summary of characterisation runs
- R/W Channel/Global configuration registers
- Data TX and decoding
- (dual-) TDC operation and fine calibration
  - quantisation error lower than 40 ps r.m.s.
- Front-end performance
  - internal calibration circuitry
  - external charge injection (spy channel)
  - Charge measurement: Time-over-threshold
  - Charge measurement: S/H
- Baseline and threshold equalisation
- Channel intrinsic noise: noise vs. Cin (ongoing)
Gain dispersion

- Injection of $Q=8\text{fC}$ with internal test-pulse
- Average gain above 10mV/fC (expected 11mV/fC from post-layout simulations)
- Residual channel-to-channel dispersion (0.2 mV/fC r.m.s.)
- Results after baseline equalisation: below 25 mV r.m.s. dispersion on the DC operating point
Charge Measurement - ongoing

- Charge Measurement with a **Sample-and-Hold circuit** or Time-over-threshold (single/dual Vth)
- Calibration of dynamic range with external test-pulse generator (managed by test DAQ SW)
- Back-annotation to generate a parameter space for the internal calibration circuit
- Charge measurement below 5 fC a problem with single-threshold - Next: work on double-threshold operation
- Still, Fast Branch noise higher than expected
Noise measurements - preliminary results for Fast Branch

- Threshold scan (N meas/point, typ 50) for a fixed internal calibration circuit TP
- Normalise efficiency and fit with sigmoid for noise evaluation
- Repeat M times (typ 100)
- Plot noise and std deviation of measurement
- Sweep input capacitance and repeat measurement
  - ENC @ Cin 100 pF $\approx 2500$ e-
  - expecting $1700$ e- from post-layout simulations at $T=40^\circ C$
- PSRR, interference and grounding: under study

ENC (Cin)

![Graph showing ENC (Input Capacitance)]

$\chi^2$ / ndf $= 1.891 / 7$

constant $= 1529 \pm 132.4$

slope $= 10.78 \pm 2.321$
- Dual-branch TDC scanned over dynamic range (sweep TP phase)
- Create LUT with gain and offset correction for all channels
- Average TDC quantization error after calibration \( \approx 30 \text{ ps r.m.s.} \)
- Re-use method with TP injected to front-end to quantify intrinsic jitter - tbd
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FEB Design for the on-detector electronics

Contact person: Marco Mignone - INFN Torino

L3
- Board FE1 (56x40mm)
  - 2 ASICs, biasing and references, filtering
  - ESD protection network for 122 channels
  - 2 Analogue domain power regulators
  - connector towards anode
  - connector towards FE2
    ➞ Routing done, waiting confirmation on anode connector
- Board FE2 (56x30mm)
  - 2 Digital domain power regulators
  - 7 LVDS Buffers
  - connector towards FE1: power, signalling
    ➞ Routing done

L1-L2
- Board FE1 (56x52.8mm)
- Board FE2 (56x67mm)
  ➞ Layout to be started, relaxed clones of L3
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Each of the 20 Read-Out Cards (ROC) handles 4 ASIC PCBs (8 ASICs)

Prototype is based on an ALTERA e-kit (ArriaVGX FPGA), coupling to motherboard through HSMC high performance connector

Motherboard provides electrical and physical interfaces to the ASIC carrier PCBs, to the data concentrator (bi-directional fibre optic links) and the BES-III Fast Control system. Ethernet port also available for monitoring and debugging.

2 Advanced Trigger Logic Board (ATLB) Data Concentrators manages interface with VME based BESIII DAQ system.
each triple CGEM requires 7 voltages (range: 0-5 kV)

each CGEM voltage must be distributed to many macro/micro sectors to reduce the section capacitance and the energy released in case of discharge

the system allows to monitor the current dragged by each CGEM foil (nA sensitivity)

the system allows to disconnect a single micro-sector in case of local short to minimise the system dead-zone
CGEM not be accessible after its insertion into the BESIII apparatus

→ tracker services (i.e. HV and LV generation and distribution) designed with reliability as primary goal
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On-detector FEB Design

✅ on-schedule, space/volume criticality of L3 design overcame

Status of Readout ASIC

✅ Time-based readout working properly
✅ Charge measurement with S/H ok
→ BLH temperature/VDD sensitivity minor revision ongoing, corrected for engineering version
→ Noise and grounding sensitivity under study
✅ Organising SEU, TID beam tests
✅ First tests with planar and cylindrical GEMs in March
✅ Engineering run during 2017, minor fixes and design flavours

Off-detector Electronics

✅ First smoke tests with TIGER ongoing - data reconstruction from test-pulses
Thank You!

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Backup Slides
Baseline scan

- Threshold scan on all channels, for T1 only (single-threshold mode)
- Baseline saved at 50% level of the sigmoid
- below 25 mV r.m.s. dispersion

![Graphs showing baseline scan results]
Threshold equalisation

- A 64-channel baseline scan is performed on every chip
- Threshold scan results are saved on a LUT
- The same effective threshold is set for all channels during acquisition

→ example of a ToT charge measurement before (below, left) and after (below, right) the equalisation.
TDC/ADC - simulation of one event

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03.03.2017, INSTR-17, Novosibirsk